1800V Bipolar-Mode MOSFETs: a first application of Silicon Wafer Direct Bonding (SDB) technique to a power device

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Abstract

1800V and 1700V non-latch-up Bipolar-Mode MOSFETs have been developed, based on Silicon Wafer Direct Bonding (SDB) technique: a new substrate wafer fabrication process superior to conventional epitaxy. The SDB technique easily realizes an optimum N buffer structure as well as a high resistivity N^- layer. Self-aligned deep P^+ diffusions, densified hole bypasses and an amorphous silicon resistive field plate have been implemented. 0.45μsec fall-time and more than 100A maximum current capability have been successfully realized.

1. Introduction

It has become widely recognized that Bipolar-Mode MOSFETs[1] are superior to both bipolar transistors and power MOSFETs in respect to switching speed[2], current handling capability[3], blocking voltage[1] and even SOA[4]. Total chip area for 1000V (sustaining voltage), 50A Bipolar-Mode MOSFETs[5] with 0.5μsec fall-time is $144mm^2$, whereas that for equivalent Darlington bipolar transistors is $198mm^2$. Latch-up in the parastic thyristor, which is the main drawback for Bipolar-Mode MOSFETs, had been successfully suppressed, so that the device practically attained non-latch-up characteristics[6,7]. 20kHz high frequency operation can easily be realized by Bipolar-Mode MOSFETs, realizing low noise inverter systems.

This paper presents 1800V[8] and 1700V Bipolar-Mode MOSFETs. Four major breakthrough technologies have been developed for these devices. These are silicon wafer direct bonding (SDB) technique[9]: a new silicon wafer fabrication process, superior to conventional epitaxy, an amorphous silicon resistive field plate[10], a new self-aligning process for deep p^+ diffusion and an improved hole bypass structure. This paper, for the first time, reports on an application of the developed SDB technique to a semiconductor device, as an alternative method for conventional epitaxy.

The developed devices exhibited excellent electrical characteristics: 3.8V forward voltage drop for 10A drain current, 0.45μsec fall time and more than 100A maximum turn-off current. Allowable power dissipation for 10μsec DC pulse operation reached $8x10^5W/cm^2$, which exceeds the theoretical limit for npn bipolar transistors.

2. Silicon Wafer Direct Bonding (SDB) technology

Silicon wafer direct bonding technology has been developed. It is superior to conventional epitaxy because SDB completely eliminates problems, associated with conventional epitaxy such as auto diffusion. Thus, a high resistivity layer as well as an optimum n-buffer structure were easily realized by the SDB technique.

Silicon wafer bonding was carried out by facing and contacting two mirror polished wafer surfaces after hydrophilizing surface treatment. Bonding as rigid as the original bulk material is achieved by thermal treatment at more than 1000°C ambient temperature .

The SDB process sequence applied to the 1800V and 1700V devices is shown in Fig. 1. First, a mirror polished high resistivity bulk wafer and a low resistivity p^+ substrate wafer were prepared. An n type dopant, such as phosphorus, was implanted into the mirror surface of the high resistivity bulk wafer and was driven-in to form an n^+ diffusion layer. Then, a p type dopant, such as boron, was introduced, forming a shallow p^+ diffusion layer on the n^+ layer. Finally the two mirror surfaces of the p^+ substrate and the bulk wafer were faced together and bonded, in the manner stated above, to form an $n^-/n^+/p^+$ structure. The high resistivity n^- layer thickness can be adjusted by conventional lapping technique. Figure 2 shows a TEM lattice image for the bonded interface. It is seen that the lattice continues through the interface although a large number of defects are observed. No electrical barrier was observed at the bonded interface. Ordinary MOSFET fabrication processes are applied to the thus bonded wafers, yielding Bipolar-Mode MOSFETs. Because a lager number of defects exist at the bonded interface at present, SDB should not be carried out inside the device, where large carrier lifetime is required.

3. A new junction termination technique

The ability to withstand high voltage has to be realized with the use of shallow diffusion layers because shallow junction are generally used in power MOSFETs for low on-resistances. It was found that an optimized combination of a resistive field plate and a metal field plate easily realize 1800V breakdown voltage (80 percent of ideal breakdown voltage) with an only 450μm wide junction termination area and 10μm deep diffusion layers. Figure 3 shows the structure adopted for 1800V devices. A source metal layer extending over an oxide film serves as a metal field plate. A high resistance a-Si

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CH2381-2/86/0000-0122 $1.00 © 1986 IEEE

film deposited over an oxide film and metal layers create a linear potential gradient on the thick oxide film. The combined structure smoothly terminates the depletion layer created by the applied voltage. Withstanding voltage has its maximum for an optimized metal field plate length.

4. Stripe or square for a source-gate geometry ?

Hex or square patterns have been conventionally adopted for power MOSFETs. However, these patterns are not necessarily the best patterns for Bipolar-Mode MOSFETs, once latch-up susceptibility is taken into consideration. Figure 4 shows a relation between forward voltage vs. latch-up current as a function of gate polysilicon width L_G (source to source distance) defined in Fig. 4. Regarding the square pattern, as L_G increases, forward voltage first decreases and then increases again, while latch-up current simply decreases. On the other hand, regarding the stripe pattern, forward voltage decreases as L_G increases for the examined L_G range. However, latch-up current does not decrease significantly. Thus, the stripe pattern realizes better overall characteristics. Bipolar-Mode MOSFETs have been adopting the stripe pattern since their beginning[1,11].

5. Self-aligned deep p^+ diffusion

Accompishing a deep p^+ diffusion, as near the channel region as possible[12], is one of the effective methods to reduce P-base resistance and, thus, to increase latch-up current level. A new self-alignment process was developed to satisfy this requirement. Figure 5 shows the layout diagram for the developed process. (1) First, a deposited polysilicon layer is selectively etched to form a gate polysilicon layer(a) and additional islands(b). (2) These islands(b), together with a resist layer(c), are used as a mask to block implanted ions. The edge of the island(b) defines the deep p^+ diffusion edges. (3) Then, the polysilicon islands(b) are selectively etched-off, before thermal drive-in for the deep p^+ diffusion layer. The conventional DSA process for the P-base and n^+-source is, then, carried out, using the gate polysilicon layer as a mask. The final device structure achieves three self aligned layers (deep p^+, P-base, n^+-source). Addition of the self-aligned deep p^+ layer significantly improved SOA by more than 50 percent, as compared with a $4\mu m$ deep P-base device without a deep p^+ diffusion.

6. Densified hole bypass

Figure 6 shows hole bypass structure adopted for 1800V devices. In this structure, part of the source layer is not cut off. Instead, parts of the heavily doped shallow p^+ layer extend even into the channel region. This new hole bypass structure has the same effects as the previous one[6], and even has a merit in that finer hole bypasses can be easily created.

New hole bypass structure effectively reduces the saturation current without sacrificing forward voltage, since channel resistance occupies only a small fraction of total device resistance.

7. Developed device electrical characteristics

Two types of 1400V sustaining voltage devices with 1800V(A) and 1700V(B) static breakdown voltages have been fabricated. Both adopted the stripe pattern and the additional shallow p^+ diffusion. Device B(1700V) further adopted the self-aligned deep p^+ diffusion and the hole bypass structure. Consequently, it has a tripply diffused P-base. Figure 7 shows a photograph for a fabricated device. Chip size is 6x6mm with $20mm^2$ active region. Device B attained lower forward voltage drop 3.8V for 10A drain current and $0.45\mu sec$ fall-time at the cost of lower breakdown voltage by adopting a narrower N-base as compared with device A with 4.5V forward voltage. Figure 8 shows typical trade-off relations between forward voltage and fall-time (resistive load).

Temperature dependence of the fall-time was also improved by adopting device B design (narrower N-base). The fall-time for device A becomes triple from 25°C to 125°C, whereas the fall-time for device B becomes only double.

Figure 9 shows high voltage high current region saturation characteristics for device A, measured by $10\mu sec$ DC pulses. Latch-up current density is far above the saturation current for 15V gate voltage. The broken line in Fig. 9 shows the shortcircuited SOA measured by the circuit shown in Fig. 10. Figure 11 shows typical waveform for the shortcircuited SOA measurment. 1000V drain voltage was continuously applied to the device. Allowable power dissipation for 10 μsec DC pulse reached $8\times10^5 W/cm^2$. To the authors' knowledge, this value is the largest ever reported.

Maximum turn-off current is sufficiently large as seen in Fig. 12. More than 100A drain current can be turned-off within 300 nsec under an inductive load.

8. Conclusion

1800V and 1700V Bipolar-Mode MOSFETs have been fabricated, based on four breakthrough technologies. Both have more than 1400V sustaining voltage, $0.45\mu sec$ fall-time, and more than 100A turn-off capability as well as non-latch-up characteristics.

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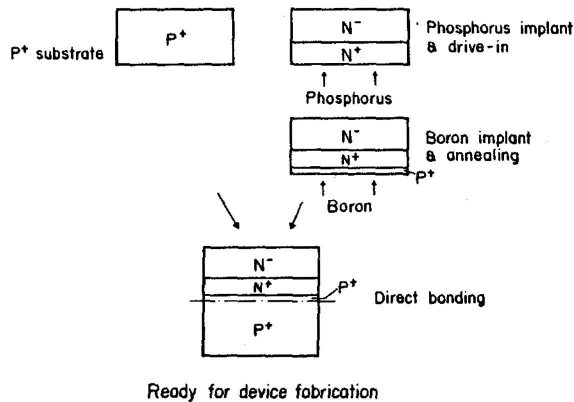

Fig.1 Silicon wafer direct bonding process sequence.

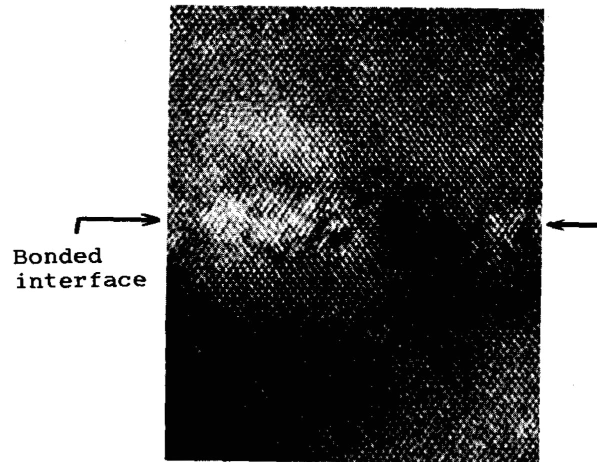

Fig.2 TEM lattice image.

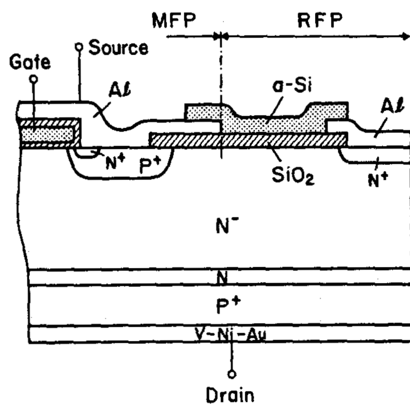

Fig.3 Junction termination technique for 1800V devices.

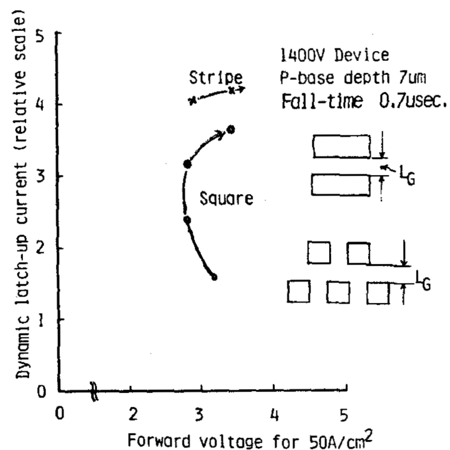

Fig.4 Dynamic latch-up current vs. forward voltage relationship as a function of source to source distance (gate polysilicon width:L_G).
Arrows indicate the direction for a decrease in L_G.

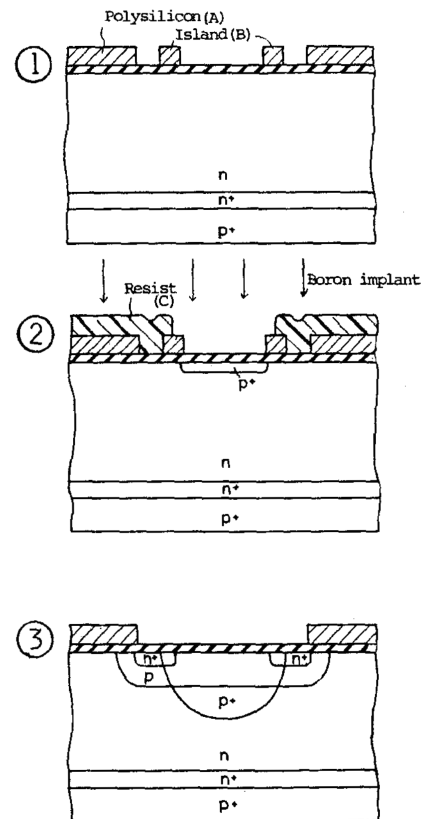

Fig.5 New self-aligning process using only polysilicon layer as diffusion mask.

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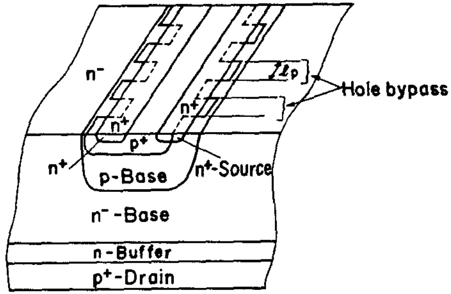

Fig.6 Improved hole bypass structure. (ℓ_p is only several microns)

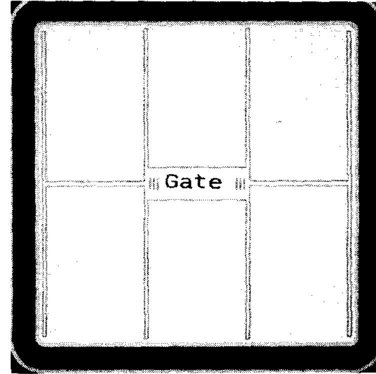

Fig.7 1800V 10A device chip.

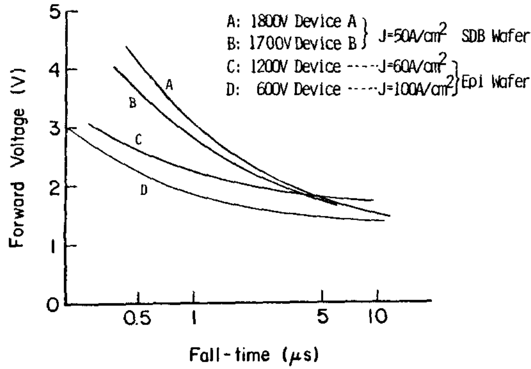

Fig.8 Trade-off curve between forward voltage and fall-time.

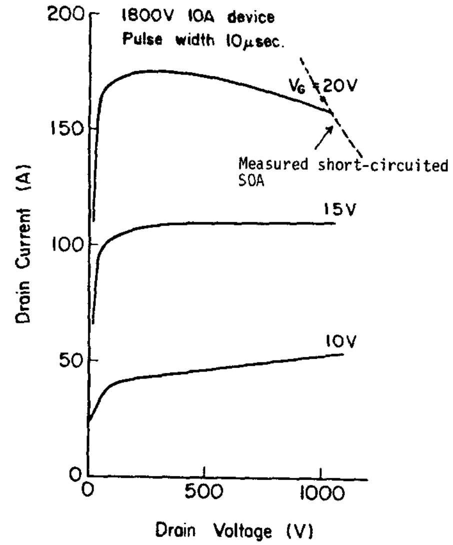

Fig.9 High voltage high current saturation characteristics and shortcircuited SOA (broken line).

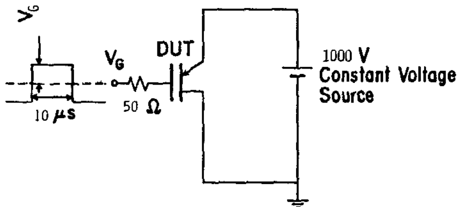

Fig.10 Test circuit for shortcircuited SOA measurement.

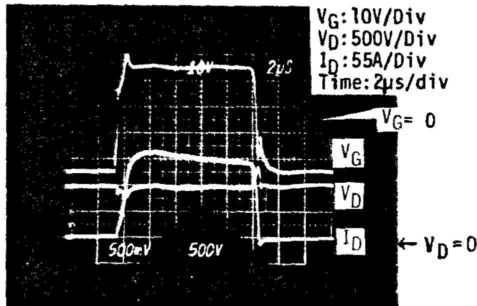

Fig.11 Typical waveform for shortcircuited SOA measurement.
1000V drain voltage is always applied to the device.

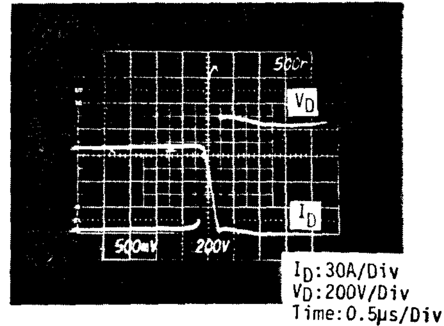

Fig.12 Typical 100A inductive turn-off waveform.
Peak drain voltage reached 1280V.

Fig.2 TEM lattice image.