Experimental and Numerical Study of Non-Latch-Up Bipolar-Mode MOSFET Characteristics

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Abstract

Bipolar-Mode MOSFET characteristics were experimentally and numerically analyzed. It was found that parasitic pnp transistor common base current gain of greater than 0.27 is necessary to realize low forward voltage drop, because carrier distributions are different from those for diodes. It was also found that three decay phases can be distinguished in the turn-off current waveform . A critical current-voltage border beyond which avalanche injection occurs was obtained from the model analysis. Safe operating areas for Non-Latchup Bipolar-Mode MOSFETs are also presented. Current concentration hardly occurs in Bipolar-Mode MOSFETs if avalanche injection is avoided.

1 Introduction

600 and 1200V Bipolar-Mode MOSFETs (also called IGT[1] or COMFET[2]) have achieved non-latchup characteristics[3], which means that the device maximum current is limited not simply by latchup mechanism but by other mechanisms such as channel saturation current or avalanche injection. Observed forward safe operating area(SOA) limit in terms of voltage and current density product exceeded $2.5X10^5$VA/cm^2 for 800V drain voltage and 10μsec. pulse operation even at 125°C case temperature. This high current capability was realized by① stripe source gate pattern[4,5],② double diffused p-base with a hole bypass[3] and③ n^+-buffer layer[4,5](see Fig.1).

In the present paper, basic operating mechanism as well as above stated current capability are experimentally and numerically analyzed, for the first time, using a time dependent 2-d model.

2 Steady state characteristics

Analyzed 600V device structure is shown in Fig. 2. Calculated current-voltage curves for a series of hole lifetimes τ_p are shown in Fig.3. The adopted assumptions are that (1) $\tau_n=\tau_p$, (2) flat band potential Ψ_{FB} =-2.5V (V_{TH}=4.0V), (3) V_G=12.5V and (4) gate oxide thickness=1000Å. The calculated results agrees well with experiments as shown in Fig.4, where both experimental and calculated forward voltage vs. carrier lifetime characteristics are compared. Carrier lifetime values were obtained through the measurement of drain current decay time constant[6], based on the results described in Section 3.

Figure 5 shows electron and hole current flow lines for the case of 125A/cm^2 current density and 0.5μsec. hole lifetime. It should be noted that hole current flows much more uniformly even beneath the p-base layer than electron current. However, for low hole lifetime cases such as 50nsec., even hole current flows not uniformly as shown in Fig.6. Percentage of electron current over total current at the source electrode side of the n-base increases from 40% to 77% as hole lifetime decreases from 5μsec. to 50nsec. This ratio significantly influences device characteristics as shown in the following. In the high injection condition such that $p\cong n$ holds in the n-base, at carrier density minimum point in the n-base, if it exists, the ratio of electron current over hole current (J_n/J_p) is equal to the mobility ratio because diffusion current components are zero. The electron current ratio over total current is $\mu_n/(\mu_n+\mu_p)$ (=0.73) at the carrier density minimum point[7]. Thus, if electron current ratio is less than 0.73 at the source electrode side of the n-base, there is no carrier density minimum point in the n-base, and the carrier density decreases monotonically from the drain electrode side of the n-base to the source elecrode side. This example is seen in the upper curve in Fig.7, where carrier densities on the X=25μm line (symmetry axis through the center of the gate electrode; see Fig.2 for X,Y-coordinates) are plotted. However, if electron current ratio becomes above 0.73, a minimum point appears in the n-base. Moreover, carrier density at the Y=5μm point on the X=25μm line decreases as carrier lifetime decreases (the reason is given later). Therfore, for a low carrier lifetime case, carrier density in the n-base has to be very small, because carrier density at the minimum point in the n-base must be still smaller than that for Y=5μm point. The carrier density at the Y=5μm point on the X=25μm line is related to the hole current density J_p flowing into the p-base. Roughly speaking, the following equation holds.

$$J_p \propto 2qD_p\, p(Y=5\mu m)/L, \quad ....(1)$$

where L denotes $L_G/2$ (see Fig.1 for the definition). Assume that carrier lifetime is decreased while retaining the total drain current at the same level. J_p value has to decrease because electron current ratio increases. Thus, it is concluded from Eq.(1) that hole density p at the Y=5μm point must decrease with decreasing carrier lifetime. Electron density at the Y=5μm point also has to decrease to increase electron diffusion current(electron density gradient) and to increase the electron current ratio. Summarizing the results, conductivity modulation in the n-base is not sufficient, if electron current ratio over total current at the source electrode side of the n-base is greater than 0.73. In other words, this is true if common base current gain of the pnp transistor is less than 0.27.

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As the current gain of the pnp transistor is a function of W_n/L_a, where W_N and L_a denote n-base width and ambipolar diffusion length in the high injection level, respectively, L_a should become larger in proportion to the increase in W_N for a high voltage device. As is shown in Section 3, Turn-off time is closely related to carrier lifetime $\tau_n + \tau_p$. It follows that shortest obtainable turn-off time must increase with an increase in n-base width.

Although several papers assumed diode like carrier distributions[8], electron injection from the channel is not sufficient for diode like carrier distributions. Bipolar-Mode MOSFET characteristics are, thus, assumed to lie between those for diodes and transistors in this respect. It is important to realize greater carrier density at the source electrode side of the n-base for a high switching speed and a low forward voltage, allowing a low pnp transistor current gain.

3 Switching-off characteristics

The analyzed circuit configurations are shown in Fig.2. A sufficiently large inductance with an ideal free wheel diode is adopted for a load impedance. Calculations were carried out under the assumptions that drain current is kept constant before the drain voltage recovers to 200V electric source voltage. The initial conditions for time zero are V_G= 12.5V, J_D=125A/cm^2 (V_D=1.8V) and $\tau_n = \tau_p$ =0.5μsec. Calculated waveforms are shown in Fig.8, where the channel current variation is also shown.

As the gate voltage decreases, the carrier densities beneath the center of the gate electrode begin to decrease. At t=0.27μsec., electrons are injected from the channel to the inner n-base through a narrow path as seen in Fig.9. Channel electron current completely ceases after the gate voltage reaches a point below the threshold. Drain voltage drastically increases in accordance with the decrease in channel electron current, accompanying depletion layer development beneath the p-base.

The stored excess electrons and holes adjacent to the depletion layer are swept away by the depletion layer expansion. The base current to the parasitic pnp transistor does not decrease even after the channel current cessation, because the swept away electrons from the depletion layer become the base current. The swept away holes cross the depletion layer, fowing into the p-base. It can be understood by comparing Fig.14 and 5 that the hole current flow become considerably uniform in the turn-off transient because of the current caused by the depletion layer expansion. After the channel current cessation, all the current(except displacement current) is carried by holes in the depletion layer. The positive ion density in the depletion layer(N_+), thus, is given by the Eq.(2).

$$N_+ = J_D/(qv_s) + N_D \quad , \quad ....(2)$$

where v_s denotes the hole saturation velosity and N_D the donor density. This situation causes avalanche injection if drain current density or drain voltage are excessively large.

Depletion layer expansion stops immediately after the drain voltage is clamped by a free wheel diode. Drain current rapidly reduces to a certain value and decays exponentially thereafter since the whole drain current flows due to the pnp transistor action. Figure 11 shows drain current variation on a logarithmic scale. Three decay phases are distinguished: first rapid decay phase, 2nd phase having a time constant nearly equal to high injection lifetime $\tau_n + \tau_p$, and the 3rd phase having a time constant of hole lifetime in the n -buffer.

Inserting a heavily doped n^+-buffer layer was proposed to improve forward voltage vs. fall-time characteristics[4,5] (see Fig.12). An n^+-buffer layer relizes short turn-off time in spite of large carrier lifetimes in the n-base. Then, decay time constant must be much shorter than high injection level lifetime in the n-base if an n^+-buffer layer is used.(The analyzed device does not use n^+-buffer)

4 Safe operating area

The following three items are assumed as causes for restricting the Bipolar-Mode MOSFET maximum current.

(1) Channel saturation current[3]

(2) Parasitic npn transistor action(parasitic thyristor latchup)

(3) Avalanche injection

For Non-Latchup Bipolar-Mode MOSFETs, parasitic npn transistor action is suppressed by optimized stripe source-gate pattern[4,5] and a hole bypass[3] so that latchup current density is far above the device saturation current. Parasitic thyristor latchup is not necessarily required and npn transistor action alone is sufficient for loss of gate controllability in the turn-off transient because the failure mode is quite similar to those for power MOSFETs.

Safe operating area for the Bipolar-Mode MOSFETs was measured by applying 5 to 25μsec. gate pulse and by connecting the device directly to the constant voltage source(400-800V). During the on-pulse, the device forward voltage become the same as the source voltage. Figure 13(a) shows the results. Device destruction occurs at the turn-off transient. Although the SOA's for the same rating bipolar transistors become narrow for more than 700V drain voltage range, SOA's for 1200V Bipolar-Mode MOSFETs do not, thus, implying uniform current flow in Bipolar-mode MOSFETs.

Figure 13(b) shows hole bypass effects on the SOA. An increase in the bypass area or an increase in its conductance improve SOA[3].

Generally, avalanche injection occurs when current density and voltage product exceed a critical value, which is given by combining Eqs.(2 and 3), assuming uniform hole current flow in the turn-off transient.

$$V_{BD} = 60(E_G/1.1)^{1.5}(N_+/10^{16})^{-3/4} \quad ......(3)$$

Figure 14 shows the calculated border line beyond which avalanche injection occurs. The equations can be used for the devices with a n-buffer because the depletion layer does not reach the n-buffer when the critical voltage is reduced to less than the static breakdown voltage. When the device current-voltage locus in the turn-off transient exceeds the border, fall-time increases. Figure 15 shows actual device turn-off waveforms, corresponding to the locus shown in Fig.14. If the drain current is less than several hundred Amperes, the stored energy in the stray inductance can be absorbed by the device itself. As avalanche injection occurs locally in a device, it will cause a current concentration. However, par-

allel device operation is successful if the current-voltage locus is controlled below the border in the turn-off transient.

References

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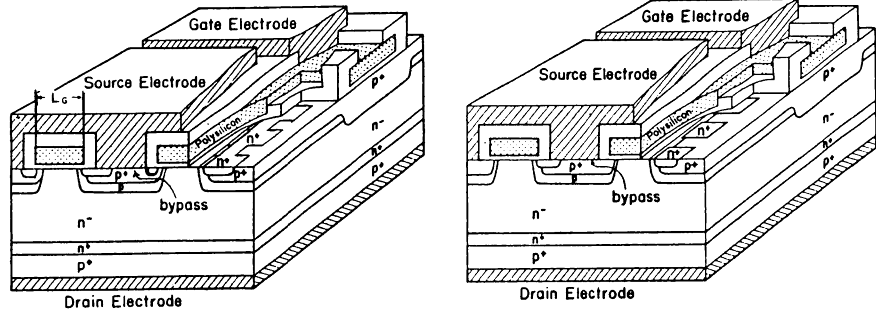

Fig.1 Two kinds of Non-Latchup Bipolar-Mode MOSFETs with Hole bypasses.

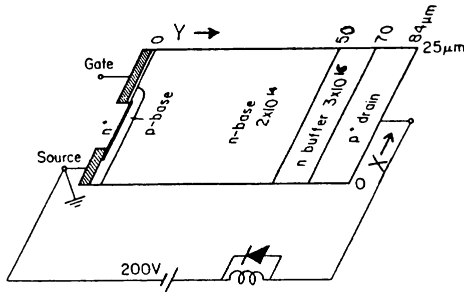

Fig.2 Analyzed device structure and Circuit configurations
An n-buffer (not n^+-buffer) is used in the analysis.

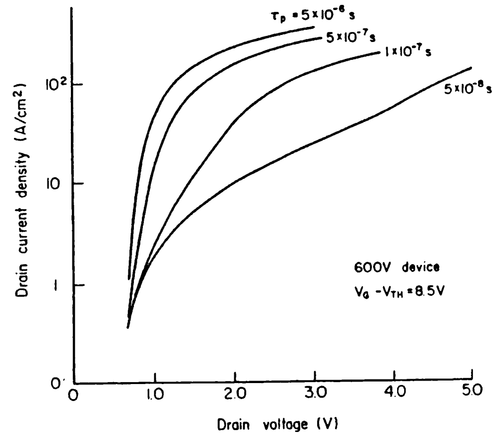

Fig.3 Calculated current-voltage curves with hole lifetime as a parameter

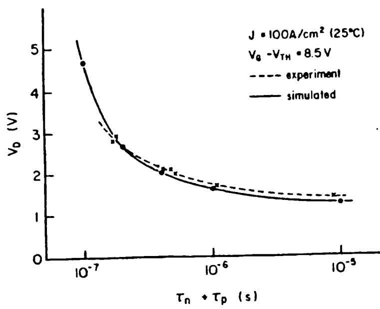

Fig.4 Experimental and calculated characteristic curves

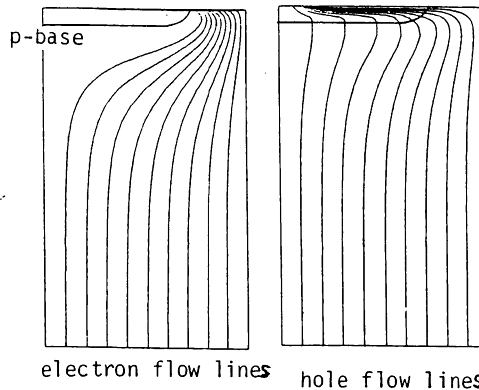

Fig.5 Calculated electron and hole current flow lines (τ_p =0.5μsec.)

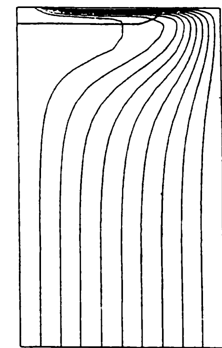

Fig.6 Hole current flow lines for τ_p =50nsec.

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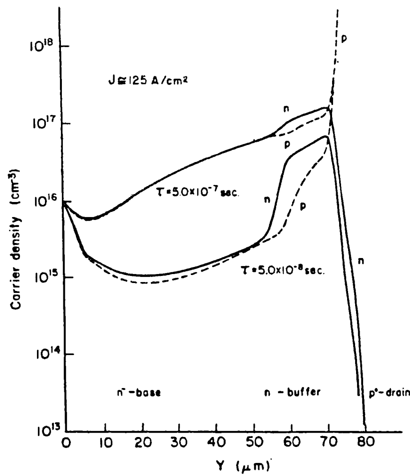

Fig.7 Carrier density distributions on x=25μm line for 0.5μsec. and 50nsec. τ_p cases.

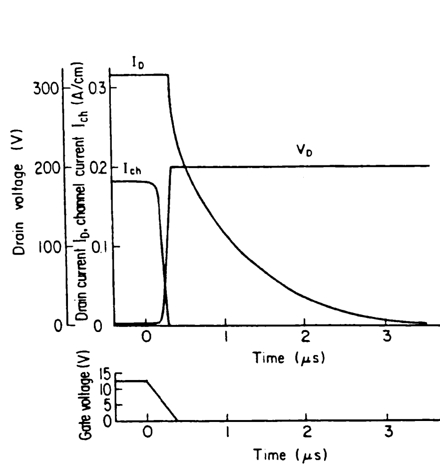

Fig.8 Calculated current voltage waveforms. Channel current variation is also shown.

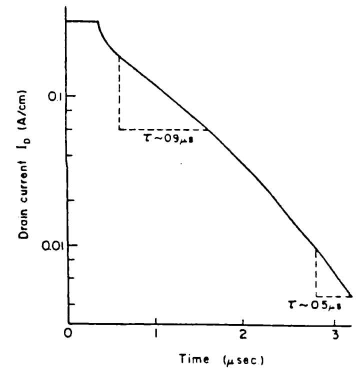

Fig.11 Hole current change

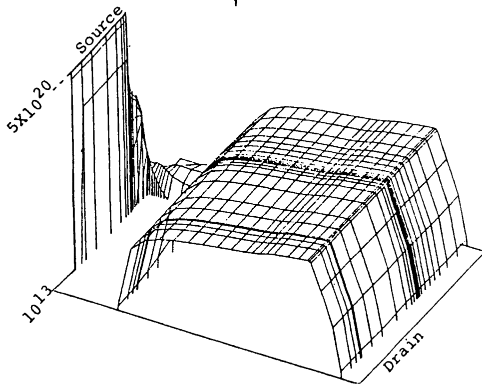

Fig.9 Electron density distribution for t=0.27μsec.

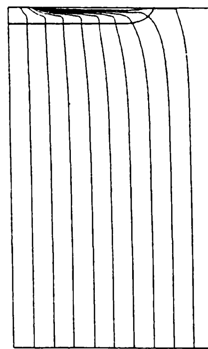

Fig.10 hole current flow line for t=0.36μsec.

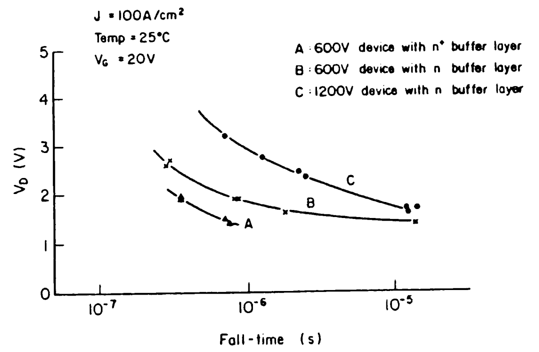

Fig.12 Trade-off curves for 600 and 1200V devices

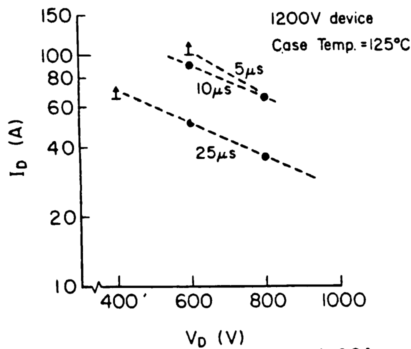

Fig.13(a) Measured forward SOA (125°C case temperature)

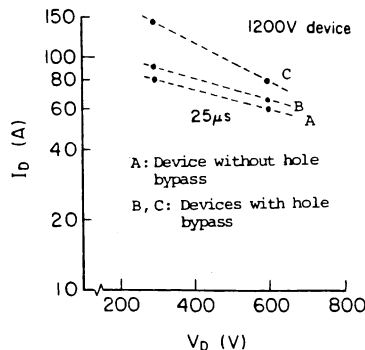

Fig.13(b) Hole bypass effects on SOA

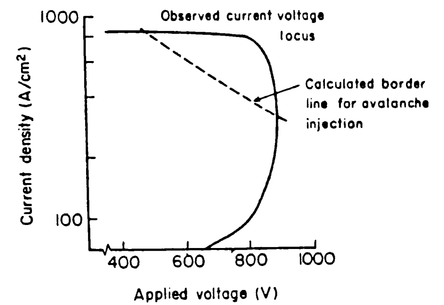

Fig.14 Calculated border for avalanche injection. Observed current-voltage locus is shown together.

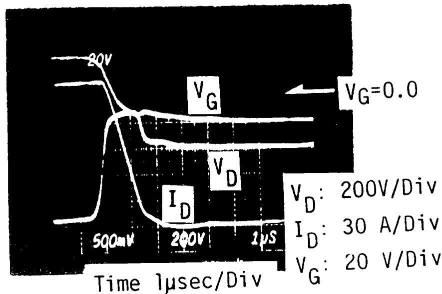

Fig.15 Turn-off waveforms corresponding to the locus shown in Fig.14.

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