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Bipolar MOS Power Device SimulatorTONADDEIIC Taking into Account External Circuit

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ABSTRACT

Device simulator family TONADDEII was revised to enable simulating MOS bipolar composite devices. An automatic mesh and input data generator MEDIT and a device breakdown voltage simulator TONADDEIIB have been developed and included as the simulator family. A newly implemented arbitrary external circuit defining function helps users to easily simulate switching characteristics, while retaining the rapid convergence feature.

1. Introduction

Device simulators are useful tools for device design and development. However, their application to high voltage and bipolar devices are limited, because a large CPU time is generally required to simulate these devices and because most of the simulators have been developed especially for VLSIs.

The device simulator family TONADDEII[1] have been developed as tools for power device development: (1)device structure optimization for a high breakdown voltage, (2)static and dynamic characteristics simulations for determining device trade-off relation, and (3)analysis of new devices such as bipolar MOS composite devices.

TONADDEII consists of (1)a pre-processor MEDIT[2]: an automatic mesh and input data generator, (2)TONADDEIIB[3]: a breakdown voltage simulator, TONADDEIIC: general purpose device simulator and (3) post-processor.

This paper introduces MEDIT and TONADDEIIC [4]. TONADDEIIB will be described in a separate paper in this proceedings. TONADDEIIC can deal with any two dimensional (bipolar, MOS and composite) devices with arbitrary external circuits, which are connected between the two device main terminals.

Through a simple interactive key-in procedure, MEDIT allows users to define diffusion layers, ion-implanted layers, silicon dioxides, air regions, gate- and base-electrodes and two main terminals for any desired device structures. MEDIT automatically generates a rectangular mesh and a complete set of imput data for TONADDEIIC.

In order to execute transient simulations, TONADDEIIC allows users to define any external circuits using passive components in addition to diodes and variable voltage sources. Thus, it is possible to accurately execute device switching-off simulations even with snubber circuits.

Since several application examples of TONADDEIIC have already been published[5], this paper emphasizes algorithms and solution methods adopted in TONADDEIIC and MEDIT.

2. Power Device Simulator TONADDEII

2.1 Convergence characteristics

Device simulators for high voltage power devices have to deal with (1) high voltage and high injection states, (2) large sized device structures and, consequently, large grid to grid distances, (3) S shaped device characteristics such as those for thyristors, as well as (4) MOS bipolar composite device structures.

TONADDEIIC has attained rapid and stable convergence characteristics even for high voltage and high injection states by adopting what we call 9 point discretization[1]. This makes it possible to include all the derivatives associated with the variables for adjacent 9 grid points in order to realize a complete Newton scheme(see Fig.1). It was confirmed for a number of devices that the inclusion of all the derivatives in the Jacobian matrix for the Newton scheme is effective to accelerate convergence. Convergence is always reached within 4 or 5 Newton iterations regardless of bias conditions[1].

Since each difference equation includes variables associated with the adjacent 9 grid points, the obtained Jacobian matrix has a larger number of non-zero elements as shown in Fig.1.

Imcomplete bi-conjugate gradient method(ILUBCG[6]) is mostly successfull and reliable for solving a large set of linearized equations with the Jacobian matrix shown in Fig.1. The direct solution method such as

Gaussian elimination is the best choice for ill-conditioned cases. A combination of decoupled method and conjugate gradient method(ILUBCG) is preferable for saving CPU time, when it works well.

TONADDEIIC takes into account higher order effects such as Auger recombination, bandgap narrowing, field dependent mobility etc. to attain better agreement with experiment results.

2.2 Bipolar MOS composite structure

For the MOS gate induced inversion layers, a channel mobility model has to be applied. A conventionally used channel mobility expression is, however, too complicated to include its derivatives in the Jacobian matrix. Thus, TONADDEII adopts an approximated channel mobilty model only for the channel region. In the thin inversion layer, it is reasonably assumed that channel current flows perpendicular to the electric field. This leads to the following simplified channel mobility μ_{ch} expression for the Yamaguchi model[7].

$$\mu_{ch}=\mu_0(|Ex|)(1+1.539\times10^{-5}|Ey|)^{-0.5},$$

where Ex and Ey are simply used instead of the two electric field components parallel and perpendicular to the current flow vector. Ordinary bulk mobility model is applied for the remaining regions.

This approximation only introduces less than 1% error for the total current, and makes it feasible to include all the derivatives in the Jacobian matrix, attaining rapid convergence.

If convergence is easily obtained and decoupled method well works, it is better to specify an option which apply conventional channel mobility model(Yamagichi model) to the entire device region.

3. Input data control and grid mesh generation by MEDIT

For ease in input data generation and programming, three integer arrays IB, IBH and ICHMOB were introduced in TONADDEIIC. IB is defined at each grid point and represents the type of electrodes. IBH represents the materials used for the rectangular spaces defined by the adjacent 4 grid points. ICHMOB is defined at four sides of the rectangular area and represents the type of mobility that should be adopted. IBH is defined even ouside the calculated device area, as is shown in Fig.2, and has a greater dimmension than that of IB by 1. Outside the device area, IBH is set to be 10(=N), representing the Neumann boundary condition.

Priorities are set among the three variables. IB has the highest priority and ICHMOB has the lowest. For example, ICHMOB has a meaning only where IBH is zero (for example, channel mobility is adopted only where the region is silicon). IBH has a meaning where IB is zero and, thus, the Neumann condition is cancelled where electrodes are defined. Figure 3 shows an IBH distribution for a certain device, where IB and ICHMOB are also shown in a merged fashion.

3.1 Interactive and graphic mesh editor: MEDIT

Typical input procedure in MEDIT is presented in this section.

(1)Structure data definition: Through interactive key-in procedure, users first define different meterial regions such as SiO_2, Air and Silicon on a CRT. These processes set IBH values. Then, they specify various electrode regions, determining IB values. Since IB is given highest priority, any IBH value is allowed if all the IB's for the 4 corners of the rectangular space are the same nonzero values. An epitaxial layer, diffusion layers, and ion implanted regions are, then, defined.

(2)Auto mesh generation: After structure data definition, MEDIT automatically generates a grid mesh. MEDIT generates mesh lines so that impurity density differences between two grid points become less than three times, unless the distances become less than the user specified minimum grid distances. Users have to specify critical lines so that MEDIT checks impurity density change along the defined critical lines.

(3)Mesh line modification: Users can check not only the generated mesh on the CRT but also the impurity profiles along any mesh lines. Users can delete any mesh line unless it coincides with one of the defined material boundaries, or can add new mesh lines as desired(Fig.4).

(4) Finally, users can define the regions, where different mobility models such as channel mobility are adopted, setting ICHMOB values.

Generated input data are automatically transfered to TONADDEIIB or C.

4. Transient simulation including external circuit.

TONADDEIIC can simulate transient device characteristics with an arbitrary external circuit connected between the two main terminals. The adopted solution algorithm is shown in Fig.5, where external circuit equations are solved by a decoupled method.

The voltage Vap^m applied to the device is corrected in the following way. The external circuit equation to be solved for a certain time step is given as:

$$f(Vap^m+\delta V^m,\ Id^m+\delta I^m)=0,$$

where Vap^m and Id^m are m-th device voltage and device current calculated by TONADDEII.

The unknown corrections δV^m δI^m can be obtained by assuming the following relation:

$$\delta V^m/\delta I^m=(Vap^m-Vap^{m-1})/(Id^m-Id^{m-1})$$

Then, device current Id^{m+1} is to be obtained by TONADDEII for the (m+1)-th device voltage $Vap^{m+1}(=Vap^m+\delta V^m)$. These iterations are continued for the same time step until correction δV^m becomes sufficiently small.

Figure 6 shows typical convergence characteristics, when external circuits are solved simultaneously. Convergence is always reached within 10 Newton cycles although external circuit equations are solved in a decoupled manner. A combination of 9 point discretization and a coupled method is a key to reducing the number of Newton iteration cycles for time dependent solutions.

5. Application example: Latch-up phenomena in vertical IGBTs.

Latch-up phenomena in IGBTs is presented as an application example. Dynamic current voltage characteristics were calculated, by increasing the electric source voltage, which was directly connected to the device (see Fig.7(A)), at the rate of 400V/μsec. Figure 8 shows a calculated dynamic current voltage curve, where latch-up phenomena is clearly seen.

Figures 9 to 11 show electron density distributions, describing the initiation of electron injection into the P-base when latch-up occurs. Thyristor action occurs for a half of the N+ source layer.

Current-voltage characteristics having even negative resistances can well be simulated by inserting a resistance between the voltage source and the treated device, as is shown in the circuit shown in Fig.7(B).

6. Summary

Device simulator family TONADDEII have been developed for power device design and analysis. TONADDEIIC simulates time dependent device characteristics, including external circuits. An algorithm for rapid solution as well as an application example were presented.

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[7]K.Yamaguchi, IEEE Trans. Electron Devices, ED-26,p.1068(1979)

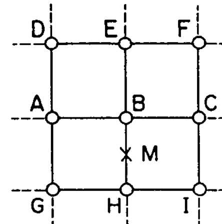
APPENDIX

For example, the circuit shown in Fig.12 is defined in the following way.

```
ARROW 999  3  E   200       0.64555
ARROW   3  2  R   305.1644  0.64555
ARROW   2  1  L   1.0E-3    0.64555
ARROW   1 999 D   1.0E-8    1.0E-8
ARROW   1 999 S   1.0       0.64555
INIT    1  3.0
INIT    2  3.0
INIT    3  200.0
```

ARROW statements define two node numbers, type of the device which is connected between the two nodes (time dependent variable voltage source E , resistance R , inductance L , capacitance C , diode D , and the device treated by TONADDE S , etc), characteristic values for the device (voltage, resistance, inductance, capacitance diode saturation current, ratio of actual device area over calculated device area) and the current flowing in the device for initail time step t=0.

INIT statements define a node and its voltage for the initial time step t=0. Voltage changes for the gate terminal, voltage source etc. can be defined by optional statements.



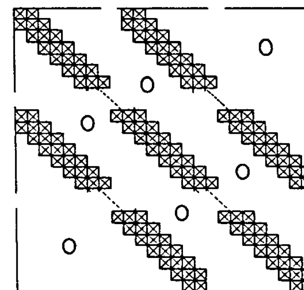


Fig.1 Jacobian matrix for Newton iteration including all the derivatives associated with adjacent 9 grid points.

Fig.2 IB and IBH values are defined for individual grid points and rectangular spaces, respectively. IBH values are defined outside the device region for the rectangular spaces shown by dotted lines.

Fig.3 IBH value examples for an actual device. IBH values are replaced by corresponding IB values, if all the IB values for the 4 corner grid points are the same number other than zero. Similarly, ICHMOB values are shown instead of IBH values, if defined ICHMOB values are effective.

Fig.5 Flow chart for time-dependent solution.

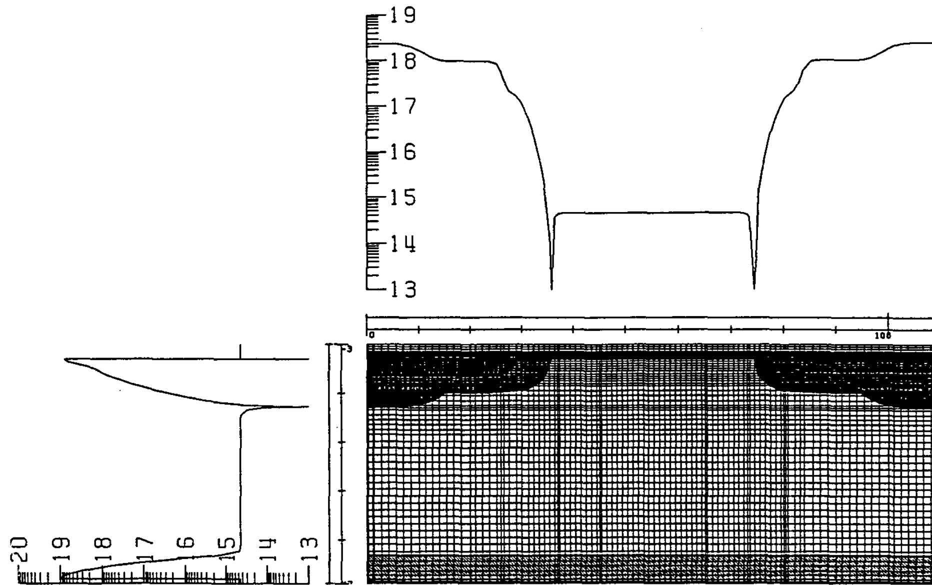


Fig.4 An example picture on CRT generated by MEDIT.

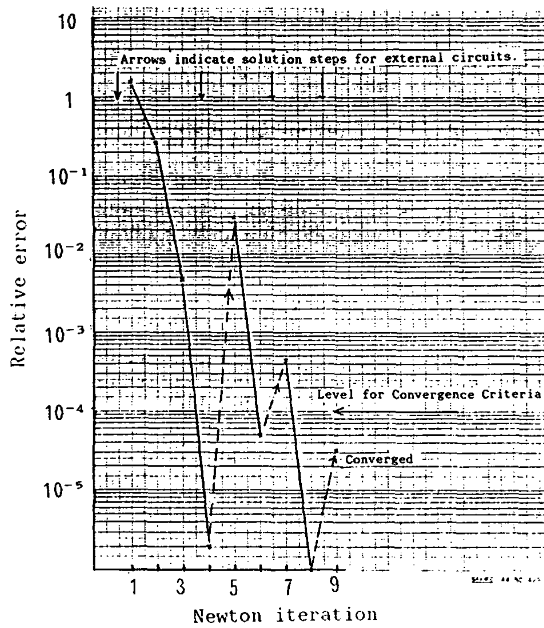


Fig.6 Typical convergence characteristics for time dependent solution including an external circuit

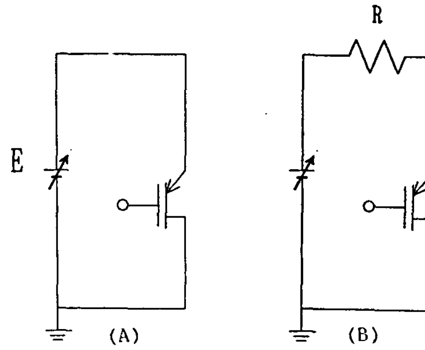


Fig.7 Circuits for dynamic current voltage curve calculation.

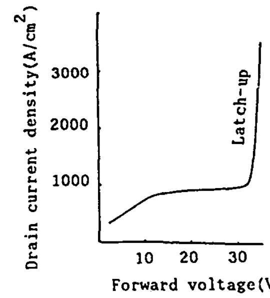


Fig.8 Current voltage relation, where drain voltage was raised at the rate of 400V/μs.

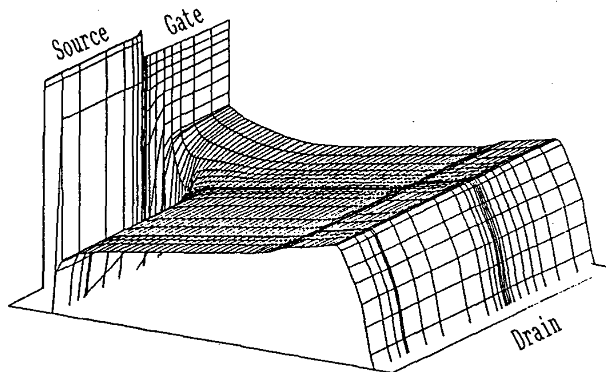


Fig.9 Electron Density Distribution(V=4.0V)

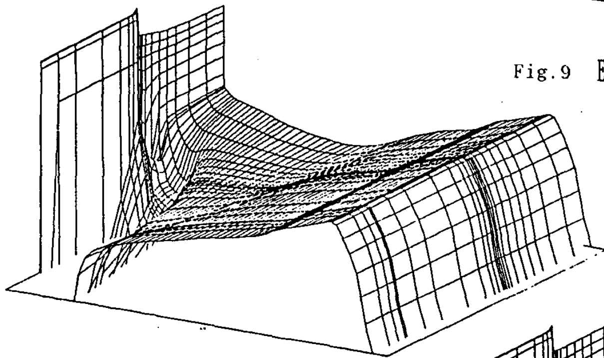


Fig.10 Electron Density Distribution(V=32.6V)
:Just before latch-up

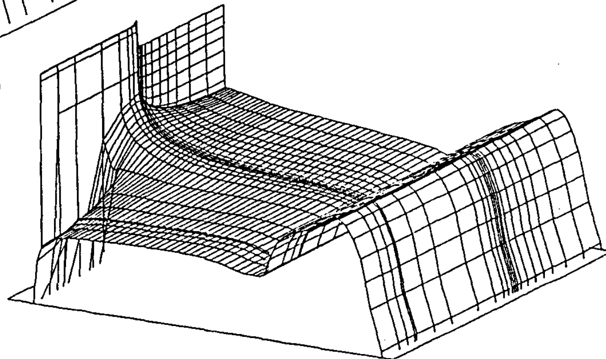


Fig.11 Electron Density Distribution(V=39.4):Latched-up

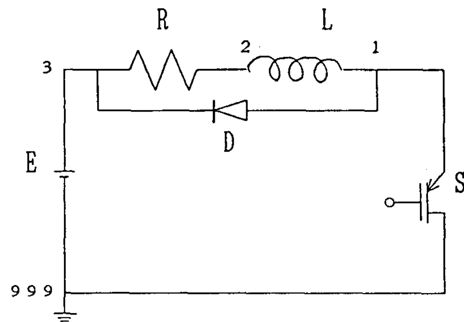


Fig.12 Example circuit.