Design Optimization of 500V 1A SOI 1 Chip Inverter ICs

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Abstract:

The present paper reports development of 3rd generation 500V 1A SOI single chip inverter ICs. Important issues for the present ICs are chip cost reduction and long-term reliability of high voltage junctions, where 500V interconnection layers exist over the junctions. Reliable high voltage capability was realized by optimized multi-ring resistive field plates.

The same low cost process, developed for 250V SOI power ICs, was adopted, and only 30V CMOS devices were utilized for logic, analog control and protection circuits without bipolar transistors. This greatly simplifed the fabrication processes, and increased the reliability of the circuits under high dV/dt driving conditions.

1. Introduction

First, we briefly review Toshiba's development history of 500V single chip inverter ICs. The chip photos are shown in Fig.1. The first 500V 1A chip was developed in 1991, using the sophisticated 50um thick SOI layer[1]. Each high voltage device was dielectrically isolated by deep V grooves as shown in Fig.2. Low voltage control circuits were formed in a single isolated island and each low voltage device was isolated by conventional junction isolation within the island. Since the fabrication process included wafer bonding, epitaxial growth, V groove etching and poly-silicon filing etc., it was complicated and not cost efficient.

In 1990, we proposed, for the first time, the high voltage SOI device structure of Fig.3 [2], using trench isolation and a thick buried oxide film. Deep trenches realize dense high voltage device integration with BiCMOS circuits. When a high voltage is applied to the high voltage device, the buried oxide itself supports a large part of the voltage[2,3]. The buried oxide serves as a part of the high voltage device and the structure is widely recognized as SOI Resurf.

In 1994, we successfully developed 500V 1A single chip inverter ICs based on 1.5um BiCMOS technology[4]. At that time, we assumed that the system integration would be the main stream, and that even CPUs would be integrated in high voltage power IC chips in the next generation. High voltage lateral devices were fabricated based on 1.5um CMOS process. We once abandoned diffusion self-alignment DMOS process at that time and adopted fully CMOS compatible process for the high voltage MOSFETs.

Recently, however, we have realized that the cost optimization is the first priority and that the high level functionality can be located outside the chip, if 5V logic level interface is provided.

In view of these situations, we have re-developed new simplified low cost SOI power IC families by adopting 30V CMOS analog control circuits. The fabrication processes have been greatly simplified by excluding bipolar transistors.

In the last PCIM China 2001, we reported 250V 1A 1 chip inverter ICs. In the present paper, we report the new issues and design optimizations for 500V 1A inverter ICs.

2. High Voltage SOI Lateral IGBT

IGBTs are suitable for high voltage large current output devices. Switching speed of power devices is conventionally controlled by introduction of lifetime killer. However, lifetime control process is not compatible with conventional CMOS process. There are several methods to control the switching speed of power devices. One is to use thin SOI layers. The switching speed of IGBTs improves as the SOI thickness decreases[5] because the carrier lifetime is effectively decreased by the large surface recombination velocity at the silicon

dioxide interface[5]. Another is to reduce emitter efficiency of the p+ drain or collector. The effective method is a low dose p-emitter[6].

For 250V devices, SOI thickness is relatively thin and the effective lifetime of the SOI layer is sufficiently small to achieve 150nsec fall time.

However, for 500V devices, achieving a high switching speed is a more difficult challenge since thick SOI layers such as 15um is required and the effective lifetime is large[7].

Figure 4 shows a cross section of our 500V large current lateral IGBTs. The p-emitter injection efficiency is carefully controlled by the low dose p-emitter.

It is extremely important to reduce on-resistance of LIGBTs in order to shrink the chip size. This is because output devices occupy most of the chip area and the cost of the power ICs deeply depends on the size of the power devices.

The improvement has been made possible by adopting a multi-channel structure[8] as shown in Figs.4 and 5. Simply adding more channels in the lateral direction does not necessarily improve the on-resistance because the distance between the added channel and the drain becomes larger. The electron current from the added channel must go through the two JFET regions. First JFET is formed by the two adjacent p-wells. The first p-well and the buried oxide constitute the 2nd JFET. For example, electron current, injected from the added 2nd poly-gate channel in Fig.4, must go through the n-layer underneath the first p-well. The situation can be improved by reducing the width and the depth of the p-well. Thus, finer design rule is required for this purpose.

In 1999, we developed 500V 3A inverter IC chip using i-line lithography[9]. The achieved current density of the developed multi-channel LIGBT for the chip was 175A/cm2 for 3V forward voltage.

For the present low cost version, we adopted g-line lithography for cost reduction. The same multi-channel structure is still effective.

3. High Voltage Structure and Interconnection

One of the important issues for the high voltage ICs is high voltage interconnection. Improper interconnection metal layers degrade the breakdown voltage of high voltage devices. SIPOS layers are often used as electric field shielding layer. In the 1st generation inverter ICs, we adopted the SIPOS resistive field plates (RFP) to shield the influence of the interconnection layer and to realize a high breakdown voltage[10].

In 1994 ISPSD, we proposed "scroll poly-silicon resistive field plate (SRFP)" in order to replace the expensive SIPOS layer[4]. The present paper reports further optimization of the concept. We propose and experimentally evaluate "multi-ring RFP structure". The results are compared with "scroll RFP".

The figures 6 and 7 show schematic illustrations of the multi-ring poly-silicon RFPs. The each ring of the multi-ring RFP is electrically connected to the adjacent rings in the two opposite points. The two ends are electrically connected to the gate and the drain electrodes. A small current flows in the high resistance poly-silicon and creates a linear potential gradient. This effectively shields the influence of the interconnection layer.

The multi-ring RFP has a merit that it is easy to draw an actual mask design and to control the amount of current flow, which results in the leakage current. The number of the connected bridges between the rings determines the amount of the leakage current.

It was found that the breakdown voltage is a function of the drift region length and the thickness of the interlayer oxide film under the high voltage interconnection layer, as shown in Fig.8. The breakdown voltage strongly depends on the thickness of the interlayer oxide under the interconnection metal layer if the drift layer length is below 53um.

It was also found that one of the important parameters is the opening width between the two poly-silicon rings, W, which is illustrated in the Fig.6. Figure 9 shows that reducing the opening width effectively enhances the breakdown voltage. This is because that the influence of the interconnection layer is more effectively shielded by the reduction in the opening width.

Optimum design of the RFP ensures stable 500V breakdown voltage even for the relatively thin interlayer oxide film of 3.7um. Conventionally, thicker interlayer oxide film of more than 4.5um has been required for 500V breakdown voltage.

It should be noted that the breakdown voltage has a time dependent feature if high resistivity p-type wafers are used as substrates. Figure 10 shows an example. A high breakdown voltage exceeding 800V is initially seen for an instant when a high voltage is first applied to the device. However, the breakdown voltage quickly reduces to the original value after a certain time period, which depends on the various conditions. We assume that a depletion layer develops initially under the buried layer and that a high breakdown voltage is observed until an inversion layer replaces the depletion layer by generated

electron and hole pairs (see Fig.11).

4. Process Optimization for 500V 1A Inverter IC Chip

This section reports development of low cost 500V 1A 3-phase 1 chip inverter ICs. The chip includes only five kinds of devices: n-ch LIGBTs, Diodes, 30V CMOS, and HVNMOS. Thus, the fabrication process was greatly simplified.

Elimination of bipolar transistors in the control circuits greatly increased the system reliability, because bipolar transistors ofen caused malfunction of the circuits. The details were reported in our last paper in PCIM China 2002.

Figures 12 and 13 show I-V curves and the switching waveforms of 0.5A drain current at room temperature. Forward voltage drop is 2.0V for 0.5 amperes of the drain current. The fall-time is 400nsec.

Table 1 shows the electrical characteristics of NMOS ,PMOS and FWD

Figure.14 shows a block diagram of the fabricated inverter ICs. The bootstrapping technique is adopted as the internal high side voltage source. The circuits include drive circuits for LIGBTs, bootstrap diode, logic circuits, PWM circuit and various protection circuits. The protection circuits include under-voltage, over-current and over- temperature protections.

Figure.1 shows a developed 500V 1A single chip inverter IC. The chip size is $4.1 \times 6.6mm^2$.

High efficiency and cost effective sinusoidal wave drive of DC motors is also made possible by combining the developed ICs with an ASIC "TB6539" without using MCP or DSP.

5. Conclusion

We have successfully developed highly reliable low cost 3rd generation 500V 1A three-phase single chip inverter ICs for DC brushless motor control.

New high voltage structure, multi-ring RFP is successfully implemented to ensure high voltage reliability of the power ICs.

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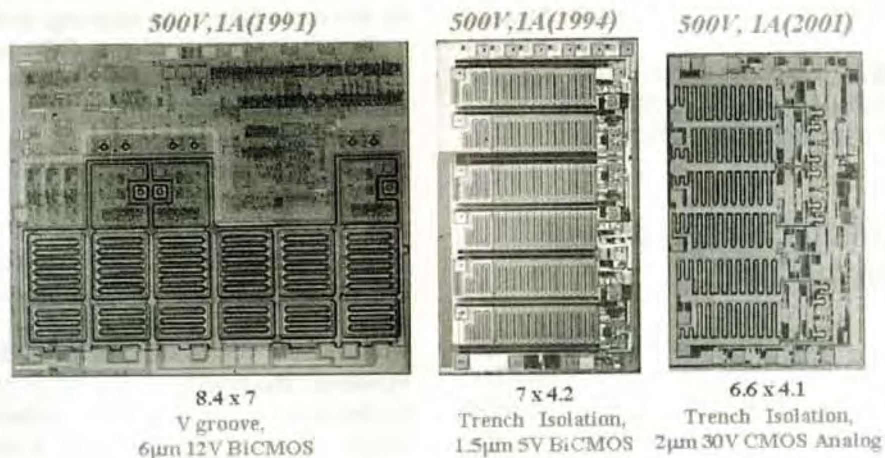


Fig.1 Evolution of 500V 1A 1 chip Inverter ICs

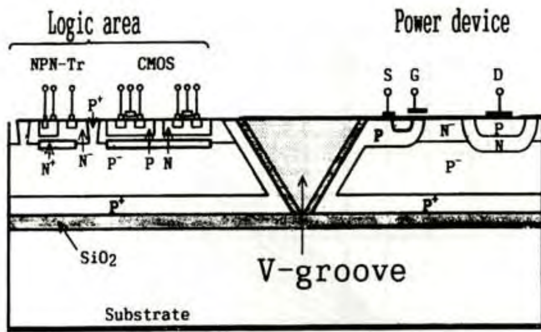


Fig.2 Basic structure of 1st generation SOI power IC

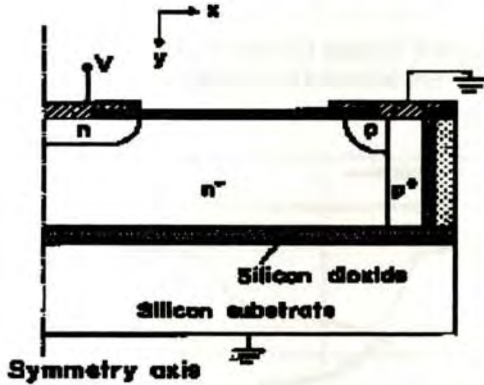


Fig.3 First High voltage SOI structure in 1990.

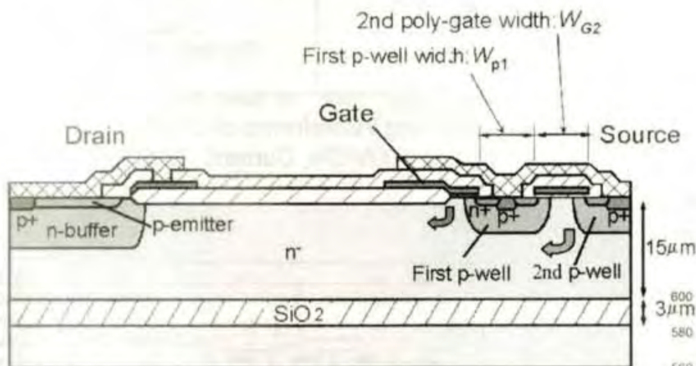


Fig.4 Multi-channel Lateral IGBT

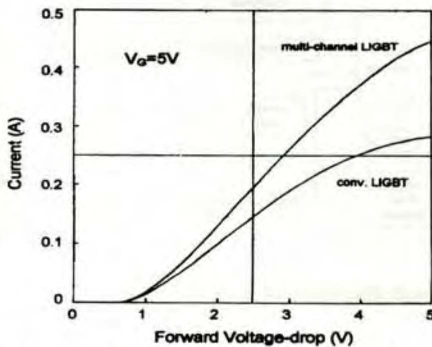
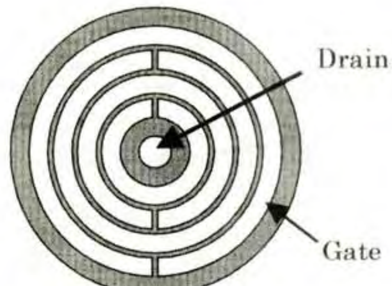


Fig.5 Comparison of I-V curves between multi-channel LIGBTs and conv. LIGBT



(a) Multi-Ring RFP

(b) Scroll RFP

Fig.6 Plane view of Multi-Ring Resistive Field Plate(RFP) and Scroll RFP

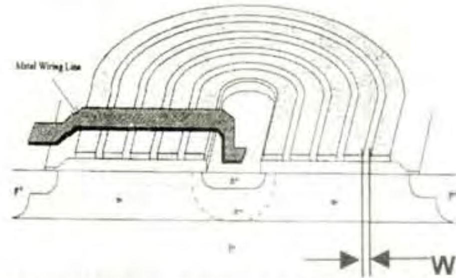


Fig.7 Bird's eye view of Multi-Ring RFP. Opening width , W, is defined in the figure.

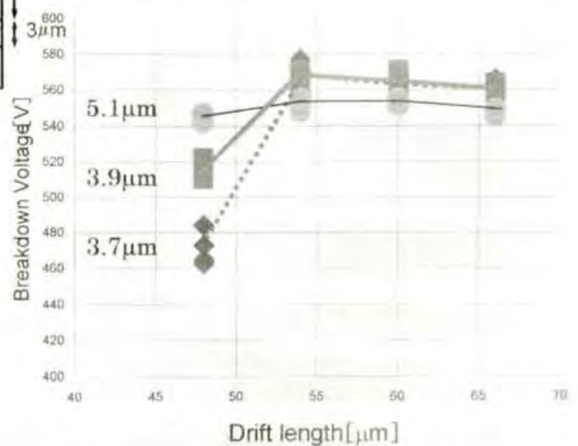


Fig.8 Breakdown voltage as a function of drift layer length with interlayer oxide thickness as a parameter.

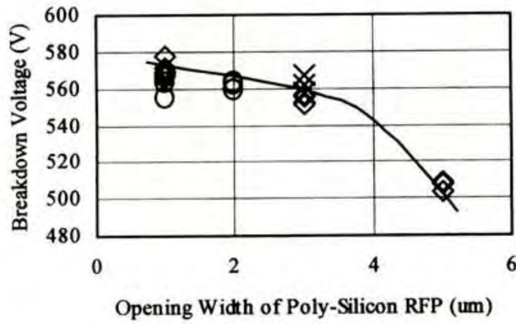


Fig.9 Breakdown voltage dependence on opening width of RFP.

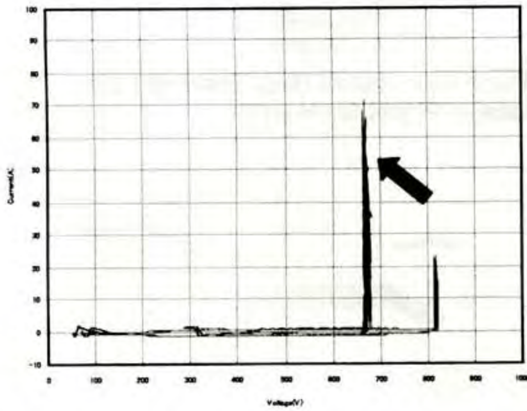


Fig.10 Breakdown voltage drifted if high resistivity p-type wafer was used as substrate. A high breakdown voltage over 800V was initially seen. It quickly reduced to the original value.

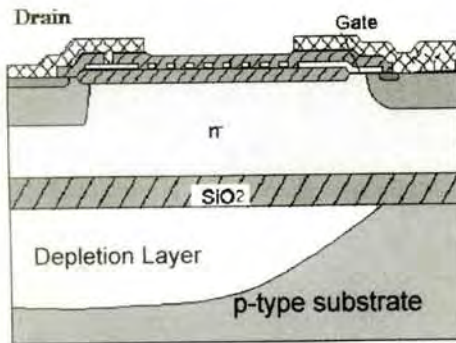


Fig.11 Depletion layer initially develops in the p-type substrate, enhancing the breakdown voltage for an instant.

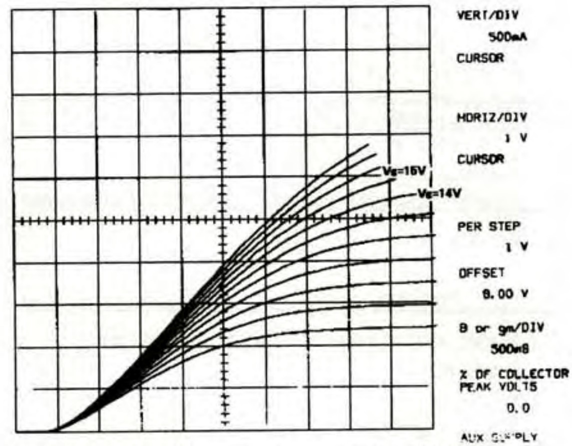


Fig.12 Current Voltage Curves of 500V LIGBT (Current:500mA/Div, Voltage: 1V/Div)

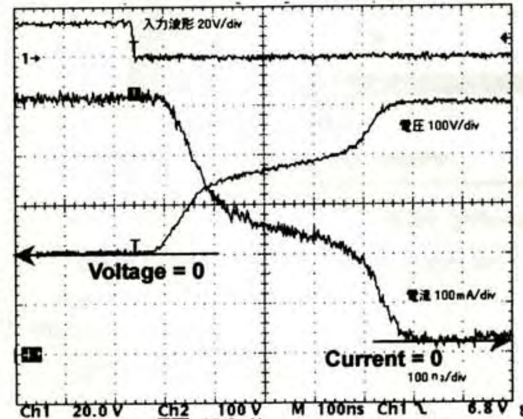


Fig.13 Switching Waveforms of LIGBT (Voltage: 100V/Div, Current: 100mA/Div)

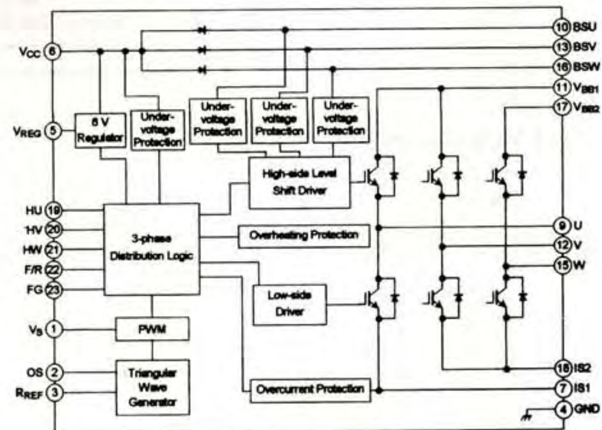


Fig.14 Circuit diagram of 1 chip inverter ICs.