Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp. 120-121

25V - 13 m$\Omega\cdot$mm^2 Low On-Resistance Novel Structure Trench Gate LDMOS

Yusuke Kawaguchi, Takeshi Sano[1] and Akio Nakagawa

Advanced Discrete Semiconductor Technology Laboratory, Toshiba Corporation
[1]Microelectronics Center, Toshiba Corporation Semiconductor Company
1, Komukai Toshiba-cho, Saiwai-ku, Kawasaki 210, Japan
Phone: 044-549-2139, Fax: 044-520-1501
E-mail: yusuke.kawaguchi@toshiba.co.jp

1. Introduction

Many studies of low on-resistance 20 V range MOSFETs have been conducted because these devices have a variety of applications in computer peripherals. It was recently reported that a 25 V LDMOS achieved a specific on-resistance as low as 18 m$\Omega\cdot$mm^2 [1] by optimizing cell structure using fine design rule.

In this paper, we propose, for the first time, a novel lateral trench gate MOSFET, which utilizes narrow and shallow multiple trenches as channel regions as shown in Fig.1. Conventionally, trench gate structures have been used for vertical trench MOSFETs, where channel current flows vertically on the trench side walls. The unique feature of the lateral trench gate MOSFETs is that the electron current spreads into the channel regions induced both on the trench terrace and on the trench side walls, and that the channel current flows laterally on the trench side walls from the source to the drain. The n-diffusion layer reaches the bottom of the trenches so that the electron channel current, flowing widely spread in the trench side walls, is effectively collected by the n-layer, reducing channel resistance.

The proposed device was fabricated using the standard 0.6μm CMOS process and an additional trench gate formation process. The developed device achieved 13m$\Omega\cdot$mm^2 on-resistance with the breakdown voltage of 25V, which is the record low on-resistance among the previous works, and is even lower than that of the vertical trench MOSFETs.

2. Device structures and process design

Figure 1 shows a top view the proposed trench gate LDMOS and fig. 2 (a), (b) shows cross-sectional views of line A-A' and B-B' in fig. 1 respectively. A number of fine trenches were formed, running from the source to the drain n-layer.

The width, space and depth of the trenches are 0.4 μm, 0.4μm and 1.0μm, respectively. Since the terrace and the side walls of the trenches works as channels, the effective gate width is 3.5 times as wide as that of the conventional planer LDMOS. It is important to reduce the spreading resistance from the source to the channel. The trench gate must overlap sufficiently with the source n+ diffusion.

Calculations were carried out using 3D device simulator dessis-3D in order to optimized device parameters. The overlapped length of the trench and the source n+ layer (L in fig. 2 (c)) were optimized in order to reduce the spreading resistance and to realize uniform electron current flow in the trench side wall.

Figure 3 shows the calculated dependence of breakdown voltage on the dose of drift region. It was predicted that the proposed trench gate LDMOS achieves 10 m$\Omega\cdot$mm^2 specific on-resistance for the breakdown voltage of more than 20 V. This is about a half of that of conventional planer LDMOS.

Figure 4 shows the SEM photograph of fabricated device which correspond to the cross-section of fig. 2 (b). This photograph shows that the fine trenches are formed and filled up with gate polysilicon.

3. Experimental results

Figure 5 shows the reverse blocking characteristics and fig. 6 shows the V-I characteristics of proposed trench gate LDMOS. The measured breakdown voltage is 25 V and specific on-resistance is 13 m$\Omega\cdot$mm^2 at V_{gs} = 5 V. Figure 7 compares the measured and calculated specific on-resistance of proposed device with previously publish data. The developed device shows the record low on-resistance among the previous works. However, the measured value of the on-resistance is not so low as the calculated value. This is assumed that the channel mobility of trench side wall is lower than that of planer devices because of the surface roughness. It was reported [2, 3] that the surface roughness of trench side wall greatly influence the channel mobility. The on-resistance will be further reduced by optimization of the smoothing process of trench side walls.

The developed LDMOS also has a sufficiently large current turn-off capability of 8.6×10^3 A/cm^2.

4. Conclusion

We have presented a 20V range low on-resistance novel structure trench gate LDMOS. The proposed device can be fabricated using standard CMOS process and additional trench formation process. The proposed device achieves 13m$\Omega\cdot$mm^2 of on-resistance when the breakdown voltage was 25V and this value is the best performance among the previous work. The on-resistance will be further reduced by optimization of the smoothing process of trench side walls.

Acknowledgments

The authors would like to thank Dr. Yujiro Naruse for supporting this research.

References

1) V. Parthasarathy, R. Zhu, W. Peterson, M. Zunino and R. Baird: 1998 ISPSD, pp.61-64.
2) A. Yahata, S. Urano, and T. Inoue: Jpn. J. Appl. Phys. 36 (1997) p. 6722.
3) A. Yahata, S. Urano, T. Inoue and T. Shinohe: Jpn. J. Appl. Phys. 37 (1998) pp.3954-3955.

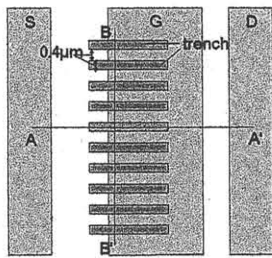

Fig. 1 Top view of the proposed trench gate LDMOS. Trench gate is arrayed at right angles with device pitch. The width and space of trench gate is 0.4 µm

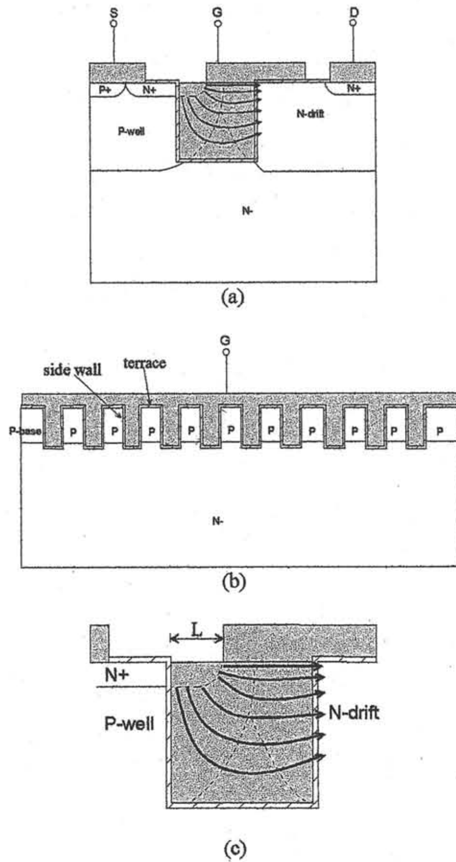

Fig. 2 (a) Cross sectional view of proposed trench gate LDMOS in line A-A', (b) line B-B' in fig. 1.and (c) magnified view of the channel region in fig. 2 (a). The depth of trench gate is 1.0 µm. The electron channel current flows laterally on the trench side walls from the source to the drain.

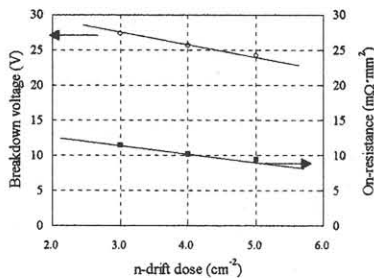

Fig. 3 Calculated dependence of breakdown voltage and on-resistance on the dose of drift region. It was predicted that the proposed trench gate LDMOS achieves 10 $m\Omega{\cdot}mm^2$ specific on-resistance for the breakdown voltage of more than 20 V.

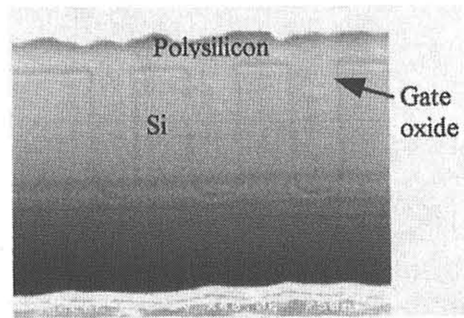

Fig. 4 SEM photograph of fabricated trench gate LDMOS. The fine trenches are formed and filled up with gate polysilicon electrode

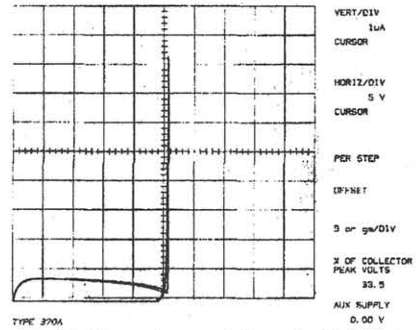

Fig. 5 Reverse blocking characteristics of fabricated trench gate LDMOS.

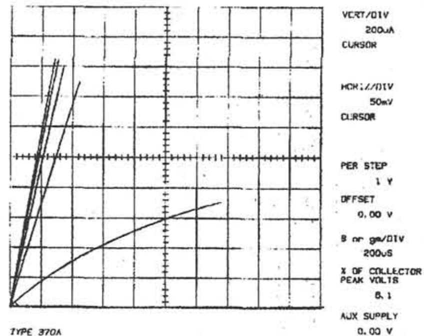

Fig. 6 V-I characteristics of fabricated trench gate LDMOS .

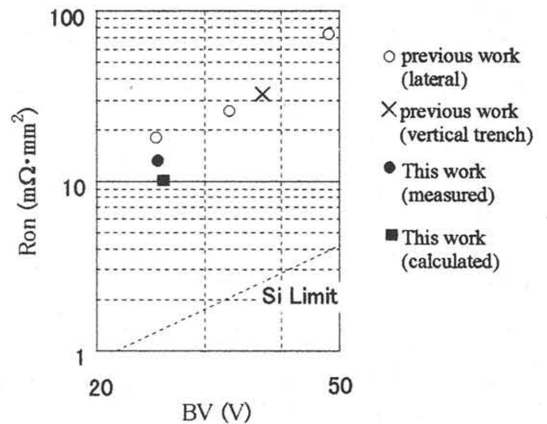

Fig. 7 Comparison of on-resistance and breakdown voltage for this work and previously publish data. The developed device shows the record low on-resistance among the previous works, and is even lower than that of the vertical trench MOSFET. The on-resistance will be further reduced by optimization of the smoothing process of trench side walls.