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0.8 μm CMOS Process Compatible 60 V–100 mΩ·mm^2 Power MOSFET on Bonded SOI

Yusuke KAWAGUCHI, Yoshihiro YAMAGUCHI, Hideyuki FUNAKI, Yoshinori TERAZAKI and Akio NAKAGAWA

Materials and Devices Research Laboratories, Toshiba Corporation, 1, Komukai Toshiba-cho, Saiwai-ku, Kawasaki 210, Japan

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In the present paper, we propose high voltage lateral power metal-oxide-semiconductor field effect transistor (MOSFET) on silicon on insulator (SOI), using the pure 0.8 μm complementary metal-oxide-semiconductor (CMOS) processes without diffusion self-alignment. The measured specific on-resistance of the developed lateral power n-channel MOSFET (NMOSFET) was 100 mΩ·mm^2 and breakdown voltage was 60 V. The fabricated device attains its on-resistance comparable to that of diffusion self-align MOSFET (DMOSFET). It also achieves high side switch operation by a reasonable cost, and can be integrated with Bipolar CMOS (BiCMOS) circuits and micro processing unit (MPU). Compatibility of the developed MOSFET to these low voltage circuits are demonstrated. Furthermore, we show that the MPUs and BiCMOS analog circuit on SOI is suitable for high temperature operation.

KEYWORDS: high voltage MOSFET, bonded SOI, low on-resistance, CMOS process compatible, power IC, dielectric isolation

1. Introduction

The SOI technology has been of great interest because it makes it possible for high voltage devices to be integrated on the same chip together with BiCMOS circuitry by simply using shallow trench isolation. It has the further advantages of high-speed and high-temperature operation. The authors have already reported that high voltage lateral IGBTs fabricated on 1.5 μm thick SOI operated at 200°C at a frequency of 20 kHz.[1,2] The SOI solution is now practical because the price of bonded SOI wafers with thicker silicon layers has become almost the same as that of epi-wafers with n$^+$ buried layers.

Many studies of 60 V range low on-resistance MOSFET have been made for a variety of applications such as automotive systems and computer peripherals. It was recently reported[3] that lateral DMOSFET achieves lower on-resistance than that of vertical DMOSFETs, if they are fabricated by using a fine design rule. Since it is both expensive and difficult to integrate vertical DMOSFET with BiCMOS circuits, simple integration of lateral power MOSFET and BiCMOS circuits is a reasonable solution even for large current power ICs. One of the problems is that low on resistance lateral DMOSFET demonstrated so far on p-type substrate cannot be used as a high side switch.

The DMOS structure has conventionally been adopted for power devices because a short channel length and low on-resistance is easily attained with high breakdown voltage, although it requires an additional p-base diffusion process.

In the present paper, we propose high voltage lateral power NMOSFETs on SOI, using the pure CMOS processes without diffusion self-alignment. The developed lateral power NMOSFET achieves on-resistance comparable to that of DMOSFET, high side switch operation by a reasonable cost, and can be integrated with BiCMOS circuits and MPUs. In addition, we demonstrate the operation of a 4 bit MPU and BiCMOS analog circuits fabricated by the same 0.8 μm BiCMOS process on the SOI wafer. Furthermore It is shown that these circuits on SOI is suitable for high temperature operation.

2. Device Design and Structure

Figure 1 shows the cross-sectional view of the high voltage NMOSFET on 5 μm thick p-type SOI substrate. This structure was designed and implemented into 0.8 μm rule BiCMOS process (the shortest gate length of CMOS is 0.8 μm). The gate length, n-drift length, gate oxide thickness of the fabricated high voltage NMOSFET are 2.2 μm, 3.0 μm, 15 nm, respectively. Figure 2 shows the fabrication flow of this process. The p-body region was formed by CMOS p-well. The n-drift layer was formed using the same thermal process for the CMOS n- and p-well. The gate oxide was formed using by the same oxidation process. Therefore, no additional thermal processes are required. Since the channel region is formed not by DSA (diffusion self-align) but by the same processes as low voltage NMOSFETs, the channel length depends on the accuracy of mask alignment.

Taking advantage of the SOI structure, the n-drift layer resistance can be minimized by choosing an opti-

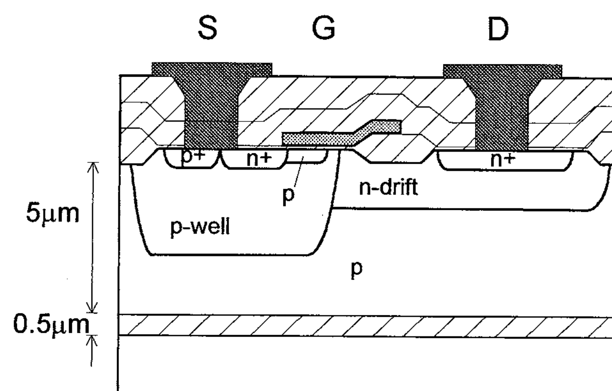


Fig. 1. Cross-sectional view of the developed 60 V NMOSFET. When this device is used for high side switch, the hole accumulation layer is induced on the buried oxide, shielding the influence of the source to substrate bias.

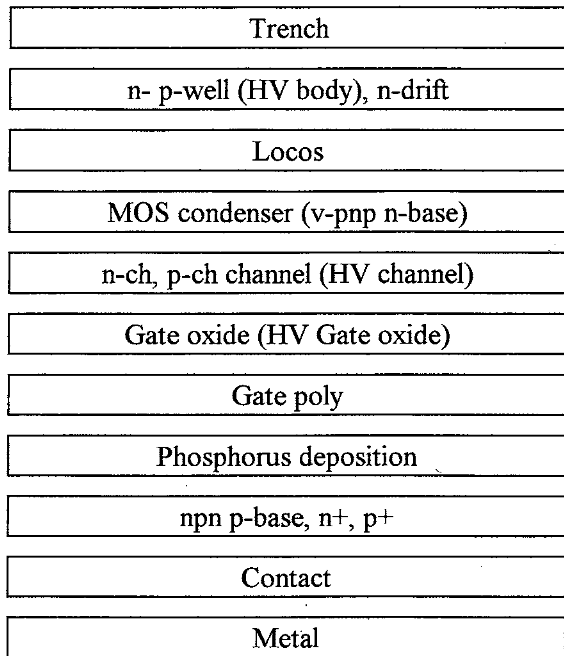


Fig. 2. Process flow of the developed high voltage NMOSFET. Only one additional mask (for n-drift layer) and no additional thermal processes are required to the conventional 0.8 μm BiCMOS process.

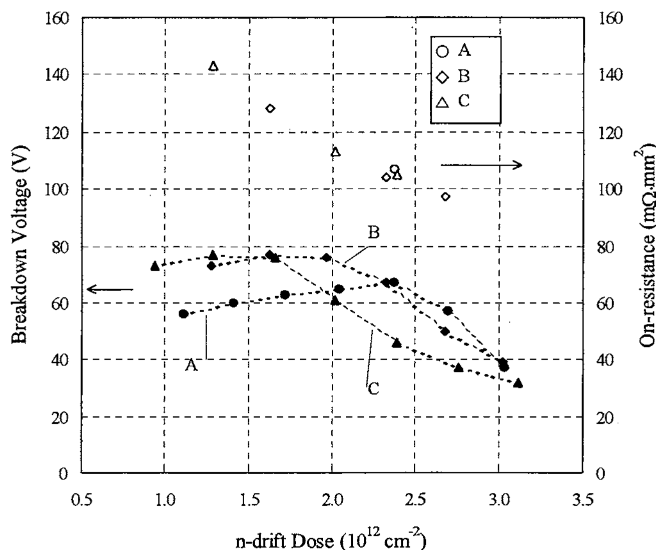


Fig. 3. Dependence of calculated on-resistance and breakdown voltage on the impurity dose of n-drift layer for three cases of p type silicon layer concentration (A-C). The value of p-type silicon layer concentration of B is 25% of A, that of C is 10% of A.

mum p layer doping on the buried oxide. The optimization parameters are the p-type silicon layer impurity concentration, the n-drift layer impurity dose, length, and depth. Shallower n-drift layer, carrier mobility are decreased by impurities scattering, and deeper, the current path length in n-drift layer is increased.

Figure 3 shows calculated on-resistance and breakdown voltage dependence on the impurity dose of n-drift layer for three cases of p type silicon layer concentration. The value of p-type silicon layer concentration B is 25% of A, that of C is 10% of A. It was found that p type silicon layer impurity concentration is an important parameter for a lower drift layer resistance.

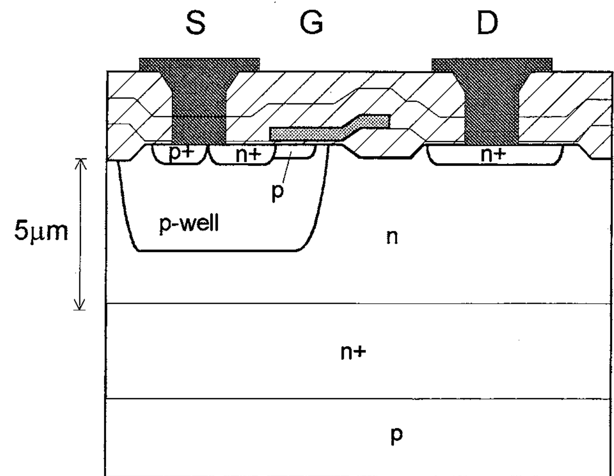


Fig. 4. Cross-sectional view of an NMOSFET using n-epi wafer with n^+ layer. The best calculated on-resistance value for this structure was 157 mΩ·mm^2 and breakdown voltage was 65 V.

Conventionally, DMOSFET have been fabricated on n-epi/n^+ buried layer. The on-resistance and breakdown voltage were also calculated and optimized for the structure shown in Fig. 4. The best calculated on-resistance value was 157 mΩ·mm^2 and breakdown voltage was 65 V. Since n-layer dose of this structure is lower than that of SOI devices in order to achieve the same breakdown voltage, its on-resistance is larger than that of NMOSFET on p-layer.

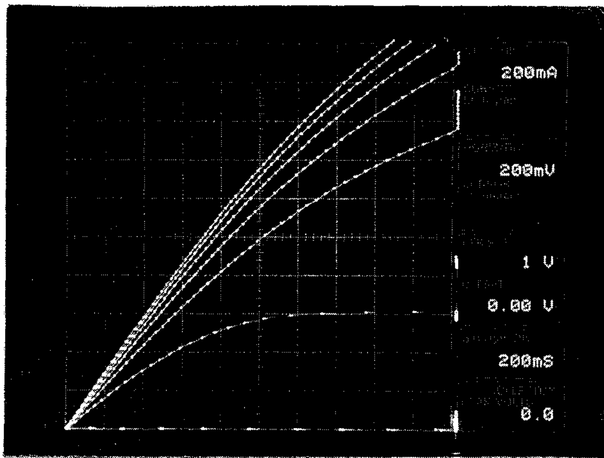
3. Results and Discussion

3.1 *On-resistance and breakdown voltage*

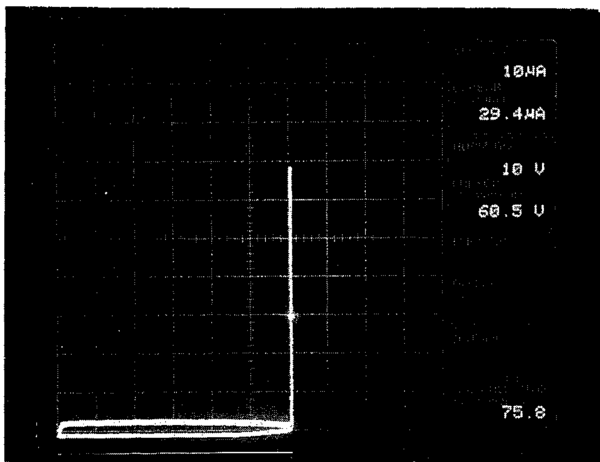
The experimentally obtained current-voltage curves and forward blocking characteristics for n-drift dose of 2.3×10^{12} cm^{-2} are shown in Fig. 5. The measured breakdown voltage is 60 V and specific on-resistance is 100 mΩ·mm^2 at $V_{gs} = 5$ V. Figure 6 shows experimentally obtained on-resistance and breakdown voltage dependence on the impurity dose of n-drift layer, and, these values show good agreement with the calculated values. The threshold voltage is the same as that of CMOS, because 60 V NMOSFET channel is formed by the same diffusion processes as that of CMOS. Figure 7 compares the on-resistance of this device to previously published data. The developed 60 V NMOSFET shows the best performance among the CMOS-compatible structures.

3.2 *High side switch operation*

High side switching operation is an important function in automotive applications, especially in case of H-bridges for motor control. The on-resistance of conventional high voltage MOSFETs on SOI is influenced by the substrate bias.[4)] However, the developed NMOSFET is free from substrate bias influence as seen in Fig. 8. This is because the hole accumulation layer is induced on the buried oxide, shielding the influence of the source to substrate bias (see Fig. 9). These results indicate that



(a)



(b)

Fig. 5. (a) Current-voltage curve, and (b) forward blocking characteristics of the developed 60 V NMOSFET.

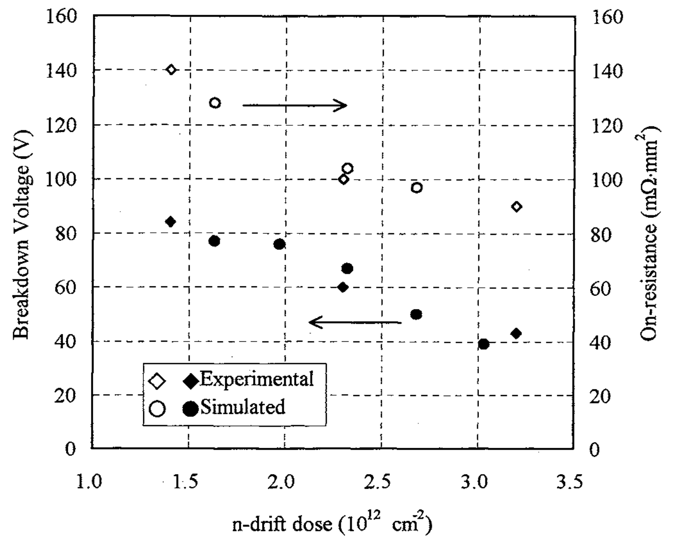


Fig. 6. Dependence of experimentally obtained on-resistance and breakdown voltage on the impurity dose of n-drift layer.

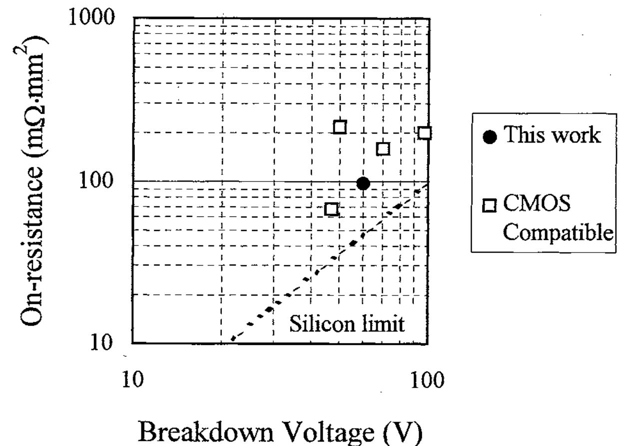


Fig. 7. Comparison of on-resistance—breakdown voltage for this work and previously published data. Only our device can be used as a high side switch.

this device can be used for high side switch without on-resistance increase.

3.3 *High temperature operation*

Figure 10 shows the dependence of leakage current on temperature. The measured leakage current at 200°C is only 3 μA, while on-current is 1.3 A (V_g = 5 V and V_d = 1 V; see Fig. 5(b)). This results indicate that the developed device is suitable for high temperature usage.

4. Application to Integrated Circuit

Many studies of power ICs have been presented. Epi-wafers with n^+ buried layers have been conventionally utilized.[5,6] However, the SOI solution is now practical because the price of bonded SOI wafers with thicker silicon layers has become almost the same as that of epi-wafers with n^+ buried layers. Dielectric isolation using SOI substrate and shallow trench can reduce their large isolation area and parasitic devices. One possible power IC structure to which the developed high voltage NMOSFET is applied is shown in Fig. 11. In this section, we present the operation of other low voltage devices and circuits on the same SOI wafer in order to verify the compatibility of the process.[7]

4.1 *4 bit CMOS MPU*

The fabricated SOI 4 bit MPU consists of 30,000 FETs for Core, 6,000 FETs for cash and 120,000 read-only-memory (ROM) FETs, shown in Fig. 12. This MPU were fabricated on 2 μm SOI by the same 0.8 μm rule BiCMOS process as high voltage NMOSFET. The p- and n-well layers were diffused into the buried oxide layer.

This MPU chips operated at a 20% faster clock speed of 50 MHz at 25°C as compared with 42 MHz of the bulk version MPU and even operated at over 200°C. It was found that clock speed can be improved and that a large latch up immunity at high temperature was realized even if any MOSFET is not isolated by trenches and if the SOI layer is not thin as SIMOX. The maximum operating temperature was expected to be more than 300°C but was not able to be measured because of instrument limitation. It was found that the yield of the MPU fabricated on SOI is the same as that on bulk wafers, verifying that the crystal quality of the currently available SOI wafer is sufficiently good. It was also found that

even bulk MPUs can be operated at 300°C if MPUs consist of pure CMOS although the power consumption of the bulk MPU is larger than that of the SOI one.

4.2 *Vertical pnp and npn transistors*

Although SOI wafers have no n^+/p^+ buried layers, vertical npn and pnp transistors fabricated on the n-well and p-well layers exhibited sufficiently good characteristics, as seen in Fig. 13. The p- and n-base diffusion area are 48 μm^2 and 114 μm^2, respectively. The current gains h_{FE} obtained for the vertical npn and pnp transistors were 80 and 30, respectively.

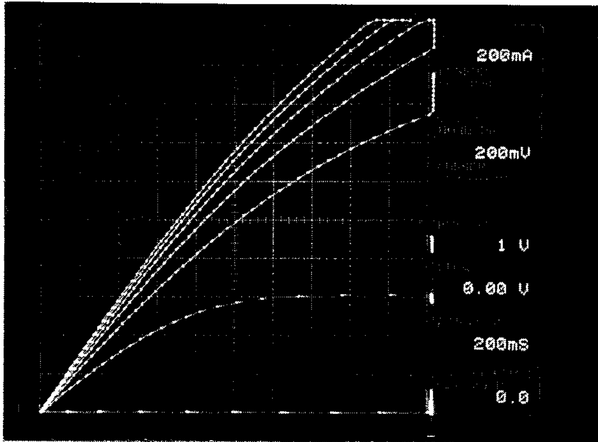


Fig. 8. Current-voltage curve of the 60 V MOSFET for −50 V substrate bias voltage. The substrate bias influence was completely suppressed.

4.3 *Analog circuits*

Figure 14 shows the output voltages of the ban gap reference circuit shown in Fig. 15 as a function of temperature with the silicon layer thickness as a parameter. It was found that maximum operating temperature of CMOS/npn analog circuits (not trench isolated) simply increases as the silicon layer thickness decreases. and 200°C operation is possible for 2 μm SOI.

It should be noted that the CMOS and bipolar transistors described in this section were fabricated by 6 μm rule BiCMOS process and were not isolated by trenches but isolated by pn junction (see Fig. 16). If each bipolar transistor is isolated by trenches, much higher temperature operation is expected. These results assure 200°C operation of whole IC chips based on the SOI wafer, if each bipolar transistor is trench-isolated.

5. Conclusion

We have developed high voltage lateral power NMOSFETs on 5 μm SOI which are compatible with 0.8 μm CMOS process. The measured specific on-resistance of the fabricated device was 100 mΩ·mm^2 and breakdown

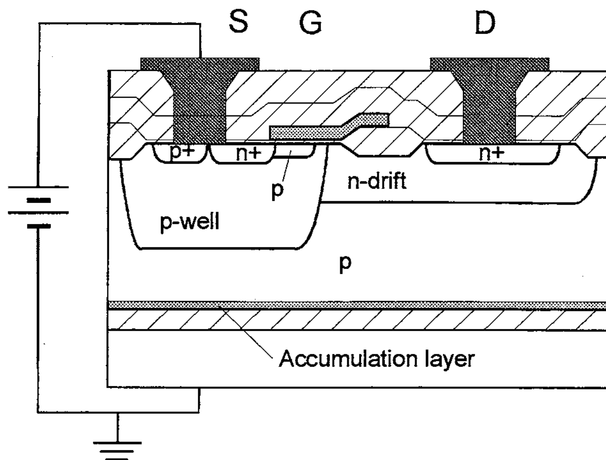


Fig. 9. Cross-sectional view of the high voltage NMOSFET on the p-type SOI substrate. When this device is used for high side switch, the hole accumulation layer is induced on the buried oxide, shielding the influence of the source to substrate bias.

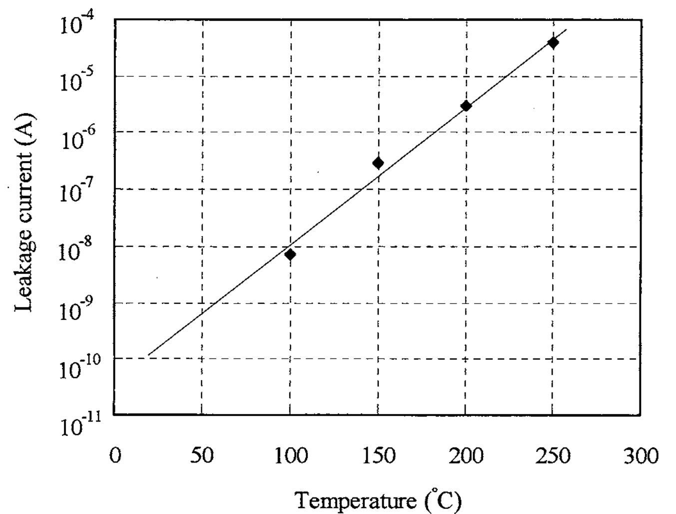


Fig. 10. Dependence of leakage current on temperature for 25 V drain voltage.

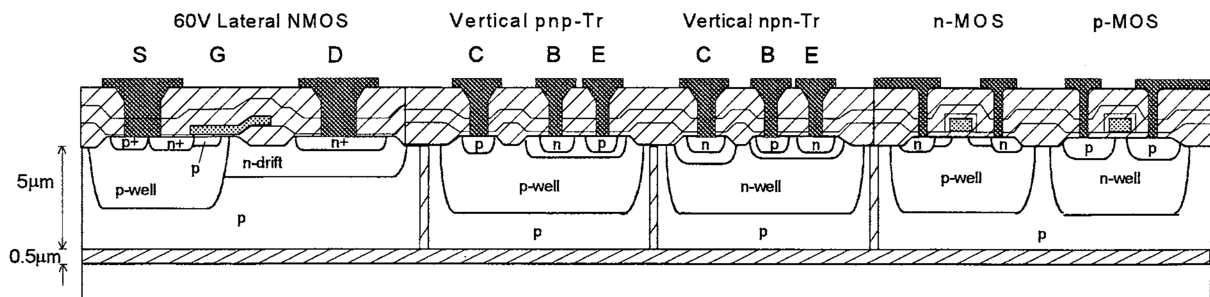


Fig. 11. Cross-sectional view of one possible power IC to which the developed power MOSFET is applied.

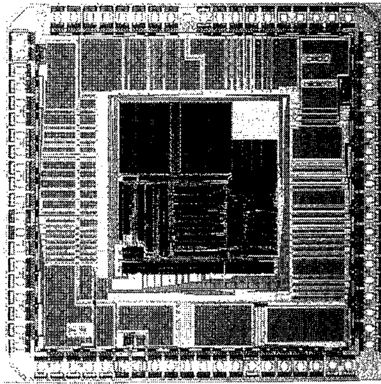
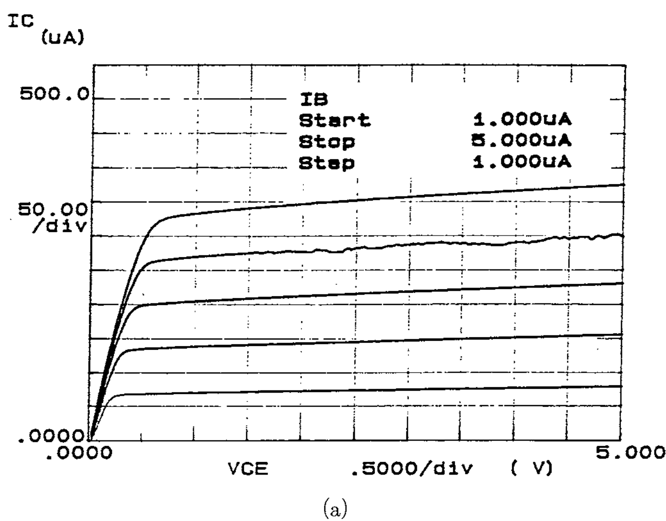
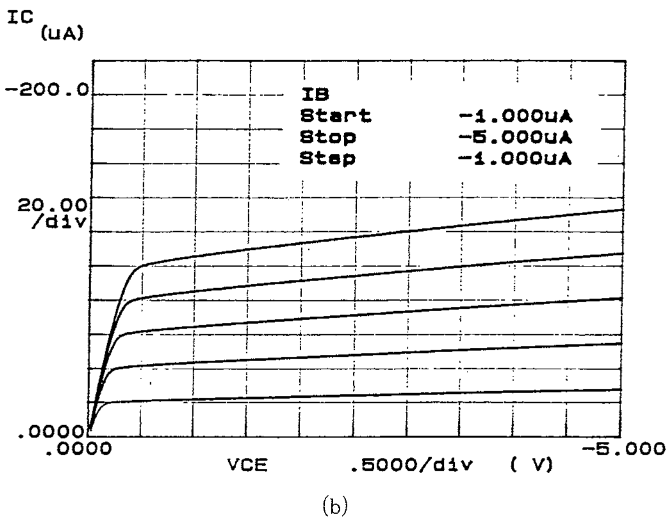


Fig. 12. Photograph of the 4 bit CMOS MPU of 156,000 transistors.



(a)



(b)

Fig. 13. Current-voltage curves of the vertical (a) npn and (b) pnp transistors. The p- and n-base diffusion areas are 48 μm^2 and 114 μm^2, respectively.

voltage was 60 V, which is the best performance among the CMOS compatible structure and comparable to that of diffusion self-aligned DMOSFET. Furthermore, The fabricated device can be operated as a high side switch without on-resistance increase because of the induced bottom accumulation p-layer.

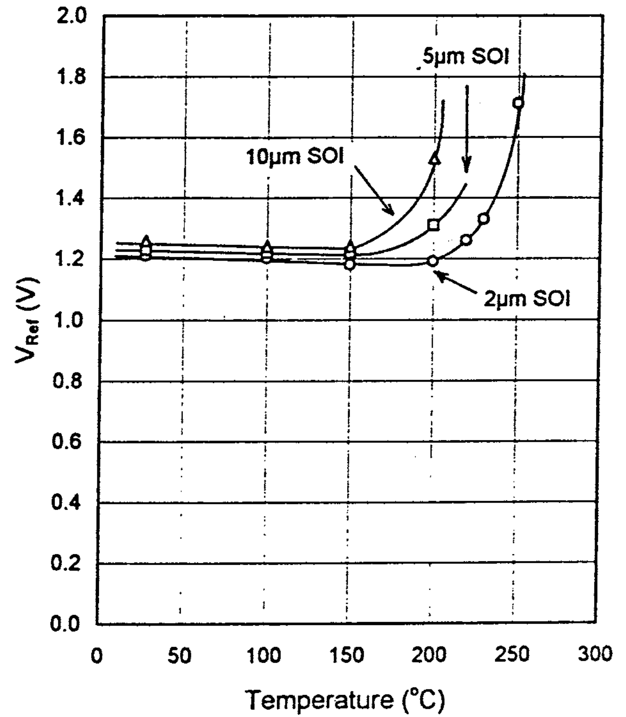


Fig. 14. Output voltages of the band gap reference circuit on SOI as a function of the temperature with the silicon layer thickness as a parameter.

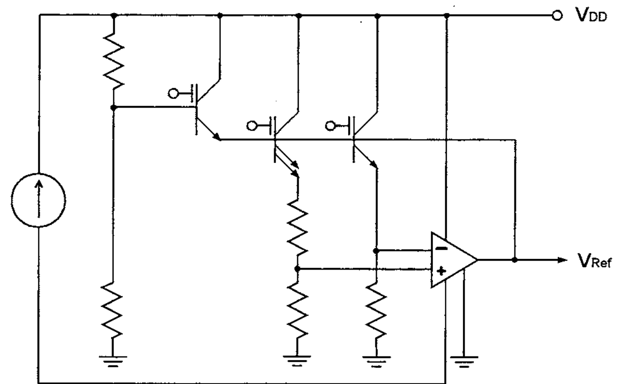


Fig. 15. Block diagram of the band gap reference circuit.

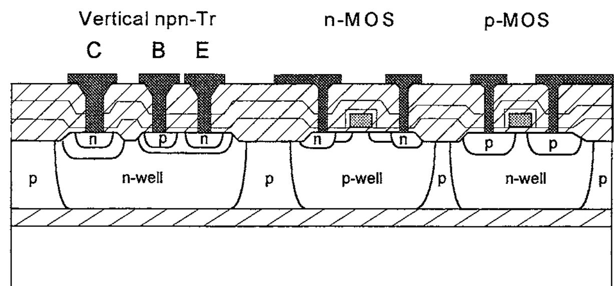


Fig. 16. Cross-sectional view of the analog circuits. CMOS and bipolar transistors were not isolated by trenches but isolated by pn junction.

Application of the developed device for power IC is also discussed. Since exactly the same process was adopted for fabrication of the developed power MOS-

FET, it is suitable for output devices in power ICs integrating MPU and BiCMOS circuitry. Operations of these circuits are demonstrated. these results verify the compatibility of the process.

In addition, we also show that MPUs and BiCMOS analog circuits on thin SOI is suitable for high temperature operation.

Acknowledgements

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