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Numerical Prediction for 2GHz RF Amplifier of SOI Power MOSFET

Ichiro Omura and Akio Nakagawa
Research and Development Center, Toshiba Corp.
1 Komukai Toshibacho, Saiwai-ku, Kawasaki 210, Japan
Phone: 044-549-2150, Fax.:044-520-1254

RF performance of a MOSFET on silicon-on-insulator (SOI) with a 0.5 μm gate length and a 2 μm buried oxide thickness has been numerically predicted using 2-D device simulator to check its applicability to digital cellular telephones. The device has been found to have excellent performance for 2 GHz high-power amplifier at 2.8 V power supply. Calculated f_t and f_{max} for the intrinsic MOSFET are 23 GHz and 65 GHz. SOI MOSFET is a promising candidate to replace GaAs MESFETs in 2 GHz RF applications.

1 Introduction

Silicon MOSFETs have been increasingly adopted to RF power amplifiers for personal communication systems operating at frequencies below 1 GHz, because of the low cost of these devices and the maturity of the technologies they employ, compared with GaAs MESFETs ([1], [2]). To operate silicon power MOSFETs at a higher frequency such as 2 GHz, it is necessary to reduce the output capacitance and to reduce the electron transit time through the gate channel. In this paper, the authors numerically show that an SOI MOSFET with a 0.5 μm gate length and a 2 μm buried oxide thickness has excellent performance for a 2 GHz high-power amplifier at 2.8 V power supply. An SOI structure with relatively thick buried oxide layer reduces the output capacitance. A submicron channel achieved by the recent advanced silicon technology reduces the electron transit time through the channel.

Simulations have been carried out using a 2-D device simulator, TONADDE II C, which can simulate devices with arbitrary external circuits([3],[4]).

2 Simulated SOI MOSFET structure

The cross-section of the simulated MOSFET is shown in Fig. 1. Large output capacitance is one of the most serious problems to which conventional bulk silicon RF power MOSFETs are subject at a high frequency operation. Output capacitance for an SOI MOSFET consists of drain-substrate capacitance and drain-source junction capacitance. Thus MOSFET is fabricated on SOI with a sufficiently thick buried oxide to reduce the drain-substrate capacitance. A combination of a DMOS structure and

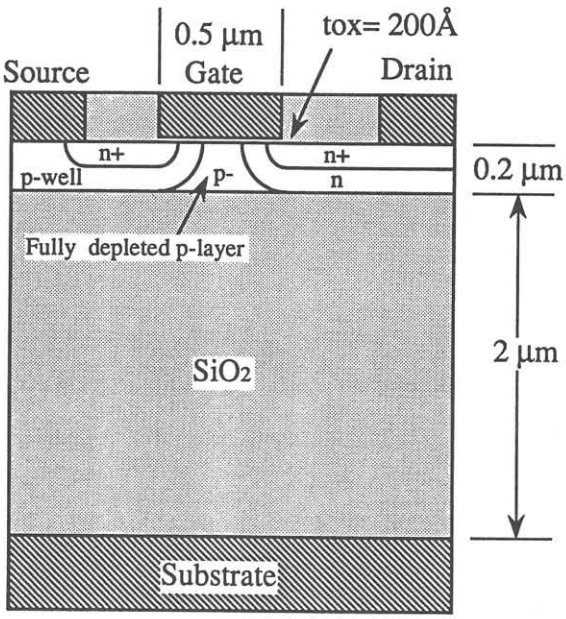

Fig. 1 Cross-section of the simulated SOI RF power MOSFET.

a fully depleted 0.2 μm thick high resistance p^- layer under the gate oxide is adopted to reduce the drain-source junction capacitance and to prevent bipolar action.

Unlike conventional lateral RF power MOSFET structures on a bulk silicon, the device has a double diffused drain n-layer(LDD), instead of a drain extension layer (n-offset layer), because of the following reason. The n-offset layer has been used to enhance the drain-source breakdown voltage. However, a low drain-source breakdown voltage of 8 V,

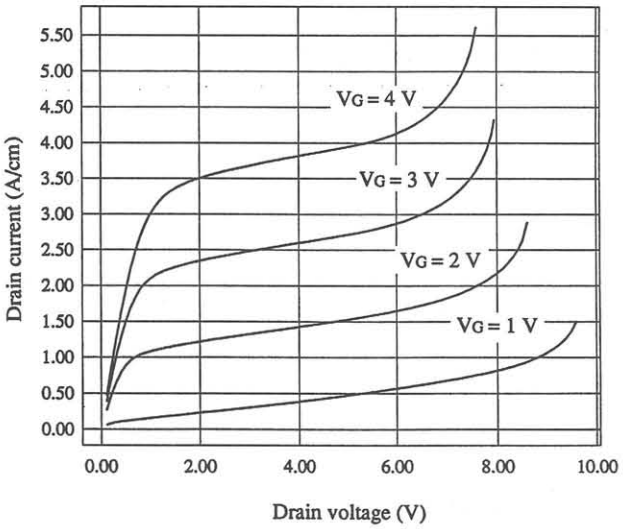

Fig. 2 V–I characteristics for the SOI-MOSFET.

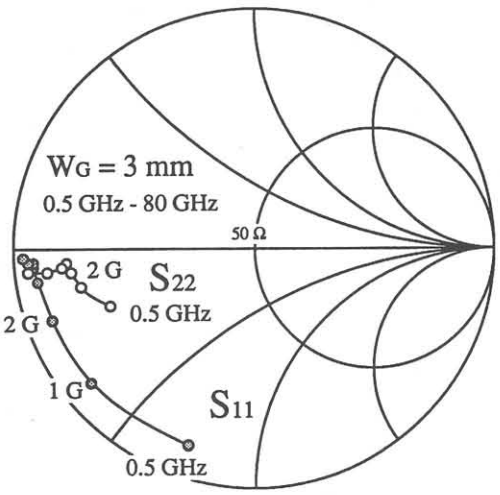

Fig. 3 Calculated S_{11} and S_{22}.

which is sufficient for a 2.8 V power supply, can be attained without the n-offset layer. Further, voltage drop in the n-offset layer degrades the V–I characteristics in a high current region. Thus, LDD structure has been adopted instead of the n-offset layer.

3 V–I characteristics and output capacitance

Calculated V–I characteristics for the device is shown in Fig. 2. The breakdown voltage of 8 V is realized without an n-offset layer. The transconductance gm is 1200 mS for a 1 cm channel width.

The drain-substrate capacitance is reduced to 0.16 pF for a 1 cm gate width by adopting the SOI structure with relatively thick buried oxide. Since the active layer thickness is only 0.2 μm, the drain-source junction capacitance is about 0.4 pF for a 1 cm gate width. Also, the output capacitance is found to be almost constant for a wide range of the drain voltage. This enhances the linearity of RF characteristics at large signal operations.

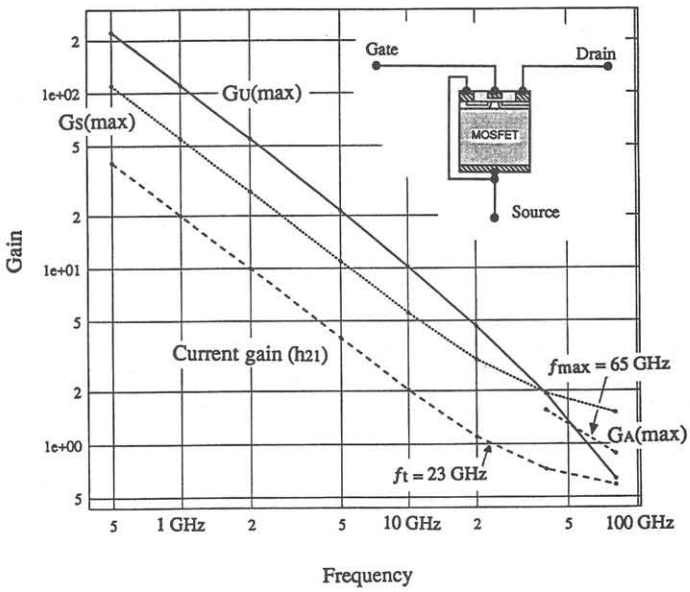

Fig. 4 Current gain, Gu(max), Gs(max) and Ga(max) for intrinsic MOSFET.

4 Small signal analysis

The small signal characteristics of the intrinsic SOI MOSFET have been simulated using the 2-D device simulator. Fig. 3 shows obtained S-parameters for 0.5 GHz to 80 GHz and Fig. 4 shows RF gains as functions of frequency. f_t and f_{max} are 23 GHz and 65 GHz, respectively.

The influences of parasitic resistances, capacitances and etc. on the RF gains of the intrinsic power MOSFET are also numerically predicted. Parasitic components shown in Fig. 5 are taken into account in the simulated circuit. Although the obtained gains are decreased in the high frequency region compared with those for the intrinsic MOSFET, sufficiently high f_t and f_{max} of 12 GHz and 15 GHz are still observed. These results imply that the proposed SOI MOSFET has sufficient RF performance for 2 GHz amplifiers.

5 Large signal analysis

Large-signal transient simulations at $V_{DD} = 2.8$ V and $V_{GG} = 2.0$ V have been carried out using the 2-D device simulator to obtain the output power versus input power characteristics for the intrinsic SOI MOSFET. The conjugate of small signal S-parameter s_{22} which is obtained in section 4 is used as the output load impedance of the SOI MOSFET. This assumes an ideal impedance matching circuit between the MOSFET and a 50 Ω load.

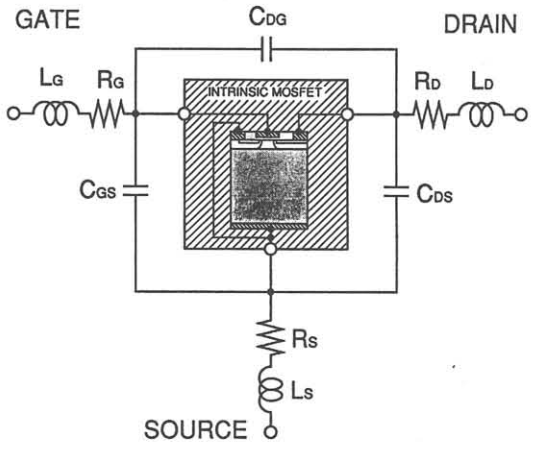

Fig. 5 A simulated circuit example with extra parasitics.

Fig. 6 shows an obtained dynamic waveform for 2 GHz operation and Fig. 7 shows the input power versus output power characteristics. Good linearity has been observed up to 1 W output power for the SOI MOSFET with a 1 cm channel width.

6 Conclusion

A MOSFET on SOI with a 0.5 μm gate length and a 2 μm buried oxide thickness for 2GHz high-power amplifier at 2.8 V power supply is simulated using a two-dimensional device simulator. Calculated f_t and f_{max} are 23 GHz and 65 GHz for the intrinsic MOSFET. Sufficiently high f_t and f_{max} of 12 GHz and 15 GHz are still observed even if extra parasitics are included in the simulation. SOI MOSFET is a promising candidate to replace GaAs MESFETs in 2 GHz RF applications.

bibliography

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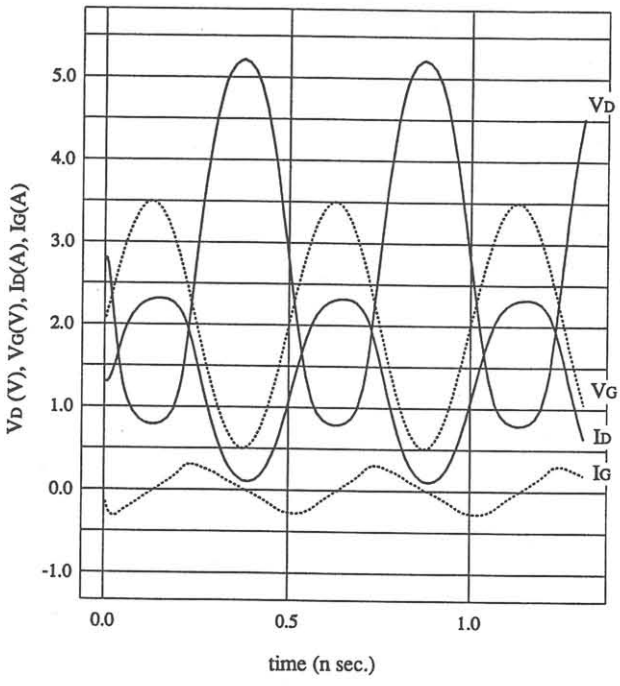

Fig. 6 Dynamic waveform at 2 GHz operation.

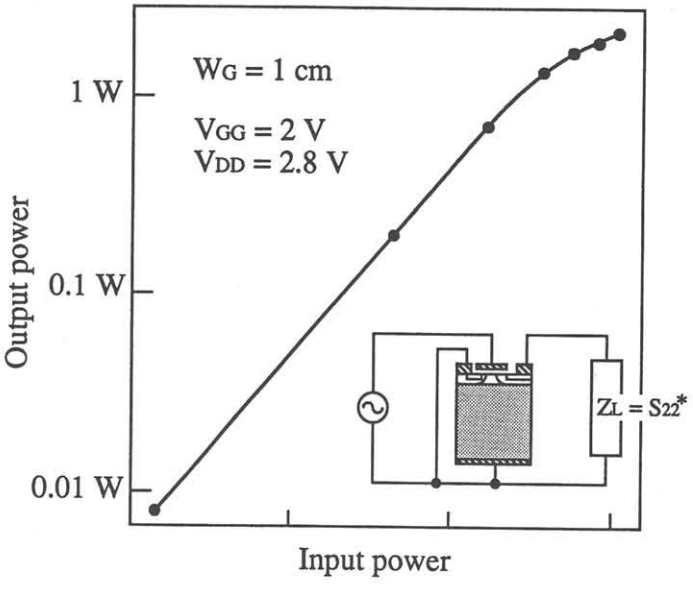

Fig. 7 Input-output characteristics at a frequency of 2 GHz for the intrinsic MOSFET obtained by 2-D device simulations. Good linearity is observed up to 1 W for 1cm gate width.