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SOI Layer Thickness and Buried Oxide Thickness Dependencies of High Voltage Lateral IGBT Switching Characteristics

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High voltage lateral IGBTs were fabricated on relatively thin SOIs. The authors realized breakdown voltages of above 300 V for SOIs on a 2 μm buried oxide and of above 400 V for SOIs on a 3 μm buried oxide. The buried oxide thickness has been found to influence the turn-off waveform but not influence the turn-off loss. The switching characteristics are improved as the SOI layer thickness decreases. Thin SOIs have advantages in realizing high speed switching lateral IGBTs without any special design and lifetime control.

1. INTRODUCTION

SOI technology is attractive for power IC applications, because complete dielectric isolation can easily be realized by simple trenches[1]. The authors have proposed and have experimentally verified that a high breakdown voltage can be realized in a device on a relatively thin SOI[1-3]. Recently, it was reported that lateral IGBTs on SOIs operate with high switching speed as compared with those fabricated on bulk wafers[4,5].

An SOI thickness of less than 10 μm is desirable for practical trench isolation. The authors fabricated lateral IGBTs on 4 μm to 20 μm SOIs and studied the SOI thickness and the buried oxide thickness dependencies of their electrical characteristics. It has been confirmed that a high breakdown voltage can be realized on SOIs less than 10 μm thick. The switching speed of lateral IGBTs has been found to be improved as the SOI layer thickness decreases. IGBTs on a 4 or 5 μm SOI operate over 20 kHz without any special device design. The trade-off relation between forward voltage-drop and turn-off fall time was as good as or even better than that for optimized IGBTs on bulk wafers. These results show that high voltage power ICs can be fabricated on SOIs at a reasonable cost by simply utilizing conventional CMOS processes with a shallow trench process and a few additional masks without using lifetime control.

2. HIGH VOLTAGE DEVICE STRUCTURE

Figure 1 shows the structure of the fabricated lateral IGBTs. SOI substrates were prepared by silicon wafer direct bonding. The buried silicon dioxide layer thicknesses were 2 μm or 3 μm.

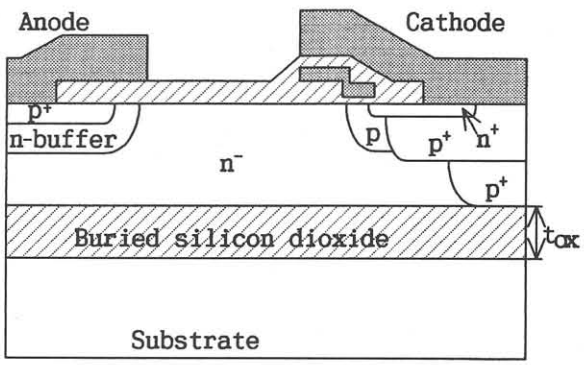

Fig.1 Cross-sectional view of fabricated SOI lateral IGBT

When the SOI is thin, a vertical high electric field occurs below the anode. If the drift region is sufficiently long and the horizontal structure is optimized, the blocking voltage is determined by the vertical high electric field under the n-buffer. In the IGBT shown in Fig.1, the n layer under the n-buffer region is completely depleted when a high voltage is applied. The voltage applied between the anode and the substrate is supported both by the depleted n layer and by the buried silicon dioxide layer. As the buried silicon dioxide becomes thicker, a larger share of the applied voltage is supported by the oxide, realizing a higher breakdown voltage. On the other hand if the SOI layer is thicker, the depleted n

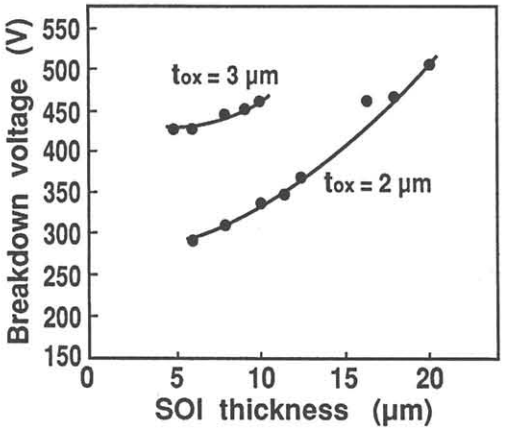

Fig.2 Breakdown voltage vs. SOI thickness

layer can sustain a larger voltage. The breakdown voltage increases almost linearly with an increase in the SOI thickness.

Figure 2 shows the relation between the breakdown voltage and the SOI thickness. Decreasing the SOI thickness decreases the breakdown voltage. However, using a 2 μm thick buried silicon dioxide layer maintains the breakdown voltage above 300 V even for SOI thicknesses of less than 10 μm, and a 3 μm thick dioxide layer maintains the breakdown voltage above 400 V. Trench isolation is available for SOIs of such thicknesses.

3. TURN-OFF CHARACTERISTICS

The turn-off characteristics were measured under a resistive load. Figure 3 shows the turn-off waveforms for IGBTs with the same SOI thickness, the same n-buffer impurity dose, and different buried oxide thicknesses.

It has been found that the turn-off waveforms for SOI IGBTs have unique shapes, characterized by a terrace tail current. The terrace current is influenced by the buried oxide thickness, as shown in Fig.3. The reason is explained as follows. The substrate, the buried oxide layer, and the SOI layer constitute a MOS structure. A p channel is induced on the buried oxide when the drain voltage recovers during the turn-off transient. The stored holes are swept away through the p channel as the terrace current. The conductance of the induced p channel determines the magnitude of the terrace current. The conductance depends on the buried oxide thickness. A p channel on a thinner buried oxide have a higher conductance for the same applied voltage. Accordingly, IGBTs with a 2 μm thick oxide have higher terrace currents than IGBTs with a 3 μm thick oxide. The amount of stored holes does not depend on the buried oxide thickness. If the terrace current is large,

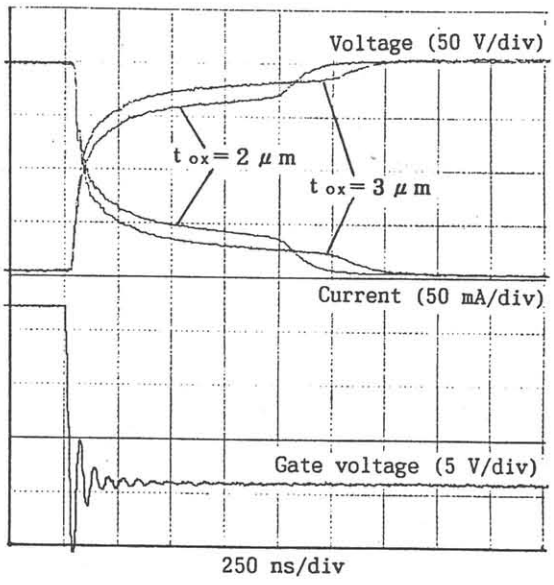

Fig.3 Turn-off waveforms for IGBTs on 9 μm thick SOI

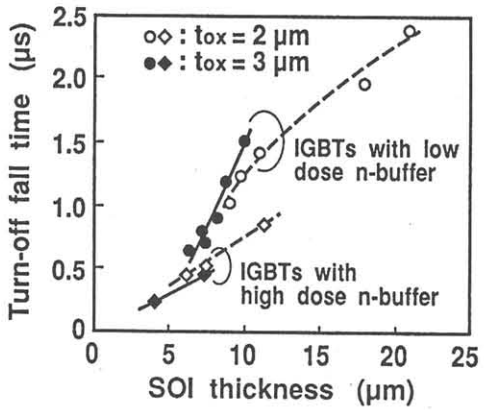

Fig.4 Turn-off fall time vs. SOI thickness

the stored holes are swept away quickly and the terrace is short.

The relation between the turn-off fall time and the SOI thickness is shown in Fig.4. The fall time is improved by decreasing the SOI thickness. The reason is that the amount of carriers stored in the SOI layer at the on-state depends on the drift region volume. The amount of the stored carriers also depends on the n-buffer impurity dose or hole injection efficiency. A high dose of the n-buffer contributes to high speed turn-off. IGBTs with a high dose n-buffer on a thin SOI are suitable for a high frequency operation of over 20 kHz.

The relation between the turn-off loss and the SOI thickness is shown in Fig.5. Decreasing the SOI thickness decreases the turn-off loss. The turn-off loss does not depend on the oxide thickness, although the turn-off waveforms are influenced by the oxide thickness as described above.

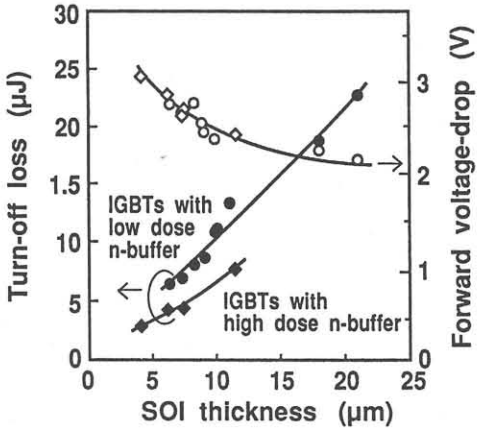

Fig.5 SOI thickness dependencies of turn-off loss and forward voltage-drop

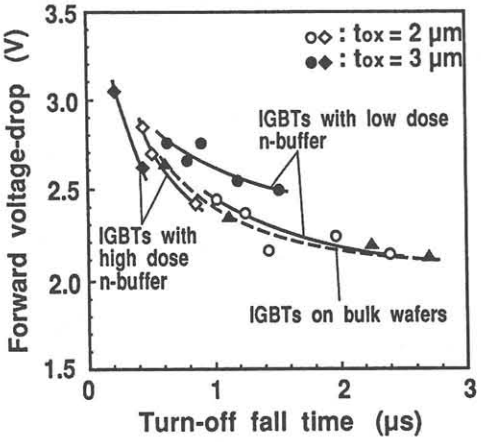

Fig.6 Trade-off relation between forward voltage-drop and turn-off fall time

4. FORWARD VOLTAGE-DROP

The SOI thickness dependence of the forward voltage-drop for a current density of 100 A/cm2 is also shown in Fig.5. The forward voltage-drop slightly increases with decreasing the SOI thickness. However, it does not depend on the buried oxide thickness and the n-buffer impurity dose.

5. TRADE-OFF RELATION BETWEEN FORWARD VOLTAGE-DROP AND TURN-OFF CHARACTERISTICS

It has been found that a high impurity dose of the n-buffer gives a good trade-off relation between the forward voltage-drop and the turn-off characteristics. A high dose n-buffer causes high speed turn-off, and results in a low turn-off loss. On the other hand, the forward voltage-drop does not depend on the n-buffer impurity dose. The trade-off relation between the forward voltage-drop and the turn-off fall time is shown in Fig.6. The individual lines show the trade-offs for fixed n-buffer impurity doses and fixed buried oxide thicknesses when the SOI thickness is changed. IGBTs with a high dose n-buffer show a good trade-off relation. The trade-off for IGBTs fabricated on bulk wafers is also shown in the figure. These IGBTs have a special drain structure for suppressing the hole injection efficiency. SOI IGBTs can perform high speed turn-off without any complicated device design and have a trade-off as good as or even better than that of IGBTs on bulk wafers.

6. CONCLUSION

It has been confirmed that high voltage IGBTs can be made on thin SOIs by using a thick buried oxide layer. Breakdown voltages above 300 V have been realized on SOIs of less than 10 μm with a 2 μm buried oxide. Thin SOIs are favorable for the dielectric isolation of power devices by shallow trenches.

Using thin SOIs also improves the turn-off characteristics. IGBTs with a high dose n-buffer on a thin SOI have advantages in realizing a high speed switching operation without any special design and lifetime control. The trade-off relation between the forward voltage-drop and the turn-off fall time for SOI IGBTs has been found to be equal to or even better than that for IGBTs on bulk wafers. These results show that it is possible to fabricate SOI power ICs at a reasonable cost by utilizing conventional CMOS processes with a shallow trench process.

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