Extended Abstracts of the 1992 International Conference on Solid State Devices and Materials, Tsukuba, 1992, pp. 137-139

Dynamic Shielding of Substrate Bias Effects on Electrical Characteristics of High Voltage IGBTs on SOI

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Abstract

This paper shows that the on-resistance of high voltage MOSFETs on SOI is not significantly affected by the substrate bias, if the thickness of the SOI layer is greater than 100nm. This is because the substrate bias can dynamically be shielded by creation of a p-channel on the bottom oxide. It was found that high voltage double injection devices such as IGBTs on relatively thick SOI can be almost free from substrate bias effects.

1. Introduction

Dielectric isolation(DI) is an indispensable technique for high voltage power ICs. The conventional DI method(EPIC) has been applied to telecommunication ICs etc. However, it has demerits of high cost due to complicated fabrication processes. Recently, trench isolated SOI has been paid attention as a promising candidate for replacing the conventional DI method[1], because relatively thick SOI layers can easily be fabricated by silicon wafer direct-bonding method. Problems are:

1)how to achieve high breakdown voltages on thin SOI layers,

2)how to prevent influences of substrate bias on the device characteristics.

Several methods[1,2,3] have already been proposed to attain more than 500V breakdown voltage by applying a large share of the applied voltage across the bottom oxide film. However, no detailed study has been made on the substrate bias influence on high voltage SOI devices.

This paper shows, for the first time, that the relatively thick SOI can be relatively free from substrate bias effects. Negative substrate bias generally increases on-resistance of a junction isolated high voltage n-channel MOSFET[4]. However, it was found that the on-resistance of high voltage MOSFETs on SOI is not significantly affected by the substrate bias, if the thickness of the SOI layer is greater than a few 100nm. This is because the substrate bias can dynamically be shielded by creation of a p-channel on the bottom oxide.

2. Shielding of substrate bias effects

Figure 1 show a studied 500V IGBT structure on 15μm SOI. Figure 2 shows calculated carrier distributions when a -100V negative substrate bias is applied against both the source and the drain. It is seen that substrate bias is shielded by the induced bottom p-channel and that most of the SOI layer remains undepleted. This means that the on-resistance of relatively thick SOI MOSFETs or IGBTs is not greatly affected by the substrate bias and ,thus, can be used as high side switches or source followers.

Figure 3 shows where holes come from to create a p-channel. When the substrate is negatively biased, both the p-base n-drift layer junction and the p-drain n-buffer junction are forward biased instantaneously, and holes are injected from the p-base and the p-drain into the n-drift layer.

However, the situation is quite different for MOSFETs and anode shorted IGBTs. The p-base n-drift layer junction cannot be forward biased until a depletion layer is created on the bottom oxide and reaches the p-base, as seen in Fig.4, if the substrate bias is applied in a high dv/dt rate. Even for this case, a bottom p-channel will finally be created by generated holes in the depletion layer. Thus, it is recommended that the p-base is formed so as to reach the bottom oxide to act as a source to smoothly create a bottom p-channel.

On the contrary, the on-resistance of a 500V MOSFET on a very thin SOI such as 100nm depends greatly on the substrate bias as seen in Fig.5. This is because the thickness of

SOI layer is comparable to that of inversion layer(p-channel). Figure 6 shows the calculated electron density distribution for the 100nm thick SOI MOSFET with -100V substrate bias. It is seen that most of the SOI layer is depleted.

Thyristor like devices, such as IGBTs, are relatively free from substrate bias effects due to carrier plasma, and exhibit the almost same current-voltage curve regardless of the substrate bias level. Figure 7 shows the calculated current-voltage curve. It was shown that the calculated current voltage curves are hardly affected by a -100V substrate bias. Figure 8 shows the hole density distribution for a 3.0V forward voltage with a -100V substrate bias. It is seen that the carrier plasma easily shields the substrate bias and a hole accumulation layer is formed on the bottom oxide. Figure 9 shows the current flow line for Fig.8. From this figure, it is understood that the substrate bias hardly affects the current voltage curve of IGBTs since only a small portion of the total current flows in the bottom accumulation layer.

3. Switching characteristics of high side switch.

It was found that the switching speed of the lateral IGBT on SOI was almost the same, whether it was used as a high side switch or a low side switch. Figure 10 shows calculated switching waveforms for a lateral IGBT on a 15μm SOI layer as a high side switch with a resistive load. The switching waveforms for the same IGBT as a low side switch is almost the same as those for the high side switch. The two calculated circuit configurations are shown in Fig.11.

Figure 12 and 13 show the hole density distribution and current flow lines for the time step of 0.477μs. It is seen that the tail current flows in the bottom p-channel in the depletion layer. The same phenomena are seen in the low side switch operation. Since, in the tail current period, the drain to substrate voltage for the low side switch is smaller than that of the high switch, which is always 100V, the created p-channel conductance of low side switch is lower than that of high side switch. Thus, the calculated tail current of the high side switch is by 5% larger than that of the low side switch. The difference is quite small.

These results shows that the created p-channel on the bottom oxide does not significantly affects the electrical characteristics of IGBTs on a relatively thick SOI layers.

The calculated peak substrate current for Fig.10 is only 0.0025A at the time step of 0.14μs. Thus, the substrate current is sufficiently small and negligible.

Conclusion

It was concluded that high voltage devices on relatively thick SOI is not significantly influenced by the substrate bias. Lateral IGBTs on SOI can exhibit almost the same electrical characteristics as high voltage output devices regardless of the substrate bias level. This leads to a wide freedom of circuit design in SOI power ICs. Thus, SOI will surely replace conventional DI method.

References

[1]A.Nakagawa et al., IEEE Trans. Electron Devices, ED-38,p.1650(1991)
[2]S.Merchant et al., Proc. of ISPSD'91, p.31
[3]T.Matsudai et al., Proc. of ISPSD'92, p.272
[4]E.Arnold et al., Proc. of ISPSD'92, p.242

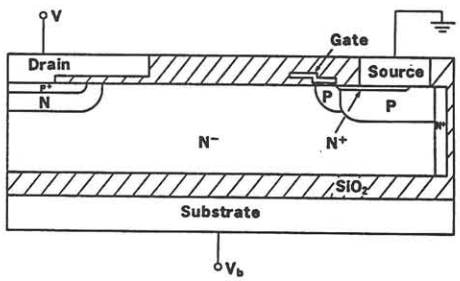

Fig.1 Calculated trench isolated 500V lateral IGBT on 15μm SOI (3μm thick bottom oxide)

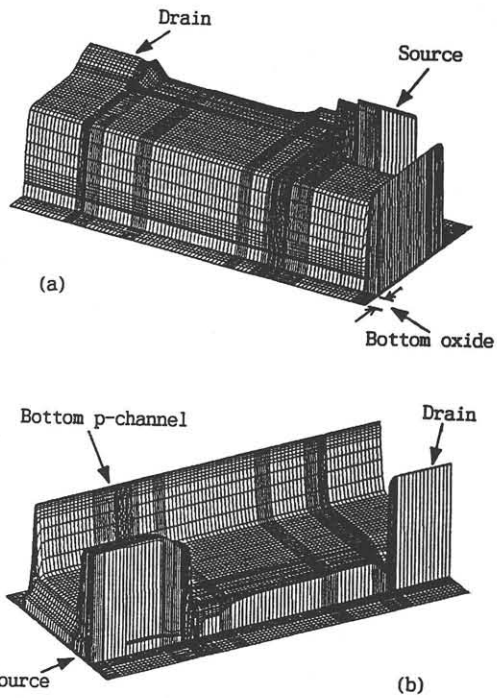

Fig.2 Three dimensional (a)electron and (b)hole density distributions for -100V substrate bias against source and drain. The bottom p-channel is induced to shield substrate bias.

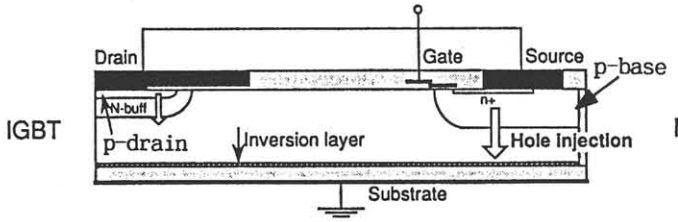

Fig.3 Holes are injected from both p-base and p-drain.

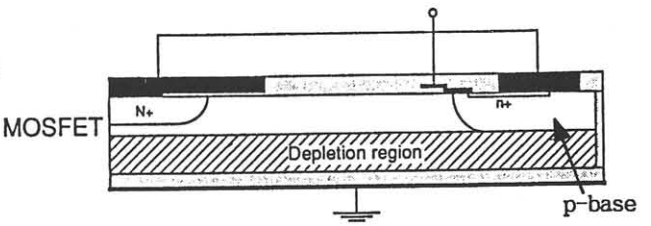

Fig.4 Depletion layer is formed unless p-base diffusion reaches the bottom oxide.

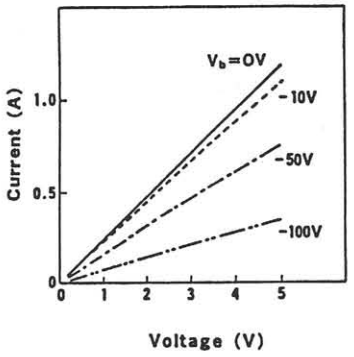

Fig.5
Calculated current-voltage curve of a 500V MOSFET on 100nm SOI for four different substrate biases.

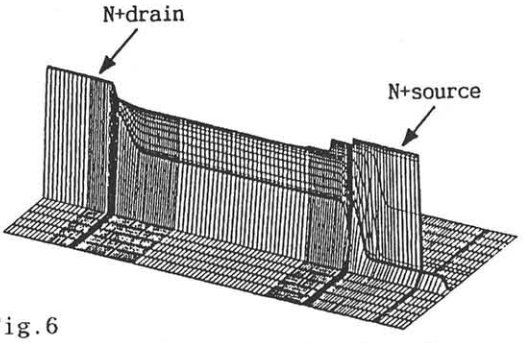

Fig.6
Electron density distribution for a 100nm SOI MOSFET with -100V substrate bias.

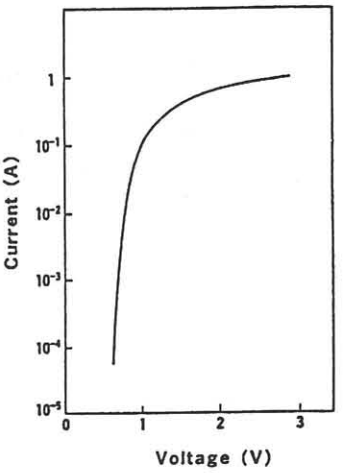

Fig.7
Calculated current-voltage curve for IGBT for Fig.1. The curve hardly depends on substrate bias.

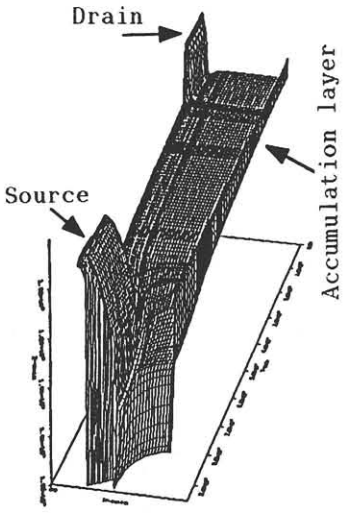

Fig.8
Hole density distribution for 3.0V forward voltage.

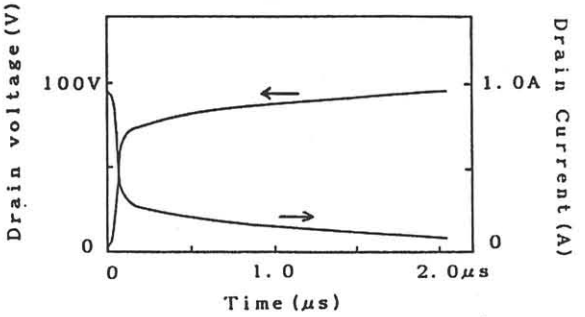

Fig.10 Calculated switching waveforms.

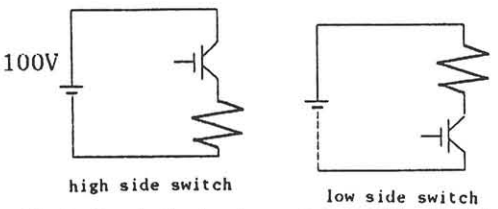

Fig.11 Calculated circuit configurations.

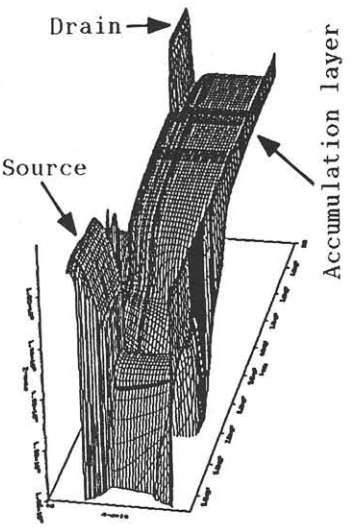

Fig.12
Hole density distribution for 0.477μs time step.

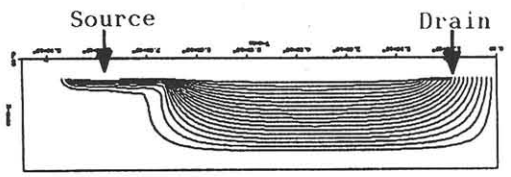

Fig.9 Current flow lines for Fig.8

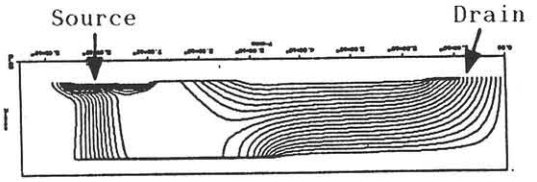

Fig.13 Current flow lines for Fig.12.