

New Anode Structure for High Voltage Lateral IGBTs

Y. Yamaguchi, A. Nakagawa, N. Yasuhara, K. Watanabe and T. Ogura

Toshiba Research and Development Center
1, Komukai Toshiba-cho, Saiwai-ku, Kawasaki-shi, 210, Japan

500 V lateral insulated gate bipolar transistors (IGBTs) with high switching speed have been developed by employing a new anode structure, which is characterized by an n^+ -region formed in a shallow p-drain region. The trade-off relation between the current density and the fall time for the newly developed IGBTs was compared with that for the conventional IGBTs. It was found that the fall time for the new IGBTs was reduced to a half value of that for a conventional one. The developed IGBTs attained 0.2 μs fall time and 0.4 μs storage time without any lifetime control and 70 A/cm² current density for 3 V forward voltage. These characteristics are well suited for output devices of high voltage power ICs.

1. INTRODUCTION

In recent years, power ICs, which integrate power devices, protection circuits and logic functions on the same chip, have been actively studied^{1),2)}. Lateral insulated gate bipolar transistors (IGBTs)³⁾⁻⁵⁾ are suitable for such power ICs as high voltage output devices, because of their lower on-resistance than that for MOSFETs. However, the turn-off switching speed for IGBTs is still not so fast as that for MOSFETs, although many studies^{6),7)} have been done to improve their switching speeds.

In this paper, a new anode structure is proposed to realize a high turn-off switching speed for IGBTs. This structure is characterized by an n^+ -region formed in a shallow p-drain layer.

2. DEVICE STRUCTURE

A schematic cross section for the newly developed device structure is shown in Fig.1 together with a conventional device structure. A dielectric isolation technique, based on the silicon wafer direct-bonding (SDB) and V-grooves was applied to isolate

output devices on a p^- silicon layer⁸⁾. The maximum withstanding voltage for the dielectric isolation between silicon islands and the substrate is over 800 V, which is sufficient for output devices with 500 V breakdown voltage. The new device structure is characterized by an n^+ -region formed in a shallow p-drain layer. A buried p^+ diffusion layer on the bottom oxide film is formed before silicon wafer direct-bonding. This layer is electrically connected to the p-base region through a p^+ -diffusion layer on a V-groove side wall.

3. EXPERIMENTAL RESULTS AND DISCUSSION

It was found that the fall time was reduced by optimizing impurity dose Q_p for the shallow p-drain layer and the n^+ -region length L_N (see Fig.1. for the definition). Figure 2 shows the experimental results for the fall time as a function of the net impurity dose (Q_p) for a shallow p-drain layer. Figure 3 shows the dependence of the fall time on the n^+ -region length (L_N). The fall time reduced with an decrease in the Q_p amount or with an increase in the n^+ -region

length. The reason is that the emitter efficiency of the p-drain layer can be effectively controlled by the parameters of Q_p and L_N .

It was further found that the fall time was reduced by increasing the impurity dose for the buried p^+ diffusion layer formed on the buried oxide film (see Fig.4). This is related to the fact that a large portion of the hole current is assumed to flow through the bottom p^+ diffusion layer, since the sheet resistance in this layer is much smaller than that in the high resistivity p^- -layer.

The newly developed LIGBTs realize a shorter fall time than the conventional LIGBTs, without significant increase in the on-resistance. The trade-off relations between the fall time and the current density for the newly developed LIGBTs and the conventional LIGBTs are compared in Fig.5, where the fall time for the newly developed LIGBTs was changed by changing the shallow p-drain impurity dose, while that for the conventional LIGBTs was controlled by the n-buffer layer impurity dose. It is manifest that the newly developed structure can attain a better trade-off relation compared with the conventional n-buffer structure.

Figures 6 and 7 show typical turn-off waveforms for the conventional LIGBTs with low n-buffer impurity dose and high n-buffer impurity dose, respectively. In general LIGBTs, fabricated on the p^- silicon island, can realize smaller tail currents although they have relatively longer storage time⁹⁾. This is because, for the device on a p^- silicon island, the depletion layer develops beneath the n-buffer layer where the largest carrier density exists in the device. Thus, the stored carriers have to be swept away in the storage period, resulting in a long storage time. Figure 8 shows typical turn-off waveforms for a new device with a

low n-buffer impurity dose and a low shallow p-drain impurity dose. In contrast to the conventional LIGBTs on p^- silicon layer, the new LIGBT successively attained short storage time.

This device attained a non-latchup operation in addition to a high turn-off switching speed. The short circuit safe operating area was realized up to 300 V drain voltage.

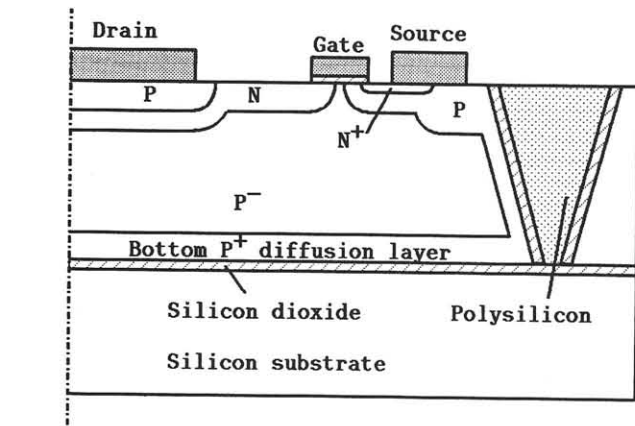
The new structure has an advantage over the anode short structure⁶⁾ or the Schottky structure⁷⁾, in that it has a low on-resistance, even at the low drain current density level, as is shown in Fig.9. This is because the new n^+ -region dose not suppress the hole injection at the low drain current region. In contrast to this, the anode short and the Schottky junction completely suppress the hole injection at the low drain current density level. The low on-resistance characteristics at the low drain current level is a one of the important characteristics for output devices for power ICs to realize small output device area.

4. CONCLUSION

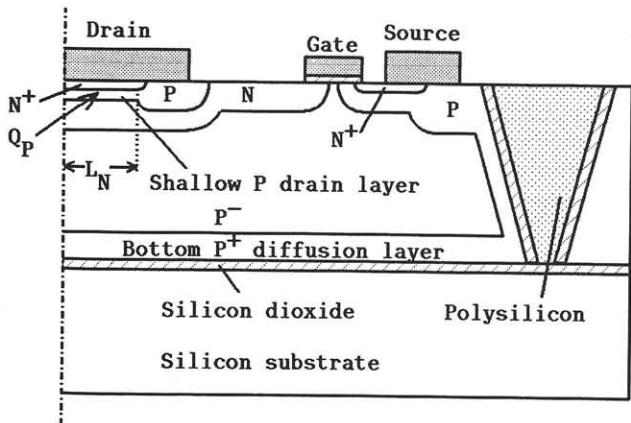
The new anode structure, characterized by the n^+ -region formed in the shallow p-drain layer, realized a short fall time, without significant increase in on-resistance. A 70 A/cm^2 current density for 3 V forward voltage, less than $0.2 \mu\text{s}$ fall time and less than $0.4 \mu\text{s}$ storage time were realized. The new structure is suitable for power ICs, because it does not need any lifetime control. These characteristics satisfy the features required for output devices for power ICs, such as induction motor control ICs.

References

- 1) J.G.Mansmann et al; IEEE PESC '88 Record, p.1319, (1988)
- 2) J.C.Gammel et al; Proc. 1988 ISPSD, p.117, (1988)
- 3) A.L.Robinson et al; IEEE IEDM Tech.Digest, p.744, (1985)
- 4) M.R.Simpson et al; IEEE IEDM Tech.Digest, p.740, (1985)
- 5) A.Nakagawa et al; Ext.Abs.of 20th ICSSDM, p.33, (1988)
- 6) P.A.Gough et al; IEEE IEDM Tech.Digest, p.218, (1986)
- 7) J.K.O.Sin et al; Electron.Lett., vol.21, p.1134, (1985)
- 8) H.Ohashi et al; IEEE IEDM Tech.Digest, p.210, (1986)
- 9) A.Nakagawa et al; IEEE IEDM Tech.Digest, p.817, (1988)



(a) Conventional LIGBT



(b) Newly developed LIGBT

Fig.1 Cross-sectional views for newly developed LIGBT and conventional LIGBT

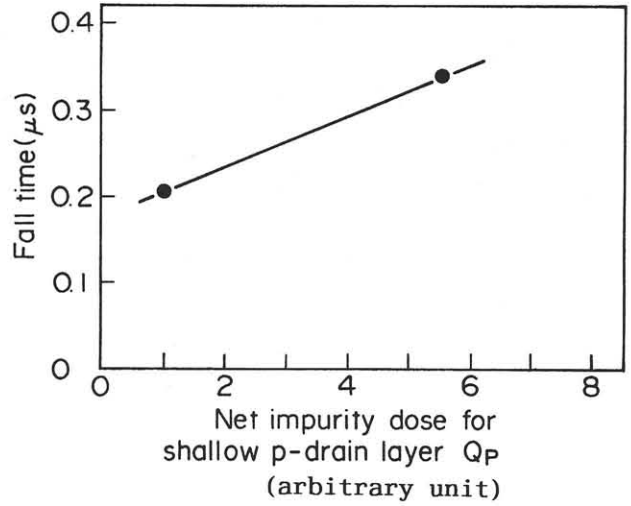


Fig.2 Fall time dependence on net impurity dose for shallow p-drain layer (Q_p)

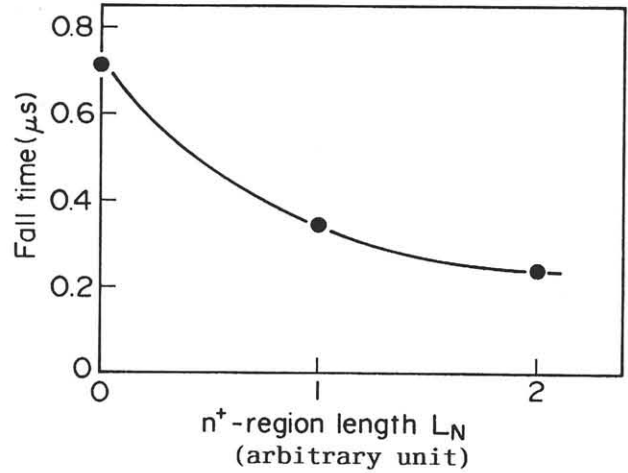


Fig.3 Fall time dependence on n^+ -region length (L_N)

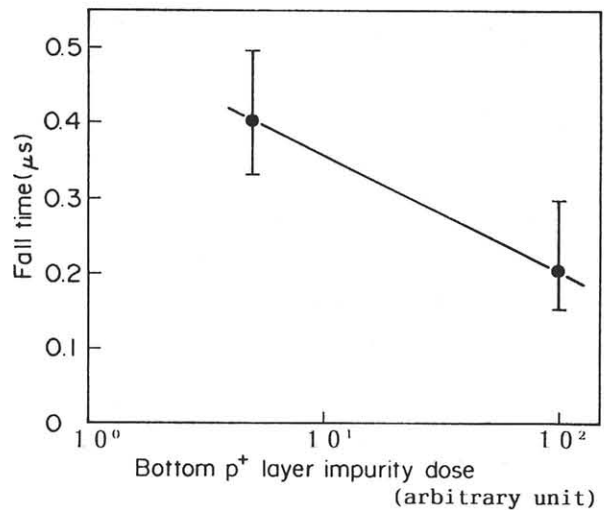


Fig.4 Fall time dependence on bottom p^+ layer impurity dose

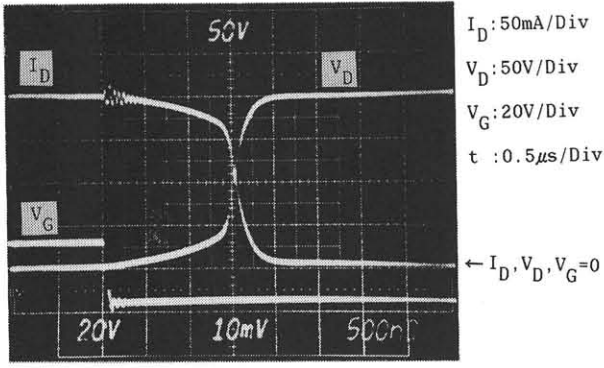


Fig.6 Turn-off waveform for conventional LIGBT with low impurity dose in n buffer

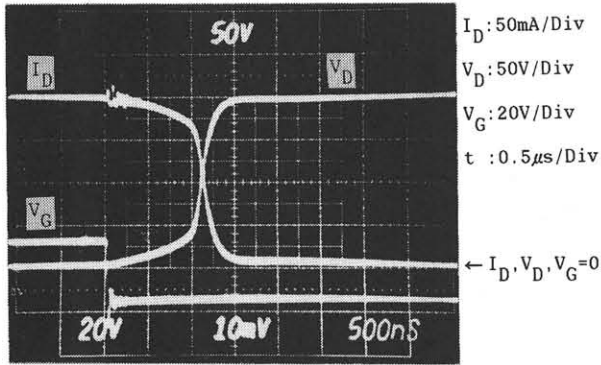


Fig.7 Turn-off waveform for conventional LIGBT with high impurity dose in n buffer

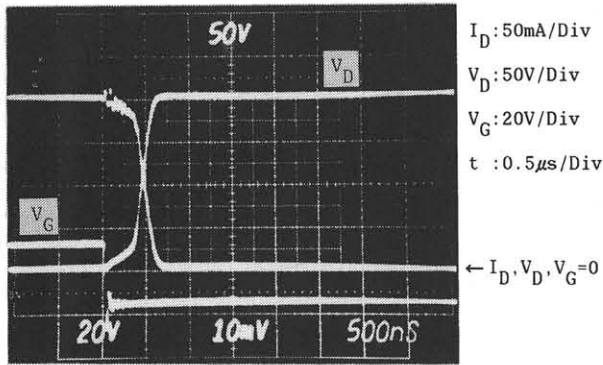


Fig.8 Turn-off waveform for newly developed LIGBT with same impurity dose in n buffer as LIGBT in Fig.6

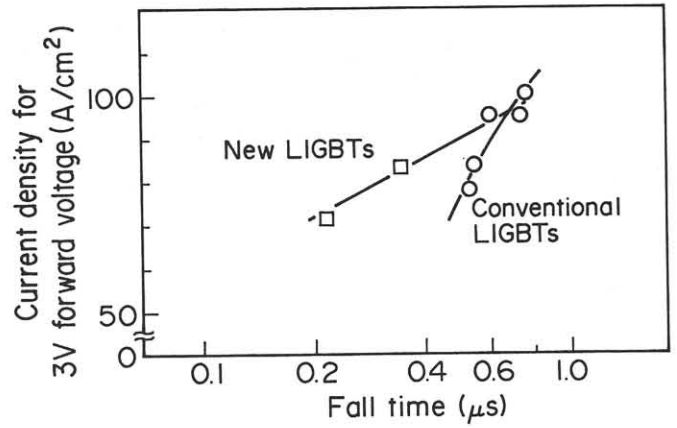


Fig.5 Trade-off relations between fall time and current density at 3 V on-state voltage for newly developed LIGBTs and conventional LIGBTs

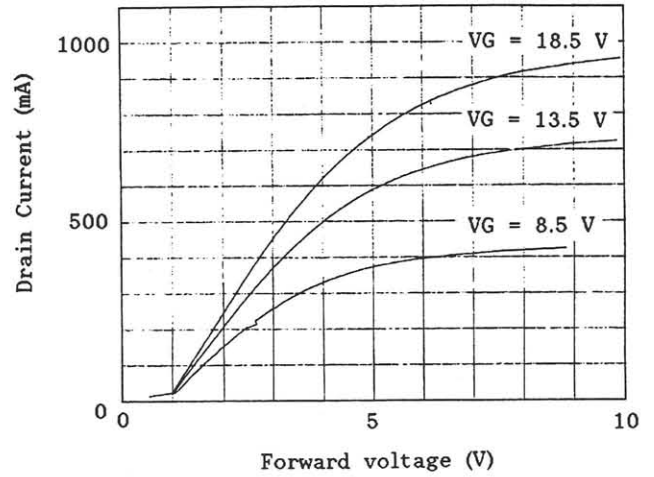


Fig.9 Current-voltage characteristics for newly developed LIGBT