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6000V Double Gate GTOs

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A double gate GTO, consisting of an n-buffer and a second gate on the n-buffer layer, has been developed. A forward blocking voltage of 6000 V was realized, even at 150 °C. Turn-off switching power loss can be reduced to approximately 1/20 of that for a single gate GTO with the n-buffer and anode short structure for an identical n-base width.

1. INTRODUCTION

High power gate turn-off thyristors (GTOs) have received much attention as key switching devices for high power inverters and choppers. It is desirable to develop higher power and higher switching frequency GTOs, to make these power systems smaller, and to improve energy conversion efficiency. The main problem in satisfying these requirement for the GTOs is a significant increase in on-state voltage and switching power loss, caused by the increase in n-base width. In order to attain high blocking voltage simultaneously with low switching power loss, various device structures have already been proposed [1)-4)]. The authors also have proposed a 6000 V GTO with a combination of an n-buffer and anode short structure [5)]. However, the maximum operational frequency, even at this GTO, is still limited to less than 1 kHz. In order to attain high blocking voltage simultaneously with low turn-off switching loss, a double gate GTO has been developed and evaluated. The device was fabricated on a 33 mm diameter silicon wafer, using conventional diffusion and PEP techniques.

2. EXPERIMENTAL RESULTS

2.1 Forward blocking characteristics

Generally, there are three GTO structure categories: reverse blocking, anode short and n-buffer structures. The n-buffer structure is the most suitable to achieve high frequency operation in high blocking voltage GTOs, because the n-base width for n-buffer structure is the narrowest in these three structures [5)]. Therefore, the double gate structure has been combined with the n-buffer, as indicated in Fig.1. A second gate is placed on the n-buffer layer. A forward blocking voltage of 6000 V was realized by a 550 μm n-base with the n-buffer, even at 150 °C, when the second gate was shorted to the anode electrode, as in Fig.2. This is because the hole injection from the p-emitter layer can be suppressed by shorting between the second gate and the

anode electrode. The maximum allowable junction temperature for conventional GTOs is 125 °C, so that a double gate GTO can operate at higher temperature than the conventional GTOs.

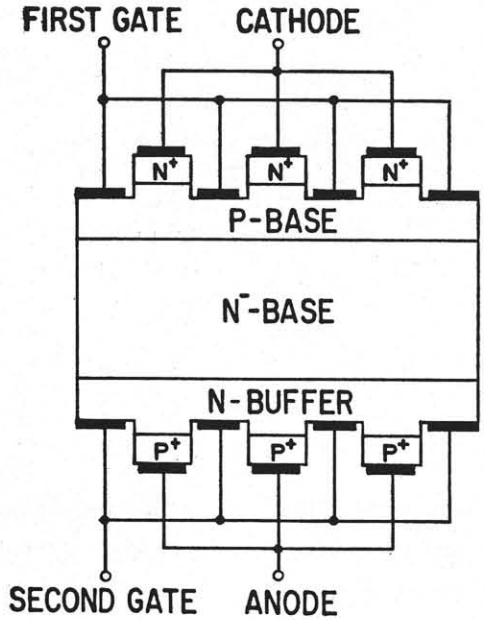


Fig.1 Cross-sectional view of double gate GTO.

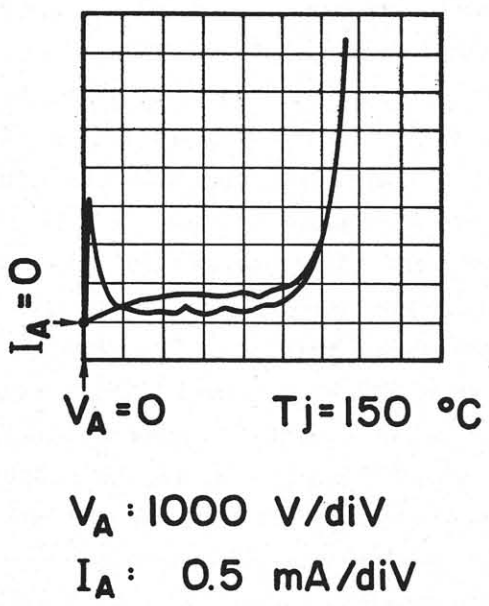


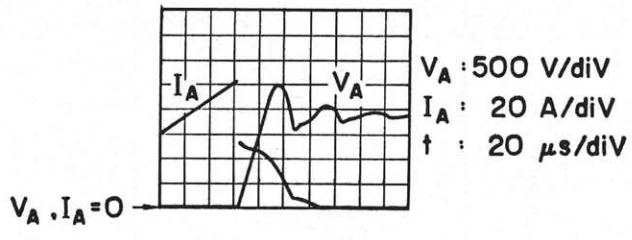
Fig.2 V-I characteristics at 150 °C for double gate GTO, when second gate was shorted to anode electrode.

2.2 Turn-off characteristics

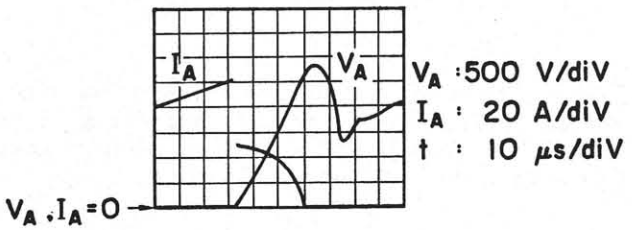
It was found that the turn-off switching loss can be greatly reduced by adjusting the time interval (Δt_G) between two turn-off gate pulse triggering times for the first and second gates. The turn-off waveforms for three Δt_G cases are shown in Figs.3 (a), (b) and (c), respectively. Figure 3 (a) shows the turn-off waveforms for anode voltage (V_A) and anode current (I_A), when only the first gate is reverse biased at turn-off period. Figure 3 (b) shows the turn-off waveforms when the first and second gates are simultaneously reversed biased. From a comparison between these two turn-off waveforms, it can be considered that the second gate does not operate effectively to reduce turn-off loss, in case of Fig.3 (b). The turn-off gain (G_{OFF}) for the second gate is given as

$$G_{OFF} = \frac{\alpha_{pnp}}{\alpha_{npn} + \alpha_{pnp} - 1}$$

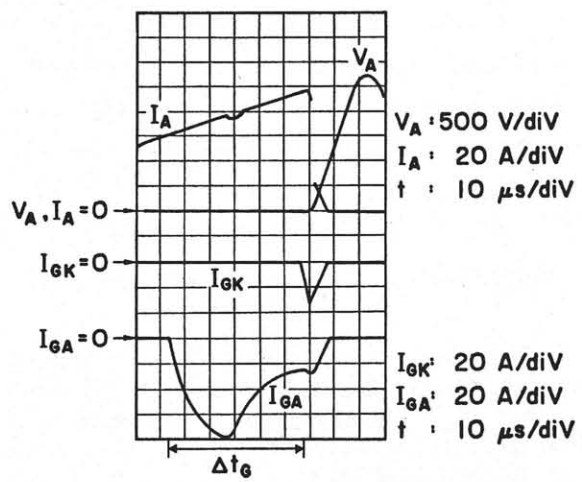
where α_{npn} and α_{pnp} are small-signal current gains for npn and pnp transistor portions of a unit GTO. Generally, α_{pnp} has a small value, compared with α_{npn}, because the n-base is wider than the p-base. Therefore, the turn-off gain for the second gate is smaller than that for the first gate, and the second gate does not have sufficient effect on reducing the turn-off loss, in case of simultaneously applying reverse bias (Δt_G=0 μs) to these two gates, as shown in Fig.3 (b). The turn-off waveforms for anode voltage, anode current, first gate current (I_{GK}) and second gate current (I_{GA}) for Δt_G=55 μs are shown in Fig.3 (c). It is clearly seen that the tail current is greatly reduced by adopting a large Δt_G, such as 55 μs. Figure 4 shows the relation between Δt_G and the peak value (I_{t1}) for the tail current. As is obvious



(a) Turn-off waveforms for anode voltage (V_A) and anode current (I_A), when only first gate is reverse biased.



(b) Turn-off waveforms for anode voltage and anode current, when first and second gates are simultaneously reverse biased (Δt_G =0 μs).



(c) Turn-off waveforms for anode voltage, anode current, first gate current (I_{GK}) and second gate current (I_{GA}) for Δt_G =55 μs.

Fig.3 Turn-off waveforms for double gate GTO.

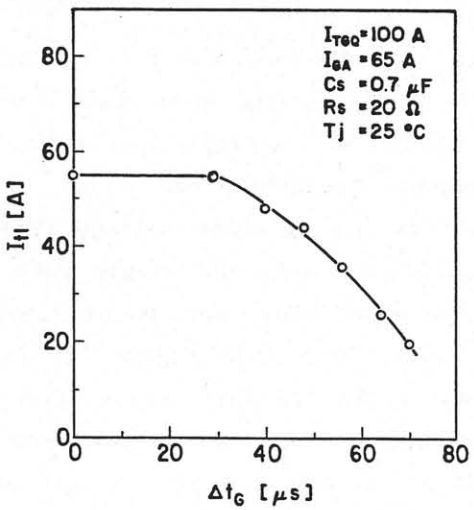


Fig.4 Peak value for tail current dependence on Δt_G for double gate GTO.

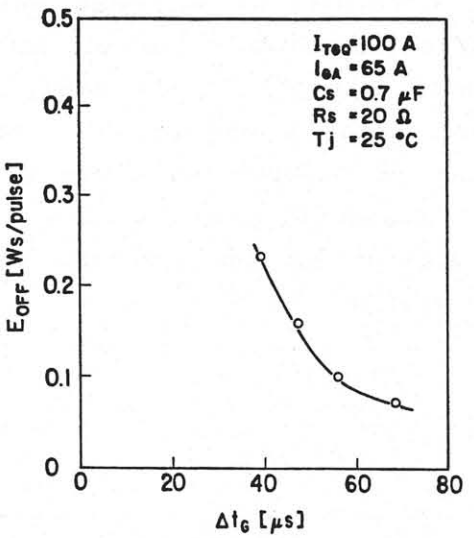


Fig.5 Turn-off switching loss (E_{OFF}) dependence on Δt_G for double gate GTO.

from this figure, I_{tl} can be reduced by increasing Δt_G. From these two figures, it can be concluded that the second gate can sweep away the excess carriers in the n-base during turn-off transient by adopting a large Δt_G. Turn-off loss (E_{OFF}) dependence on Δt_G is shown in Fig.5. This figure also shows that the turn-off loss can be reduced by increasing Δt_G.

2.3 On-state voltage and trade-off relation

The on-state voltage for the double gate GTO has compared with that for the single gate GTO. Figure 6 shows the experimental results for the n-base lifetime (τ_N) vs on-state voltage (V_T) for the double gate GTOs and single gate GTOs without an anode short portion of identical n-base width. From this figure, it can be concluded that the decreasing p-emitter area, caused by the second gate portion, does not affect the on-ststе voltage in the double gate GTO. Figure 7 shows a comparison in the trade-off relations for the on-state voltage and turn-off switching loss between the double gate GTO and the single gate GTO with n-buffer and anode short [5]. The turn-off switching loss is reduced to approximately 1/20 of that for the single gate GTO by the double gate structure. This is because the turn-off loss can be reduced by adjusting the interval between two gates, in spite of the second gate portion not affecting on the on-state voltage.

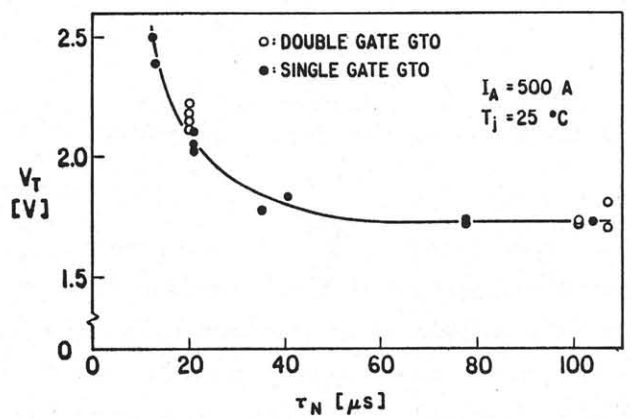


Fig.6 On-state voltage (V_T) dependence on n-base lifetime (τ_N) for double gate GTO and single gate GTO.

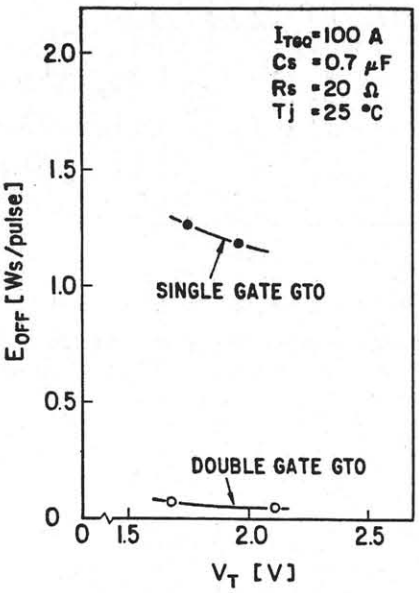


Fig.7 Trade-off relations between on-state voltage (V_T) and turn-off switching loss (E_{OFF}) for double gate GTO and single gate GTO with n-buffer and anode short.

3. CONCLUSION

The double gate GTO, consisting of the n-buffer layer and the second gate on the n-buffer, has been developed to achieve low turn-off loss in high blocking voltage GTOs. The forward blocking voltage of 6000 V was realized, even at 150 °C. The turn-off switching loss can be reduced to approximately 1/20 of that for the single gate GTO by adjusting times for the first and second gates.

4. REFERENCES

1) T.Nagano, M.Okamura and T.Ogawa: IEEE-IAS Annual Meeting Record (1978) 1003.
2) A.Tada, T.Miyajima, H.Hagino and M.Ishida: International Power Electronics Conf. Record (1983) 54.
3) K.Murakami, N.Itazu, Y.Uetake, K.Mase and M.Takeuchi: International Power Electronics Conf. Record (1983) 42.
4) M.Azuma, T.Shinohe, K.Takigami and H.Ohashi: 17th Conf. on Solid State Devices and Mater. (1985) 393.
5) T.Ogura, M.Kitagawa, H.Ohashi and A.Nakagawa: 19th Conf. on Solid State Devices and Mater. (1987) 63.