Extended Abstracts of the 20th (1988 International) Conference on Solid State Devices and Materials, Tokyo, 1988, pp. 33-36

500V Lateral Double Gate Bipolar-Mode MOSFET(DGIGBT) Dielectrically Isolated by Silicon Wafer Direct-Bonding(DISDB)

Akio Nakagawa, Yoshihiro Yamaguchi, Kiminori Watanabe

Toshiba Corporation

1 Komukai Toshibacho Saiwai-ku Kawasaki, 210 Japan

500V lateral double gate Bipolar-Mode MOSFETs(DGLIGBT) have been realized, for the first time, in N^- silicon islands, which are dielectrically isolated by Silicon Wafer Direct-Bonding. SIPOS resistive field plate successfully prevented the breakdown voltage reduction caused by overlying metal interconnection layers. The device fall-time was reduced to less than a half value by operating the second gate.

1. INTRODUCTION

Bipolar-Mode MOSFETs[1] (IGBTs[2]) have been recognized as excellent high voltage power devices because of their MOS gate controlled large current capability, simultaneously with a high switching speed and a large safe operating area(SOA). Lateral devices are also attractive as high voltage output devices for power ICs.[3),4)]

This paper presents (1)a double gate lateral device for high speed switching, (2)application of dielectric isolation by silicon wafer direct-bonding to a power device, for the first time, and (3)superiority of SIPOS resistive field plate as a junction termination technique for high voltage ICs.

It was numerically predicted by one of the authors that double gate operation in a Bipolar-Mode MOSFET improves trade-off relation between forward voltage and fall-time.[5),6)] This double gate structure was realized in a lateral device fabricated in a N type silicon island, which was dielectrically isolated by Silicon Wafer Direct-Bonding (DISDB[7),8)]) and V-grooves. Approximately 0.9mm² N^- silicon island was completely isolated by 1μm thick oxide film.

SIPOS resistive field plate combined with a metal field plate was adopted for junction termination to shield overlying metal interconnection layer influence on the breakdown voltage.[8)]

The created n-channel beneath the second gate serves as so called 'anode short' and inactivates the parasitic PNP transistor, thus, increasing device switching speed.

The developed DG device can be formed all by diffusions in a dielectrically isolated silicon island, thus, easily being implemented in power ICs and having complete process compatibility with CMOS logics and good noise immunity.

2. DIELECTRIC ISOLATION BY SILICON WAFER DIRECT-BONDING(DISDB) AND DEVICE FABRICATION

Silicon Wafer Direct-Bonding(SDB) technique was tested and applied to real devices independently by two groups in 1985[9)] and 1986.[7),10)] Recent successful

results were its applications to 1800V Bipolar-Mode MOSFETs,[10] (as an alternative to epitaxial wafer) and photodiode array.[7),11)]

In this chapter, first application of dielectric isolation technique based on SDB(DISDB) to a power device is described.

Figure 1 shows the fabrication process sequence for the DISDB.

1)First, an N-type diffusion layer is formed on one of the mirror surface of an N-type high resistivity bulk wafer. Then the surface is oxidized to create a more than 1μm thick SiO_2 layer.

2)This oxidized surface is directly bonded to a substrate wafer.

3)The thickness of the bonded N-type wafer on the SiO_2 layer is adjusted by the conventional lapping technique.

4)V-grooves are formed by the anisotropic etching technique to isolate silicon islands. The V-groove surfaces are heavily doped in phosphorus vapor and are oxidized again.

5)A polycrystalline silicon film is deposited, filling the V-grooves

7)Finally, the surface of the wafer is polished and the thichness of the N-layer is adjusted to be 50μm for 500V high voltage device.

Approximately 0.9mm^2 N^- silicon islands were dielectrically isolated by this method. More than 800V isolation voltage between a silicon island and the substrate was obtained.

Double gate lateral Bipolar-Mode MOSFETs(0.43mm^2 active region) were fabricated only by diffusions in the silicon islands. Basic designs for the diffusion depths and impurity profiles for the base and source layers are the same as those for the vertical devices. The three layers: the drain N^+-layer, drain P^+-layer and the N buffer were formed in a self-aligning manner by using the second gate polysilicon edge in order to easily control the threshould voltage for the second gate.

3. DOUBLE GATE LATERAL BIPOLAR-MODE MOSFET(DGLIGBT)

Regarding lateral IGBT, double gate structure is easy to be implemented in actual devices. Figures 2 and 3 show two basic N channel lateral IGBT structures. The difference is which conductivity type is chosen for the starting silicon island.

In this chapter, basic electrical characteristics for the fabricated DGLIGBTs in a dielectrically isolated N type silicon islands will be reported.

The electrical characteristics for the counterpart DGLIGBT in a P type silicon island was numerically analyzed and published in 1988 ISPSD.[6)]

3.1 500V BREAKDOWN VOLTAGE REALIZED BY SIPOS RFP TECHNIQUE

SIPOS resistive field plate(RFP[12)]) was shown to be a suitable passivation technique especially for high voltage power ICs,[8)] because not only it realizes a high breakdown voltage for a short source drain distance, but also it can prevent breakdown voltage reduction caused by overlying metal interconnection layers.

Figure 4 shows the top view of the fabricated device. Figure 3 also shows the RFP structure adopted in the present DGLIGBT. More than 500V can be obtained for only 65μm source to drain distance regardless of the source and gate interconnection layers over the SIPOS RFP.

The created anode short has an effect to increase the device breakdown voltage. Figure 5 shows that the device breakdown voltage increases from 270V to more than 500V when 15V gate voltage is applied to the second gate.

3.2 ELECTRICAL CHARACTERISTICS

In the double gate device in Fig.3, the first gate is used for an ordinary current control mean, whereas the second gate is for controlling the mode of the device operation by creating the N channel, which shunts the n-buffer and the N^+-layer in the p^+-drain layer.

Forward current voltage characteristics continuously change from bipolar-mode (15ohm on-resistance, 0.43mm^2 active region) to MOSFET-mode (115ohm on-resistance) as the second gate voltage changes from zero to 15V as shown in Fig.6.

The developed DG device has 120nsec storage time. By applying positive second gate bias and realizing effective 'anode short' a few microseconds before turning-off the device, the fall-time can be reduced from 2.0μs to 0.8μs as seen in Fig.7.

Switching time can be decreased also by decreasing the device carrirer lifetime (see Fig.8). However, this method causes an increase in device forward voltage drop and, thus, decreases the drain current for 3V forward voltage. Thus, double gate structure is effective to improve the device trade-off relation between forward voltage and turn-off time.

DG devices can also be operated in the reverse direction. This mode of operation might be utilized as inherent reverse conducting diodes.

The developed DG device can be formed all by diffusions, thus, easily being implemented in power ICs and having complete process compatibility with CMOS logics.

4.CONCLUSION

Double gate lateral Bipolar-Mode MOSFETs were successfully realized in dielectrically isolated N^- silicon islands by DISDB. 500V breakdown voltage could be obtained by SIPOS RFP technique. Fall-time was reduced to less than a half of the original value by operating the second gate.

REFERENCES

1)A.Nakagawa et al, Ext.Abs.of 16th ISSDM, p.309(1984)
2)B.J.Baliga et al, 1982 IEEE IEDM Tech. Dig.,p.264.
3)M.R.Simpson et al, 1985 IEEE IEDM Tech. Dig.,p.740.
4)A.L.Robinson et al, 1985 IEEE IEDM Tech. Dig.,p.744.
5)A. Nakagawa, 1988 IEEE PESC Record, p.84.
6)A. Nakagawa, to appear in Proc. of 1988 Int.Symp.on Power Semicon.devices.
7)H.Ohashi et al, 1986 IEEE IEDM Tech Dig., p210.
8)A. Nakagawa, 1988 IEEE PESC Record, p.1325.
9)J.B.Lasky et al, 1985 IEEE IEDM Tech. Dig.,p.684.
10)A. Nakagawa, 1986 IEEE IEDM Tech. Dig., p.122.
11)J. Ohura et al, IEEE Electron Device Lett.,p.454(1987)
12)K.Watabnabe et al, Trans.IECE Japan, E69,p.246(1986)

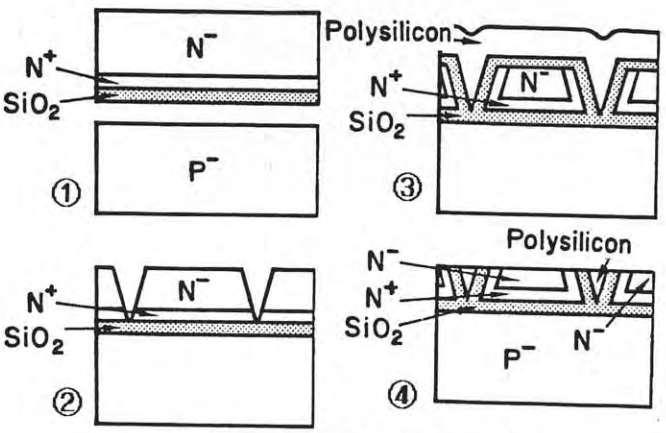

Fig.1 DI wafer fabrication process.

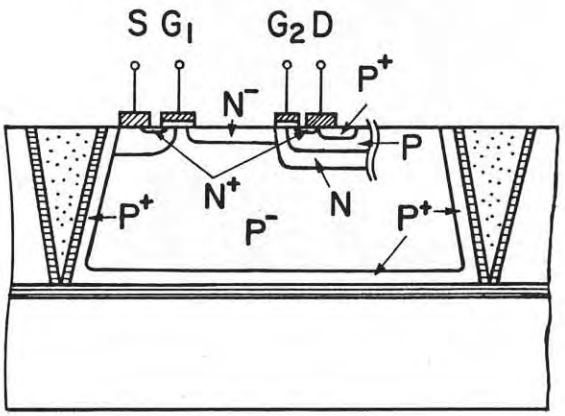

Fig.2 Lateral N-channel double gate device in a P type silicon island.

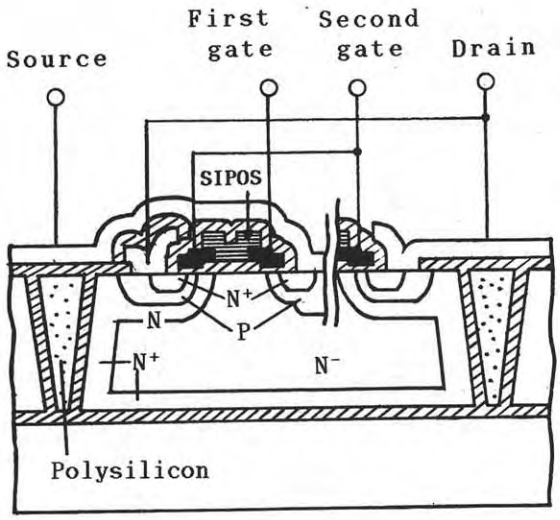

Fig.3 Lateral N-channel double gate device in a N type silicon island.

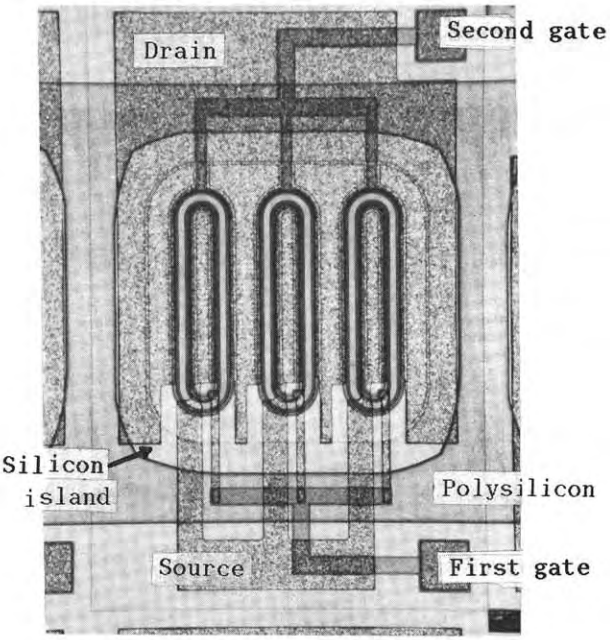

Fig.4 Top view of the fabricated DG device.

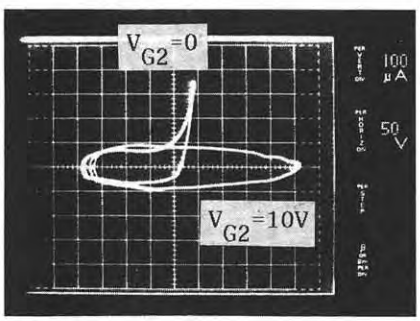

Fig.5
Breakdown voltage was increased above 500V as V_{G2} increases.

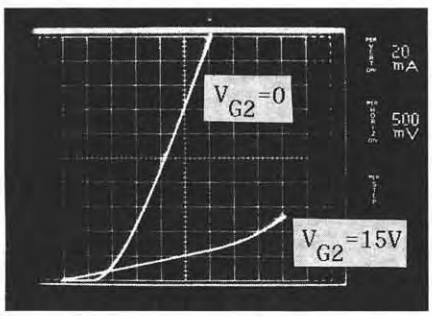

Fig.6
Current-voltage characteristics for bipolar-mode operation(V_{G1}=15V,V_{G2}=0V) and MOSFET operation (V_{G1}=15V,V_{G2}=15V).

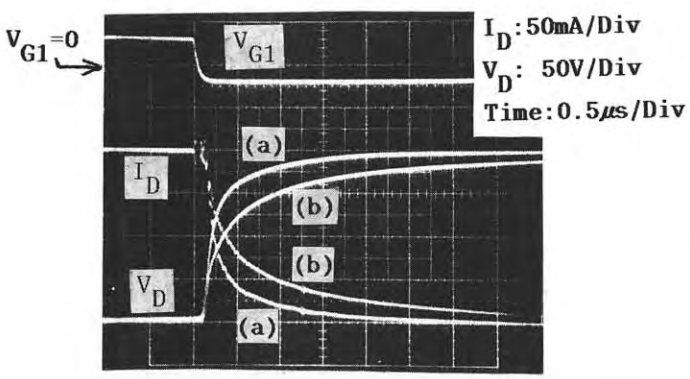

Fig.7 Turn-off characteristics.
(a)15V second gate voltage is applied 1μs before turning-off the first gate. (b)Second gate voltage is kept zero.

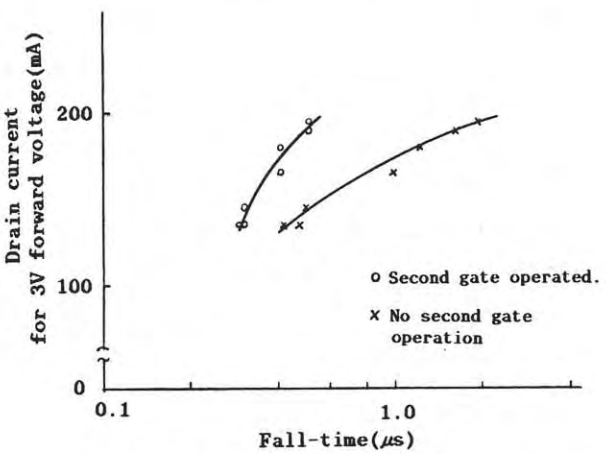

Fig.8 Modified trade-off relation between drain current for 3V forward voltage and fall-time