

An NPN Transistor Fabricated by Silicon Wafer Direct-Bonding

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Transistors were fabricated by Silicon Wafer Direct-Bonding(SDB) technique to investigate their minority carrier transport characteristics through a bonded interface, made inside the p-base. Fabricated transistors exhibited sufficiently large current gains(10), although minority carrier lifetime for the p-base was apparently decreased by the existence of the bonded interface.

1. Introduction

Silicon Wafer Direct-Bonding (SDB) is a new technique which makes it possible to bond a pair of silicon wafers without any other material. A variety of SDB technique applications are foreseen for power devices or sensors. A bonded interface between heavily doped wafers shows good ohmic characteristics[1]. The 1800V Bipolar-Mode MOSFET (IGBT) is the first application, taking advantage of these ohmic characteristics for the bonded interface[2]. The SDB technique could possibly be used to realize new devices which could not be realized by ordinary process techniques, if it can be successfully applied in the active regions inside the device. For example, impurity profiles in the base regions for a transistor or a Gate turn-off thyristor (GTO) can be improved.

This paper first reports the resistance of the bonded interface in the p-type substrate being measured. Second, NPN transistors, which have a bonded

interface inside the p-base, were fabricated and evaluated in respect to current amplification factors. The bonded interface influence on minority carrier transport was investigated by comparing the measured results with numerically simulated results.

2. Bonded interface resistance measurement

First, the resistance of the bonded interface between the two heavily doped silicon wafers was measured. Table 1 shows specifications for the bonded silicon wafers. Silicon wafer surfaces were cleaned and directly bonded according to the SDB prescriptions. At this time, the orientation flats for the two wafers were brought together so that they would coincide with each other. SDB process was completed by thermal annealing at more than 1000°C. Al electrodes were then evaporated on both surfaces of the wafer, which finally was cut into 6mm square chips (see Fig.1). Sample(A/A) means that the sample was fabricated from the same

two A wafers. Current voltage(I-V) characteristics were measured by the four-probe method to estimate the bonded interface resistance. Figure 2 shows the relation between the resistances for the bonded samples and single wafer samples A and B vs. their wafer thicknesses. Bonded wafers thicknesses are 900 μm and 700 μm , respectively. The resistance for the bonded interface can be estimated from this figure, because the difference between the resistance for a bonded sample and twice the resistance for a single wafer sample should be attributed to the resistance for the bonded interface. As the bonded interface resistance for a unit area is 0.03~0.1 $\Omega\cdot\text{cm}^2$ (see Table 2), forward voltage drop across the interface is negligibly small, even for a high current density level.

3. Transistor characteristics evaluation

Crystal defects and impurities, such as oxygen atoms, were found to exist at the bonded interface[1]. A bonded interface, formed in the active area of the device, may cause a carrier lifetime decrease. NPN transistors were fabricated by the process shown in Fig.3 to investigate the bonded interface effect on carrier lifetime reduction. Specifications for the wafers used for transistor fabrication are shown in Table 1. Figure 4 shows the transistor structure and the impurity doping profile for the fabricated NPN transistors. Figure 5 shows detailed three impurity profiles near the p base, where W_{p1} is the distance between the n emitter-p base junction and the bonded interface. Figure 6 shows a typical emitter grounded collector current(I_c) vs. collector-emitter voltage(V_{ce}) characteristics. Current gain h_{FE} was about 10. It was confirmed that anyhow, minority

carriers can pass through the bonded interface. Figures 7 and 8 show the collector current density(J_c) dependence on h_{FE} at $V_{ce}=5V$ and 50V, respectively. The collector current density, corresponding to the onset of base push-out(J_0), is 0.8 or 1 A/cm^2 at $V_{ce}=5V$ and 7 A/cm^2 at $V_{ce}=50V$. The following equation is applicable in the low bias condition[3].

$$J_0 = \frac{|V_{cb}|}{\rho_c \cdot W_c},$$

where V_{cb} is the applied collector-base voltage, ρ_c and W_c are collector layer resistivity and width, respectively. Since W_c is approximately 670 μm , the experimentally obtained J_0 values are reasonable, according to this equation. Figure 9 shows the W_{p1} dependance on base grounded current gain α_{nnp} values at $J_c=0.05\text{A}/\text{cm}^2$ and 5 A/cm^2 , respectively. This figure indicates that α_{nnp} decreases with the increase in W_{p1} . This is assumed to be caused by the difference in the p base profile as well as in the bonded interface characteristics.

The bonded interface influence on the minority carrier was investigated by using numerical device simulator TONADDE I, which solves fundamental semiconductor equations in one dimension and includes effects of band-gap-narrowing, SRH recombination and Auger recombination[4]. In conventional transistors, which have almost the same p base profile, the calculated h_{FE} value agrees well with experimental values, when 5 to 10 μsec carrier lifetime values τ_L for the n emitter and the p base are assumed. On the other hand, 0.5 μsec has to be assumed for the τ_L value to obtain agreement between experimental results and calculated values (see Fig.10).

4. Conclusion

The measured resistance for the bonded interface was 0.03 to 0.1 $m\Omega \cdot cm^2$. This value is negligibly small for device application. The carrier lifetime for the p base made by SDB was found to range from 0.5 to 1 μsec . This value seems to be small, compared with that for the conventional NPN transistors. However, it was found that minority carriers can pass through the bonded interface and NPN transistors exhibit sufficiently large current gains. Thus, better transistors will be fabricated by improving the bonded interface characteristics.

Reference

- [1] K.Furukawa, M.Shimbo, K.Fukuda and K.Tanzawa, 18th Conf. Solid State Devices and Mater., p.553, 1986
- [2] A.Nakagawa, Y.Yamaguchi, K.Watanabe, H.Ohashi, and M.Shimbo, 18th Conf. Solid State Devices and Mater., p.89, 1986
- [3] R.J.Whittier and D.A.Tremere, "Current gain and cutoff frequency fall-off at high currents", IEEE Trans. Electron Devices, vol.ED-16, p.39, Jan. 1969
- [4] A.Nakagawa, M.Kurata, IEEE Trans. Electron Devices, vol.ED-28, p.231, 1981

Sample	A	B	Transistor
Type	P FZ	P FZ	N FZ
Impurity	Boron	Boron	Phosphorus
Resistivity($\Omega \cdot cm$)	2.28×10^{-3}	3.02×10^{-3}	140 ~ 170
Thickness(μm)	450	350	730 ± 10
Diameter (inch)	3	3	3
Orientation	(1 1 1)	(1 0 0)	(1 1 1)

Table 1 Wafer specification for the experiments.

Sample	A/A	B/B
Bonded interface resistance for 1 cm^2 area ($m\Omega \cdot cm^2$)	0.034	0.113

Table 2 Measured bonded interface resistance for two samples.

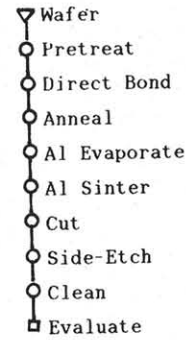


Fig.1 Process sheet for sample measurement bonded interface resistance.

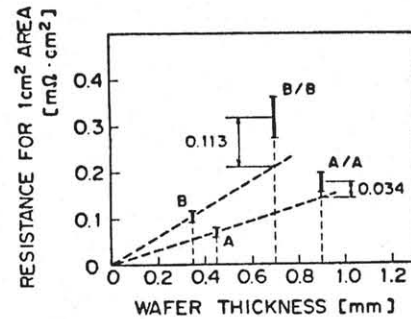


Fig.2 Relation between wafer thickness and sample resistance.

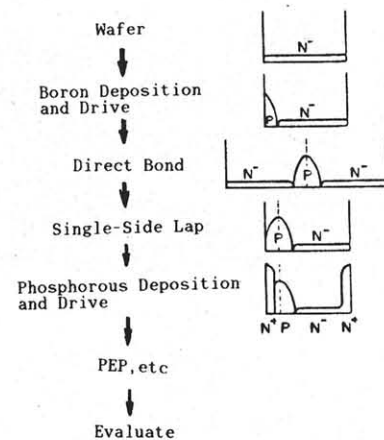


Fig.3 Process sheet for sample transistor fabrication and impurity profile.

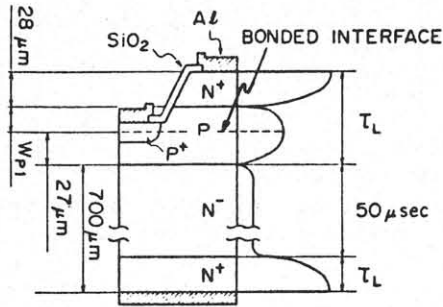


Fig. 4 Structure, impurity doping profile and lifetime for NPN transistor numerical calculation

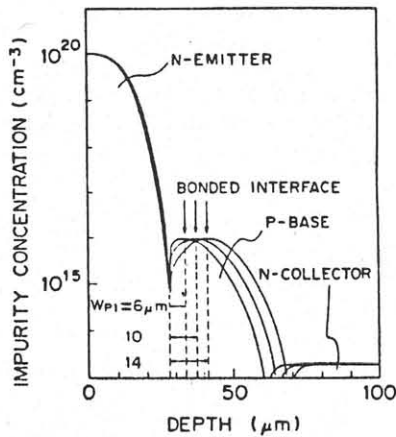


Fig. 5 Transistor sample impurity profile.

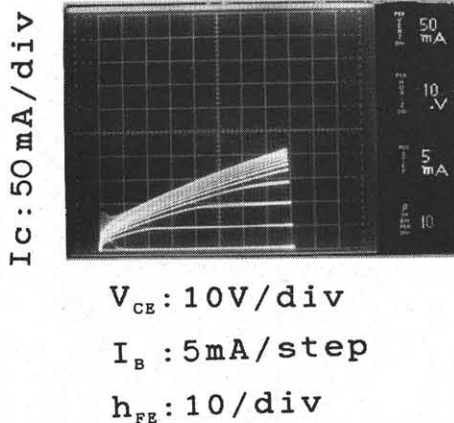


Fig. 6 Emitter grounded I_c vs. V_{ce} characteristics for a sample transistor.

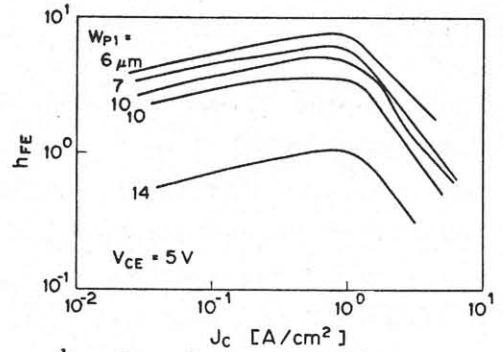


Fig. 7 h_{FE} dependence on collector current density.

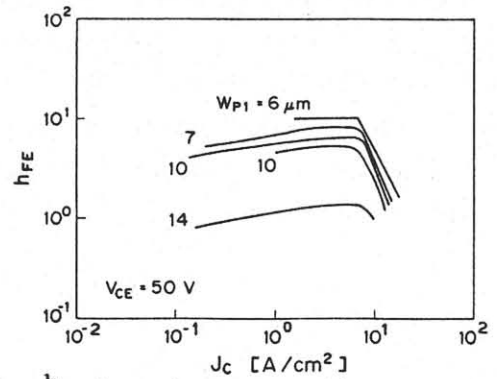


Fig. 8 h_{FE} dependence on collector current density.

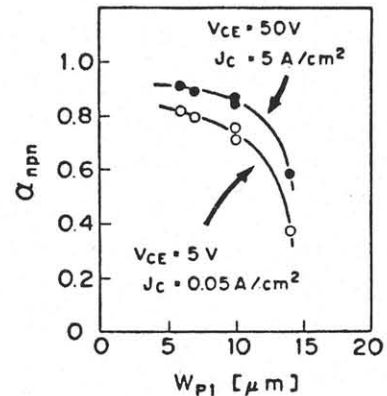


Fig. 9 Relation between W_{p1} and α_{npn} (Experimental values).

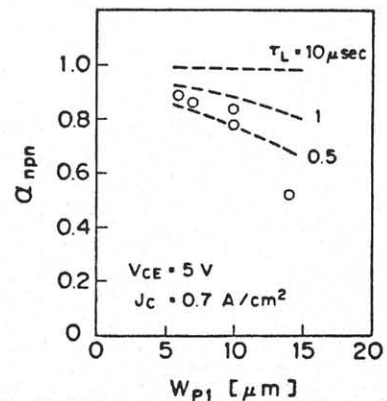


Fig. 10 Relation between W_{p1} and α_{npn} (O: experimental values, dash line: Calculated values).