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Improved Bipolar-Mode MOSFETs(IGBT) with Self-Aligning Technique and Wafer Bonding(SDB) —Why is the Bipolar-Mode MOSFET SOA Large?—

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Short-circuited safe operating area for 1400V sustaining voltage Bipolar-Mode MOSFETs exceeded 1100V for 10μsec pulse operation at 125℃ if self-aligned deep P^+-diffusion and a hole bypass structure were implemented. Trade-off relation could be improved by adopting a thinner N-base and taking advantage of crystal defects at the bonded interface to reduce hole injection efficiency. Allowable power dissipation reached $5x10^5 W/cm^2$, which is greater than the theoretical limit for npn bipolar transistors. Numerical analysis predicts that the channel electron current will play an important role in achieving a large SOA, if electron current still exists even when the anode voltage reaches its peak.

1. Introduction

The Bipolar-Mode MOSFET[1] is a new power device, capable of switching a large current at high speed by a MOS-gate.

At the 1986 IEDM, the authors presented a new process for forming a self-aligned deep P^+-diffusion layer within a P-base[2]. This paper reports that the short-circuited SOA for 1400V sustaining voltage devices exceeded 1100V for a 10μsec pulse operation at 125℃ if the self-aligned deep P^+-layer and an optimum device design are implemented. The measured current voltage product for the SOA limit exceeded the theoretical limit for npn bipolar transistors. The reason was investigated by a device simulator TONADDEII[3].

2. Device design for 1400V sustaining voltage

In order to reduce the forward voltage, thinner N-base width was adopted, compared with that for the 1800V devices[2]. The static breakdown voltage was reduced to 1600V. However, the sustaining voltage was kept the same, 1400V, by adopting an optimized N-buffer/P^+-drain condition, which will be described in detail.

Figure 1 shows the adopted silicon wafer direct-bonding(SDB) process[2,4]. If the P^+-substrate is directly bonded to the N^+-buffer surface without forming the shallow P^+-layer prior to wafer bonding, bipolar-mode operation in the MOSFET hardly took place, because a large number of defects exist around the bonded interface. The key point for the present SDB process is to form a shallow and relatively low impurity concentration layer prior to wafer bonding.

By reducing the amount of impurity dose for the shallow P^+-layer, hole injection efficiency can be reduced by taking advantage of crystal defects at the interface. This results in improvement in the trade-off relation between farward voltage and fall-time.

1400V sustaining voltage can be attained by adopting a more heavily doped N^+-buffer even if the N-base width is reduced.

One disadvantage in the conventional epitaxy is that abnormally high forward voltage appears even for relatively low current density level for devices with an N^+-buffer, as seen in Fig.2, when carrier lifetime is small. This problem never appeared for devices on SDB wafers.

3. Short-circuited SOA[5]

Figure 3 shows a newly developed self-aligning process (see [2] for details) for a deep P^+-diffusion within the P-base layer. The safe operating area can be improved by adopting either deep P^+-diffusion, hole bypass, stripe pattern[6] or N^+-buffer.

Figure 4 shows the effects of deep P^+-diffusion and hole bypass on short-circuited SOA. It is seen that the maximum allowable current simply increases by adopting hole bypasses or a self-aligned deep P^+-diffusion.

Figure 5 shows typical waveform for the short-circuited SOA measurement[5]. Allowable power dissipation for a 10μsec pulse operation reached 5×10^5W/cm^2 at 125℃ ambient temperature.

4. 2-d Model Analysis on why the Bipolar-Mode MOSFET SOA is large.

Inductive turn-off waveforms were closely analyzed by a device simulator TONADDEII. Figure 6 shows the analyzed 600V device structure and the outer circuit. Figure 7 shows one of typical calculated turn-off waveforms. Electron and hole carrier lifetimes for the high resistivity region were assumed to be 0.13μsec. Gate voltage was decreased from 12.5V to 0V in 0.1μsec.

As the gate voltage decreases, the device resistance simply increases. Channel electron current flows only under the gate electrode, as seen in Fig.8, after the anode voltage begins to recover. Thus, conductivity modulation occurs in the depletion layer only under the gate electrode region, where both electron and hole current flow. On the other hand, in the depletion layer beneath the P-base region, all of the current is carried by holes. This situation is seen in Fig.9. While channel electron current exists, the hole current density flowing up into the P-base is lower than average current density, because most of the current flows in the conductivity modulated area under the gate electrode.

After channel electron current completely ceases, all of the current is carried by holes and hole curent density beneath the P-base becomes greater than average current density (see 300V case in Fig.9). Thus, it is predicted that SOA will become greater as the total P-base area becomes larger for a unit device area.

Another important conclusion is that if the device resistance is sufficiently large, channel electron current still exists even after anode voltage has recovered to the electric source voltage level. This situation is realized for the cases of low carrier lifetime or low hole injection efficiency or for the cases where most of the current is carried by electrons. In addition, a slow dV_G/dt driving condition is effective.

Figure 10 shows this example. dV_G/dt rate is reduced to one forth of that for Fig.7 and carrier lifetime is reduced to 0.1μsec. Figure 11 shows current density distribution for a time step when anode voltage has just reached 200V. Hole current density beneath the P-base is only a half of the average current density (=122A/cm^2). Hole and electron density distributions corresponding to Fig.11 are shown by the curves A in Fig.12. Maximum electric field appears where the arrow indicates. If avalanche breakdown is determined by the positive charge density beneath the P-base, apparant power dissipation can exceed the theoretical limit, as long as the channel electron current still exists when the anode voltage reaches its peak value in the turn-off transient.

Figure 12 also shows the opposite case (curve B), where no channel electron current exists.

It should be pointed out that if the dV_G/dt rate is too steep, device resistance change cannot respond, because a large amount of excess carriers have to be removed.

If it is assumed that avalanche breakdown occurs beneath the P-base, the allowable maximum voltage V_{BD} is given by:

$$V_{BD}=60(E_G/1.1)^{1.5}([N_D+p]/10^{16})^{3/4}.$$

$$=60(E_G/1.1)^{1.5}\{[N_D+\frac{I_D-(1+\alpha)I_{ch}}{qv_sS}]/10^{16}\}^{3/4}$$

where S is the effective P-base area, Ich the channel electron current and α the factor which takes into account the enhanced hole current density under the gate electrode due to the conductivity modulation. Thus, power dissipation can exceed the pnp transistor theoretical limit unless Ich is zero.

5. Conclusion

1100V short-circuited SOA has been attained in 1400V sustaining voltage Bipolar-Mode MOSFETs. Numerical analysis predicted that the existence of the channel electron current after the anode voltage has recovered is effective for a large SOA.

References

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[2]A.Nakagawa et al, 1986 IEDM Tech.Dig. p.122

[3]A.Nakagawa et al, to be published in Proceedings of NASECODE V

[4]M.Shimbo et al, Ext.Abs. 69th Electrochem Soc. Meeting, p.337(1986)

[5]A.Nakagawa et al,IEEE Trans.Electron. Devices, ED-34, p.351(1987)

[6]A.Nakagawa et al, IEEE Electron. Device Lett. EDL-6, p.378(1985)

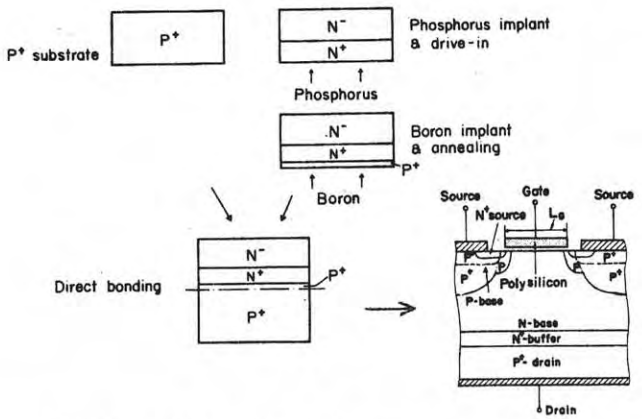

Fig.1 Si Wafer Direct-Bonding process and device structure

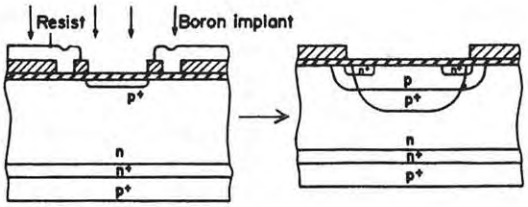

Fig.3 New self-aligning process for a deep P^+-diffusion layer

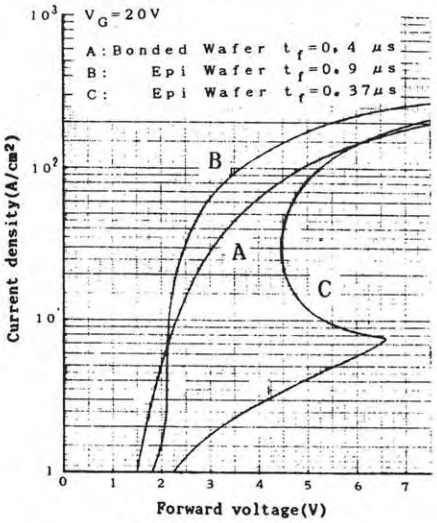

Fig.2 Current voltage characteristics comparison between Epi-wafer and SDB-wafer.

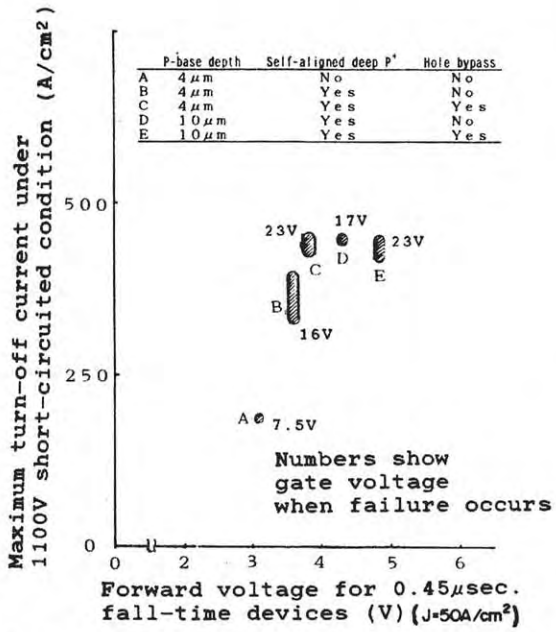

Fig.4 Short-circuit SOA(125℃) vs.forward voltage for 0.45μsec. fall-time devices. Maximum current density was limited to 450A/cm² because the peak voltage at turn-off transients exceeded the sustaining voltage.

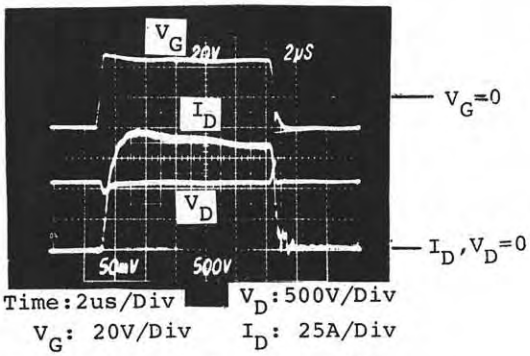

Fig.5 Typical waveform for 125℃ short-circuited SOA measurement. The 1100V anode voltage is continuously applied. The device active region is 20mm².

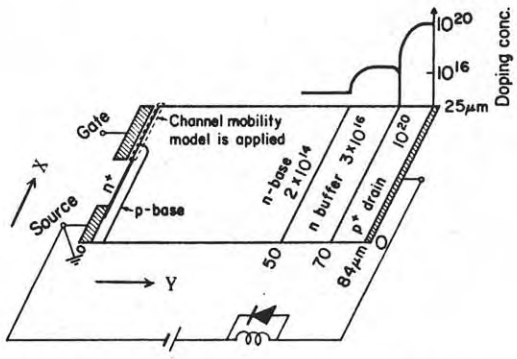

Fig.6 Analyzed 600V device structure and outer circuit configuration.

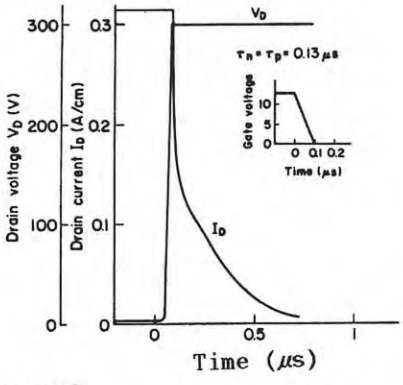

Fig.7
Calculated inductive turn-off waveforms.(0.13μs carrier lifetime)

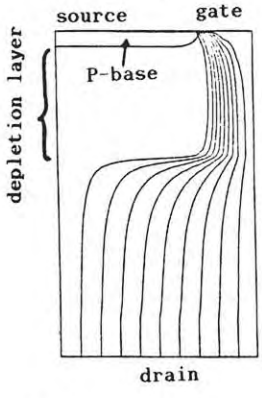

Fig.8
Channel electron current flow line for 183V drain voltage.

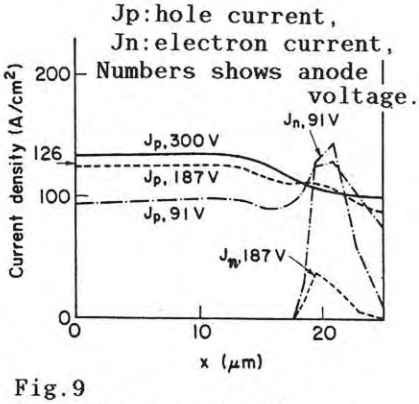

Fig.9
Distribution of hole and electron current density crossing y=6.6μm line, corresponding to Fig.7, with anode voltage as a parameter.
Average current density= 126A/cm².

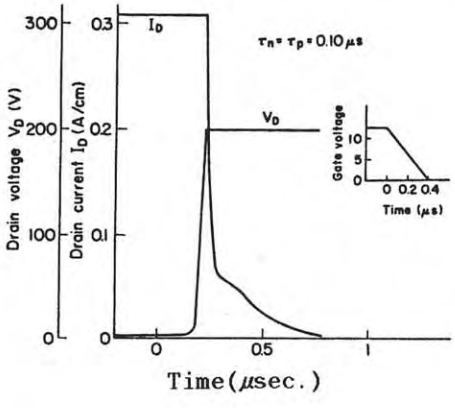

Fig.10
Calculated inductive turn-off waveforms.
(0.1μs carrier lifetime)

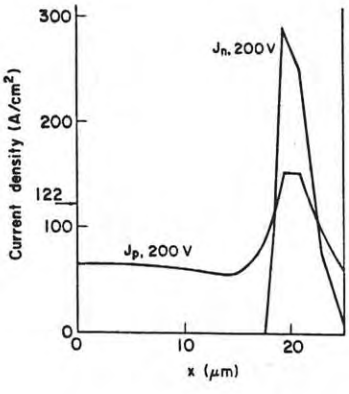

Fig.11
Hole and electron current density crossing y=6.6μm line vs. x-axis when anode voltage just has become 200V.
Average current density= 122A/cm².

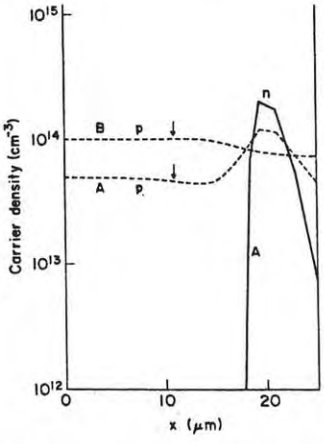

Fig.12
Carrier density distribution on y=6.6μm line. Curves A correspond to Fig.11. Solid and broken lines denote electron and hole density, respectively.