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High Voltage Bipolar-Mode MOSFET with High Current Capability

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1200V and 600V 100A bipolar-mode power MOS FETs(BIFET) have been developed in 6 mm square chips. 1200V BIFETs turn-off more than 75 Amps drain current within 2usec at 125°C. High current handling capability could be obtained by an optimized source-gate pattern and an additional shallow p+ base diffusion. It was comfirmed that a low on-resistance with a high blocking voltage can be attained in BIFETs more easily than in bipolar transistors.

1. INTRODUCTION

On-resistance for high voltage power MOS FETs is limited by the high resistivity n^--layer resistance. Operating current density for 1000V power MOS FETs is as low as 10-20 Amps/cm^2 for 3V drain voltage. This drawback is removed by introducing bipolar-mode operation in the MOS devices. One of the proposed structures for such devices(called IGT[1] or COMFET[2]) is very similar to that for a MOS thyristor. Source and base layers are short-circuited so that the thyristor action can be prevented up to a sufficiently high current density level. Drain current can be controlled by the gate electrode, like a MOS FET. Minority carrier injection from the p^+ drain modulates the high resistivity n^- layer resistance to less than a tenth of that of the corresponding power MOS FET. However, it was reported that maximum gate controllable current decreases with temperature. Devices developed thus far could handle only a small current at 125°C. The present paper presents 1200V 100A BIFETs(bipolar-mode MOS FETs), which retain gate controllability up to 100 Amps at 125°C.

2. MAXIMUM CONTROLLABLE CURRENT (LATCH-UP CURRENT)

Gate controllability for BIFETs is restricted by the latch-up phenomena of the parasitic thyristor. This section reports the results of an investigation on optimum source-gate pattern and vertical structure for preventing latch-up phenomena. 3mm square chip test devices were fabricated with various stripe source-gate patterns. Figure 1 shows a cross section of a BIFET and defines gate width:L_G and source width:L_S. Channel regions were fabricated by the diffusion self-align technique(DSA). Maximum

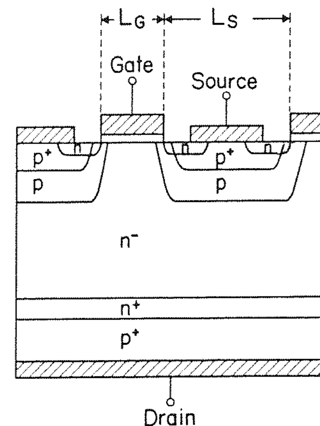
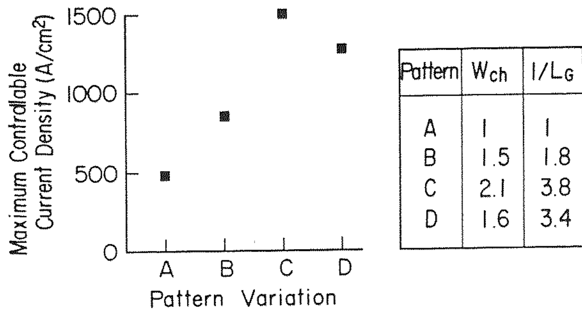


Fig.1 Cross section of a BIFET

controllable current density level(latch-up current density) was greatly affected by the source-gate pattern. The largest controllable current density was observed in the narrowest L_S pattern C(see Fig.2). It was interesting that pattern D had a larger controllable current density than pattern B, although the two patterns had almost the same total channel width. If all of the hole current flows only under the channel region and the gate oxide layer, latch-up current density should depend on the total channel width.

$$J_L \propto W_{ch} \propto 1.0/(L_S+L_G) \quad \text{..........(1)}$$

On the other hand, if the hole current flows uniformly, latch-up current density should be in inverse proportion to the gate width L_G. The latter relation is analytically derived in the following. A part of hole current, which flows up



Pattern	W_{ch}	$1/L_G$
A	1	1
B	1.5	1.8
C	2.1	3.8
D	1.6	3.4

Fig.2 Maximum controllable current density vs. pattern variation. The inserted table shows a comparison in total channel width W_{ch} and the inverse of gate width $1/L_G$ for each pattern. Total active area is the same for each pattern.

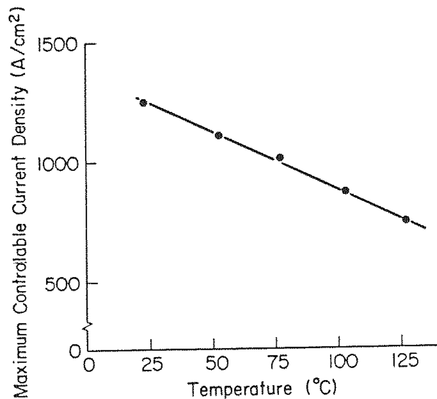


Fig.3 Temperature dependence of latch-up current density.

from the drain to under the gate oxide, flows into the base layer beneath the source layer and biases the base-source junction. This part of the hole current is roughly given for a unit channel length as:

$$I_b = L_G \, J_p, \quad (J_p\text{:hole current density}) \qquad \text{..........(2)}$$

which causes voltage drop V_b in the base layer beneath the source layer:

$$V_b = R_b \, I_b, \quad (R_b\text{:resistance of the base for a unit length}) \qquad \text{..........(3)}$$

If the latch-up occurs when V_b becomes equal to the built-in voltage of the source-base junction V_{bi}, latch-up current density J_L is expressed for the steady state case as:

$$J_L = J_p/\alpha_p = V_{bi}/(\alpha_p \, L_G \, R_b). \qquad \text{...(4)}$$

In the turn-off transient, all of the current is carried by holes because the channel is gone. Then, J_L is given by

$$J_L = V_{bi}/(L_G \, R_b), \qquad \text{........(5)}$$

The experimental data obtained for the turn-off transient is for between the two extreme cases: (1) and (5).

In order to increase controllable current density level, low p-base sheet-resistance (low R_b) is inevitable. An additional shallow p^+ diffusion enables reducing the base resistance, which is sufficiently close to the channel region. Figure 3 shows the temperature dependence of maximum controllable current density for the test devices.

3. TRADE-OFF BETWEEN TURN-OFF TIME AND FORWARD VOLTAGE DROP

It was reported[1] that electron irradiation technique reduces turn-off time to less than 200nsec at the cost of forward voltage drop. Turn-off time can also be reduced by decreasing minority carrier injection efficiency for the p^+-drain. Inserting a heavily doped n^+-layer between n^--base and p^+-drain improves switching speed without deteriorating high current density characteristics as shown in Fig.4. Figure 5 shows a comparison between the two techniques. It was found that addition of heavily doped n^+-layer improves forward voltage by 15%.

Heavy metal diffusion is an alternative method for electron irradiation. It was observed that excessive platinum diffusion deteriorates latch-up current density level and that the on-resistance shows negative temperature coefficient.

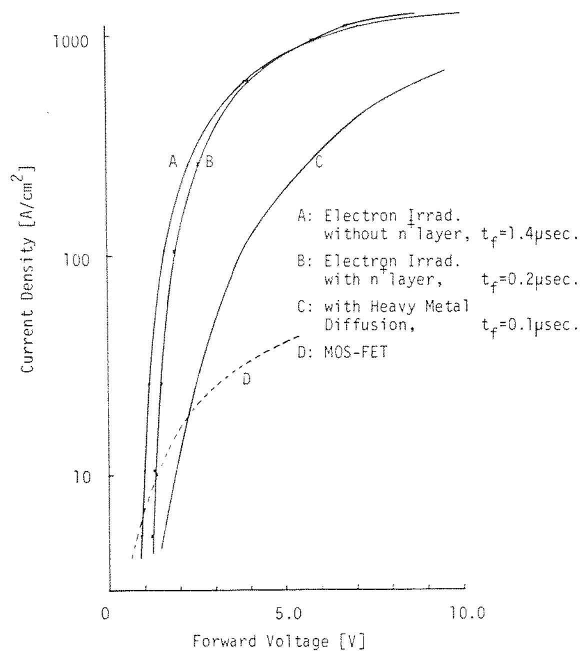


Fig.4 n^+-layer between p^+-drain and n^--base improves switching speed without deteriorating high current density characteristics.

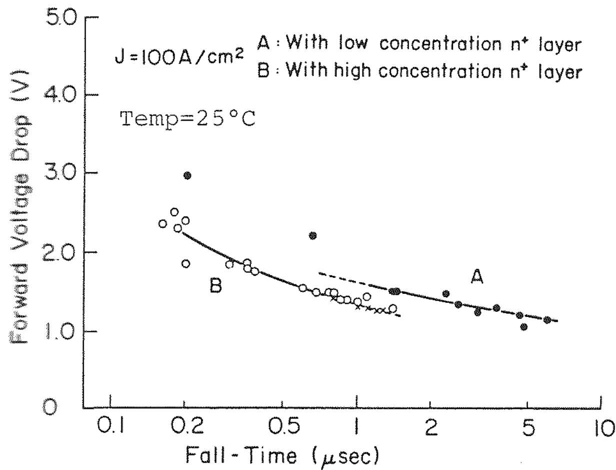


Fig.5 Trade-off between forward voltage drop and fall-time, wherein carrier lifetime is controlled by electron irradiation.

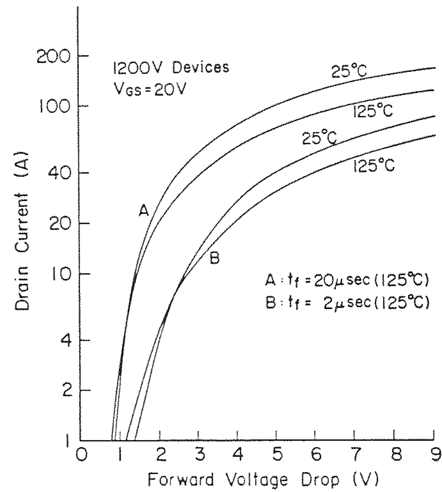


Fig.7 Current-voltage characteristics for 1200V BIFETs.

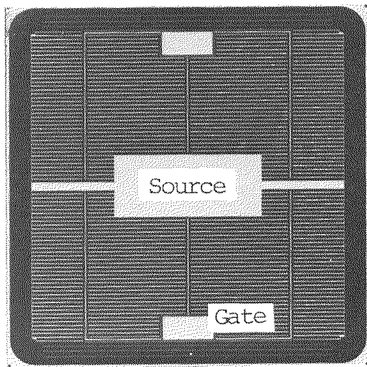


Fig.6 Source-gate pattern

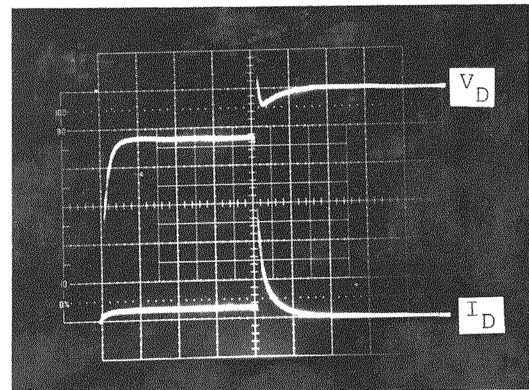


Fig.8

Typical turn-off waveforms for a 600V BIFET, which turns-off more than 140Amps drain current at 125°C. I_D: 30A/Div, V_D: 50V/Div, Time: 10μs/Div.

4. FABRICATION AND CHARACTERIZATION FOR 600V AND 1200V BIFETs.

6mm square chip BIFETs were fabricated by ordinary power MOS fabrication techniques. Figure 6 shows the source-gate pattern. The active region is 20mm^2. Figure 7 shows current-voltage characteristics for two kinds of 1200V devices. Obtained electrical characteristics are given in Table 1. Maximum controllable current capability was tested at 125°C with a resistive load. The developed 1200V BIFETs can turn-off more than 100Amps drain current within 10μsec and more than 75Amps within 2μsec at 125°C with the applied voltage as high as 1000V. Figures 8 and 9 show 140Amps turn-off wave forms for a 600V device and 75Amps turn-off wave forms with 1000V applied voltage for a 1200V device.

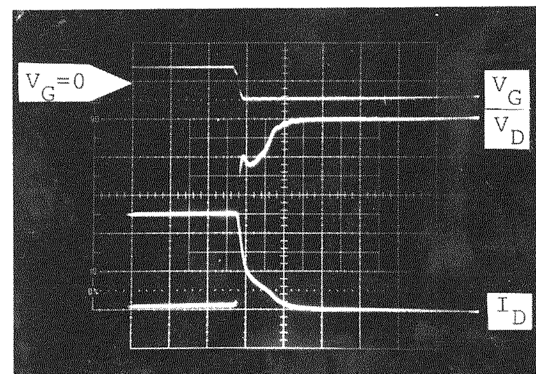


Fig.9

Typical turn-off waveforms for a 1200V BIFET, which turns-off 75Amps drain current with 1000V drain voltage at 125°C. I_D: 30A/Div, V_D: 200V/Div, Time: 2μs/Div.

5. DISCUSSIONS

Computer simulations were carried out to optimize the BIFET structure and source-gate patterns. Figure 10 shows the calculated electron density distribution inside the device. All of the hole current finally flows into the p-base and takes a completely different path from the

electron current, which flows through the channel region. This is a clear distinction between MOS thyristor and BIFET.

It is very important to realize a high controllable current in a BIFET, because a failure in the turn-off process directly means resultant destruction of the devices for the case of a high current level. However, it was observed that the BIFET could be safely latched-up when sufficient positive gate voltage was applied and that even a large surge current capability over 2500A/cm^2 could be realized by adjusting the sheet-resistance for the p-base layer. On the other hand, sufficiently low p-base sheet-resistance realizes a high latch-up current density, preventing the device from safe uniform latching-up before withstanding a high forward voltage drop.

Breakdown Voltage	600V		1200V	
V_{DS}(25°C)	1.8V(25A)	2.5V(25A)	2.5V(25A)	3.5V(20A)
V_{th}	3.5V			
t_{on}(125°C)	40ns	45ns	100ns	120ns
t_f (125°C)(25A)	10μs	2.3μs	20μs	3.0μs
t_d(off) (125°C)	0.5μs	0.35μs	0.5μs	0.3μs
I_D(MAX)(125°C)	>100A	>100A	>100A	>75A

Table 1. Electrical characteristics for four kinds of BIFETs

6. CONCLUSION

600V, 1200V 100A BIFET families have been successfully developed, based on the new vertical structure and CAD techniques. 1200V BIFETs can turn-off more than 75Amps drain current at 125°C and more than 100Amps at 25°C, both within 2μsec, without any device protection methods.

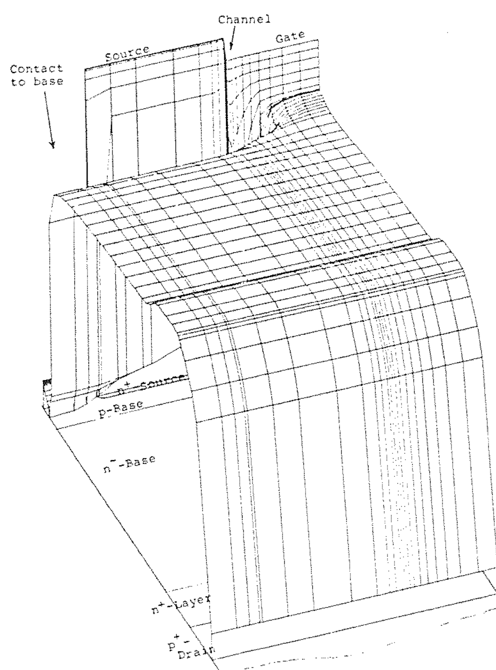


Fig.10 Calculated electron density distribution for a 600V BIFET.

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