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High Voltage Low On-Resistance VDMOS FET

Akio NAKAGAWA, Jiro YOSHIDA, Tadashi UTAGAWA,
Tsuneo TSUKAKOSHI, Hirohito TANABE[†] and Tsuyoshi KURAMOTO[†]

Toshiba Research and Development Center,
[†]Semiconductor Division, Saiwai-ku, Kawasaki 210, Japan

Recent theoretical analyses on MOS FETs revealed that most of the on-resistance came from the epi-layer so that thin and low resistivity epi-layer was desirable for low on-resistance. This paper presents a new junction termination technology suitable for achieving near ideal breakdown voltage for such low resistance epi-layer. This paper also describes design optimization of source pattern and impurity diffusion profile with aid of a two dimensional numerical model. On the basis of these techniques, a power MOS FET with 450 V sustaining voltage and 0.35 Ω on-resistance was realized at a high manufacturing yield.

§1. Introduction

Power MOS FETs are promising devices capable of handling high power at high frequency. It is only recent that MOS Field Effect Transistors appeared in the field of power electronics. The first achievement in the MOS FET technology was the concept of D-MOS.[1) It separated the high field depletion region from channel region, enabling as narrow a channel as a few microns even with high sustaining voltage. Another improvement, for realizing low on-resistance, was to make current flow vertically and place a drain contact at the bottom.[2) These two technologies are combined in Vertical D-MOS FETs.

On-resistance in the D-MOS FETs was intensively analyzed by many authors.[3–5) It was found that a large fraction of the resistance comes from the epi-layer, if source pattern is optimized. Thus a low resistivity thin epi-layer was desirable. Consequently, the junction termination technology is really important to keep high sustaining voltage with low on-resistance. A novel junction termination structure is introduced so as to realize near ideal breakdown characteristics and excellent stability, realizing high manufacturing yields. This makes it possible to fabricate FETs at a reasonable cost.

Another important point is to optimize source patterns and impurity diffusion profiles. An exact two dimensional numerical device model was developed for this purpose.[6,7) It assures that a simple stripe pattern is sufficient for low on-resistance of 0.08 $\Omega \cdot cm^2$ per unit active area.

On the basis of the above results, 5.5 mm square chip devices with 450 V sustaining voltage, 0.35 Ω on-resistance and 300 ns switching off time were easily obtained.

§2. A New Junction Termination Technology

Figure 1 shows the new junction termination method. Seemingly, the new structure consists of ordinary guard rings and field plates. However, the structure basically exhibits multi-field-plate characteristics. The guard rings only determine the potential of each field plate, which completely covers the n^- region between guard rings. The distance between guard rings hardly affects the breakdown characteristics, unless it is too short. The voltage difference between field plates or between guard rings is determined approximately by the insulator layer thickness as described in the following.

The voltage difference between guard rings 1 and 2 is the same as that between field plate

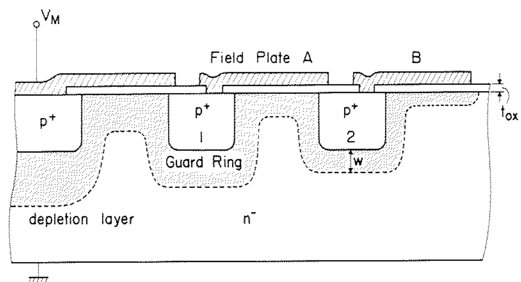

Fig. 1. The new junction termination method.

A and guard ring 2. Thus, voltage V_1 for guard ring 1 is given by eq. (1).

$$|V_1| = |V_2| + V_{ox}, \tag{1}$$

where V_2 is the guard ring 2 voltage and the V_{ox} is the voltage across insulator oxide between guard ring 2 and field plate A. Using abrupt junction approximation, V_2 is expressed by eq. (2):

$$|V_2| = \frac{qN_B W^2}{2\varepsilon_{si}} \tag{2}$$

where N_B and W denote impurity concentration and depletion layer width under guard ring 2. The ratio $|V_2|/V_{ox}$ is approximately proportional to the capacitance ratio for the oxide and the depletion layer. Thus, eq. (3) holds:

$$\frac{|V_2|}{V_{ox}} \cong \left(\frac{\varepsilon_{ox}}{t_{ox}}\right) \Big/ \left(\frac{2\varepsilon_{si}}{W}\right) \tag{3}$$

Combining eqs. (1) to (3), eq. (4) is obtained.

$$|V_1| - |V_2| = \frac{t_{ox}}{\varepsilon_{ox}} [2\varepsilon_{si} q N_B |V_2|]^{1/2} \tag{4}$$

Thus, voltage difference is only a function of t_{ox}, N_B and V_2 (or V_1). Table I shows voltage differences $|V_1| - |V_2|$ for various V_1 values under the condition that $t_{ox} = 1.0$ μm, and $N_B = 3.5 \times 10^{14}$/cm^3. Calculated voltage difference 50 V, under the condition $V_1 = -400$ V, approximately agrees with the measured 40 V value, as shown in Fig. 2.

The voltage difference between two guard rings can be determined merely by the insulated oxide layer thickness and does not depend on the spacing of two guard rings, thus realizing excellent stability. Figure 3 shows histograms manifesting superiority of this new structure by comparing with ordinary guard rings and field plates. The total number of samples was around 40 for each case. Samples were fabricated using 13 Ω·cm 38 μm epi-layer with three 5 μm diffusion depth guard rings. In the new structure, more than 400 V breakdown voltage was easily obtained at 96% manufacturing yield, whereas ideal breakdown voltage is 480 V. Figure 4 shows attained breakdown voltages for other cases. In general, 95% of ideal breakdown voltage was easily realized

Table I. Theoretical voltage differences $|V_1| - |V_2|$ for various V_1 values.

$\|V_1\|$ (V)	$\|V_2\|$ (V)	$\|V_1\| - \|V_2\|$ (V)
100	76.9	23.1
200	166.0	34.0
300	257.6	42.4
400	350.6	49.4

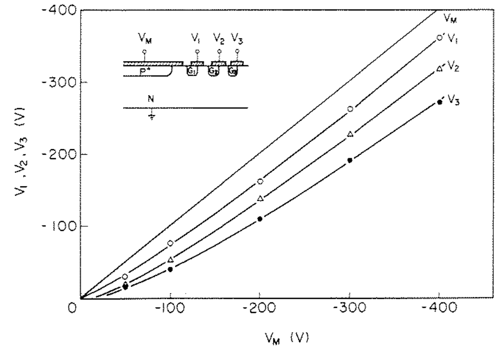

Fig. 2. Observed potential variations for three guard rings. The oxide thickness is 1.0 μm.

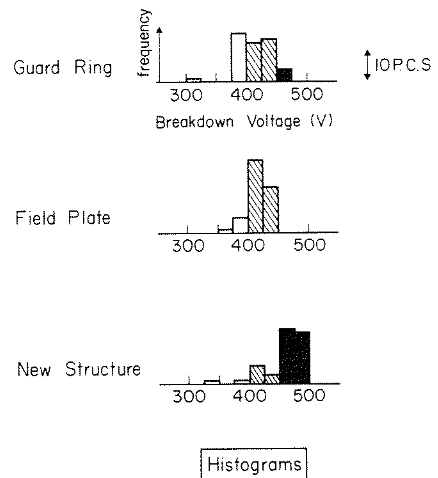

Fig. 3. Histograms for three junction termination methods.

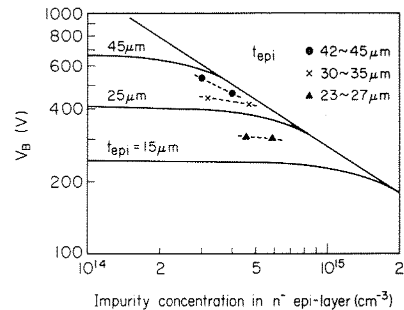

Fig. 4. Comparison between experimental and theoretical breakdown voltage.

at more than 90% yield for the case of three guard rings.

Although this structure reveals such excellent characteristics for 450 V devices, there are technological difficulties if this structure is applied for higher sustaining voltage devices, such as 1000 V devices, because the insulator oxide is required to be thicker than 2 μm in order to obtain an appropriate voltage difference between guard rings.

§3. On-State Resistance

Recently, the numerical device modeling has so progressed that it can be applied various design problems. Wieder and Tihanyi developed an exact two-dimensional numerical analysis model for a vertical D-MOS FET and analyzed a negative resistance phenomenon observed in the saturation region.[7]

A similar two-dimensional model was developed in the cource of the present study in order to make a precise estimation for the on-resistance and to optimize the device structure. In this model, Poisson and majority carrier continuity equations are approximated by a set of finite difference equations, which are solved by Stone's iterative method.[8] A gate and drain field dependent mobility model[9] is introduced to make an accurate prediction for on-resistance. Calculations were carried out for the device with simple stripe patterns which were characterized by two parameters L_S and L_G. L_S denotes the source width, and L_G denotes the source to source distance. Gate oxide thickness under the gate polysilicon is 1200 Å everywhere, sacrificing reverse transfer capacitance to favor low on-resistance.

Figure 5 shows an example of the calculated electron density distribution inside a device, which operates in the saturation region. High drain voltage causes a depletion layer to form underneath the gate electrode. This depletion layer pinches the current with the aid of the counterpart around the p-region. This pinch-off phenomenon, together with the velosity saturation effect in the channel, causes a current saturation.

In the following, a power MOS FET design optimization will be described. On-resistance in a power MOS FET is considered to be a sum of several fractional resistances: 1) channel resistance R_{ch}, 2) accumulation layer resistance

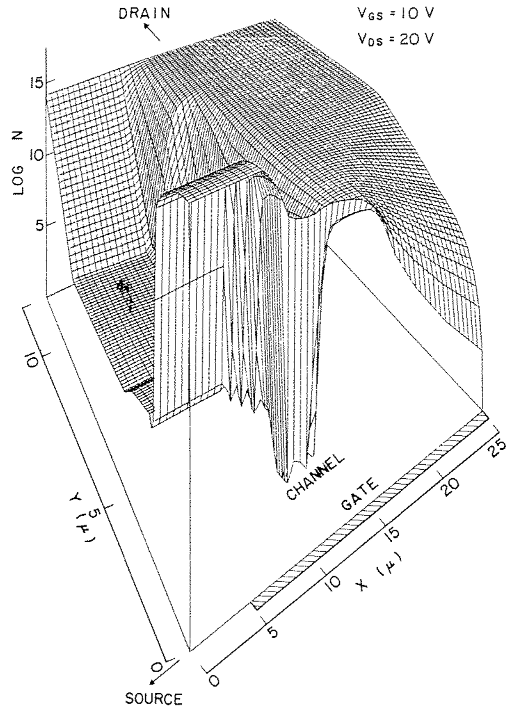

Fig. 5. Electron density distribution inside a device which operates in the saturation region.

R_{ac} and 3) epitaxial layer resistance R_{epi} including any spreading resistance. Relative contribution of these fractional resistances to the total on-resistance was estimated using a calculated potential distribution. It was found that the R_{ch} contribution to the R_{on} is around 10% for high gate voltage, unless the total channel width for a given chip area is extremely small. Though it is hard to distinguish the R_{ac} contribution to the total on-resistance from the R_{epi} contribution, the R_{ac} value is considered to be small, since it is basically a kind of channel resistance. Therefore, epitaxial silicon resistance dominates the total on-resistance for a high voltage MOS FET. In order to minimize R_{epi}, it is necessary to achieve a uniform current flow in the epitaxial layer. Owing to the accumulation layer under the gate oxide, the current will flow almost uniformly between adjacent p-regions, whereas the epi-layer beneath the p-region will not be fully utilized as a current path. Thus, narrow source width (L_S) and long source to source distance (L_G) are assumed to be favorable to a reduction in R_{epi}. However, an arbitrary increase in L_G reduces total channel width for a given chip area and, therefore, increases channel resistance R_{ch}, resulting

in large total on-resistance. As a result, there will be an optimum value for L_G which will minimize the total on-resistance.

These considerations were verified through a numerical analysis. Figure 6 shows the calculated and experimental results on L_S and L_G dependence of the total on-resistance for a 1 cm^2 active chip area. A good agreement is obtained between them. On-resistance decreases monotonically with the decrease in L_S. Therefore, L_S must be decreased down to the limit of the fabrication technology. On the other hand, it can be seen that there is an optimun value of L_G for given L_S. Though on-resistance remains small in a fairly wide L_G value range, it is desirable to choose a small L_G within this range because of realizing low gate-drain capacitance, high transconductance and high switching speed.

Diffusion depth X_{jp} of the p-well is an another important parameter which affects the total on-resistance. From a low on-resistance viewpoint, shallow X_{jp} is desirable. However, the trade-off problem between channel punch-through and threshold voltage prohibits making X_{jp} smaller than a certain critical value. For a 400 to 450 V breakdown voltage device, X_{jp} of 3 to 5 μm is an adequate value. Two-dimensional calculation shows that the difference in minimum on-resistance between 3 and 5 μm is less than 5%, unless an inadequately large L_S is chosen.

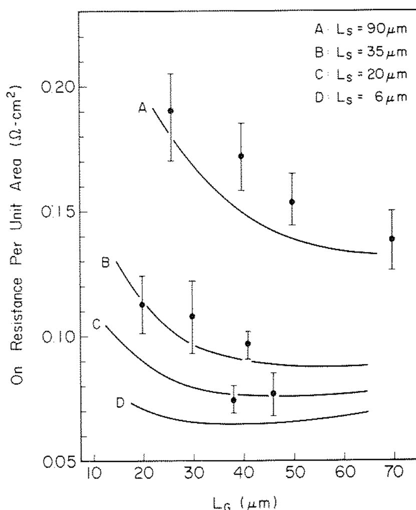

Fig. 6. L_S and L_G dependence of the on-resistance for a 1 cm^2 active chip area. The solid lines show the calculated results, and the black circle shows the experimental results.

The variation in the on-resistance with epi-layer thickness and its resistivity was also investigated by the model. On-resistance dependences on epi-layer thickness t_{epi} and resistivity ρ_s are shown in Figs. 7 and 8, respectively. As the variation in epi-layer thickness and resistivity brings about nearly the same amount of relative change in the total on-resistance, a fairly precise control of these factors is needed to realize a minimum on-resistance device.

§4. Device Fabrication and Characterization

In this section, device fabrication processes and electrical characteristics are briefly described.

The devices were fabricated using polysilicon gate and ion implantation processes. Initially, boron ions are implanted into epi-layer sub-

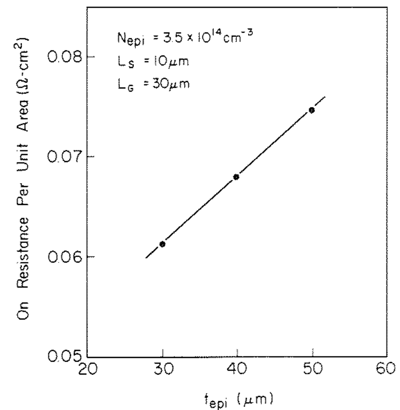

Fig. 7. Calculated on-resistance dependence on epi-layer thickness.

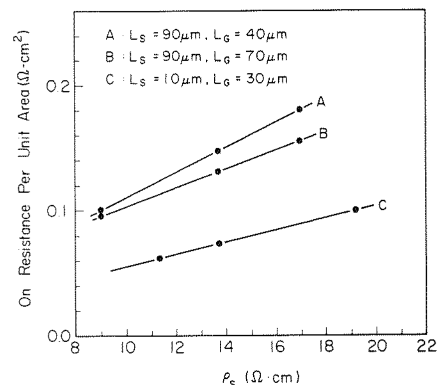

Fig. 8. Calculated on-resistance dependence on epi-layer resistivity.

strate to form 3 guard rings. Appropriately thick thermal oxide is subsequently grown as a junction passivation insulator, which determines the voltage difference between two guard rings. Channel region is automatically formed by the usual double diffusion technique, using polysilicon as a mask. Polysilicon is completely insulated by the surrounding SiO_2 layer. The source pattern is a simple stripe and short circuits between p-layer and n^+ source layer are frequently made. Figure 9 shows the device cross section. Source layers are used as lateral current paths, so a 6 μm source width can be realized. Each gate polysilicon layer is a 27×200 μm^2 square.

Obtained characteristics for a 5.5 mm square chip device (0.2 cm^2 active area) are listed in Table II. A fabricated device is packaged in a TO-3. The new guard ring structure enables obtaining high sustaining voltage 450 V. 0.35 Ω device on-resistance for 0.2 cm^2 active area agrees very closely with calculated value 0.07 Ω per unit active area. Switching times were measured when applied voltage is 200 V and drain current is 5 A.

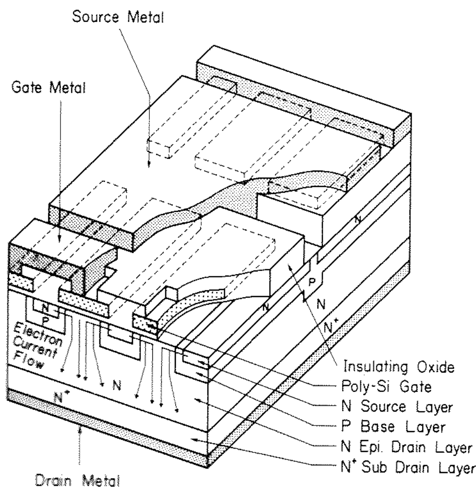

Fig. 9. Schematic representation of the structure of the power MOS FET used for experiments.

Table II. Obtained device characteristics for a 5.5 mm square chip (0.2 cm^2 active area).

Drain-source breakdown voltage	450 V
Continuous drain current, I_D	10 A
On-resistance ($I_D=5$ A, $V_{GS}=10$ V)	0.35 Ω
Reverse transfer capacitance ($V_{GS}=0$, $V_{DS}=10$ V, $f=1$ MHz)	70 pF
Forward transfer conductance	5–6 s
Turn-on time	60 ns
Turn-off time	300 ns
Max. power dissipation	120 W

Recently, 0.3–0.4 Ω on-resistance devices with 400–500 V sustaining voltage have appeared on the market.[10] However, their prices are still much higher than the corresponding bipolar devices. The new junction termination technology makes it possible to obtain low on-resistance MOS FETs at reasonable manufacturing cost by simultaneously making use of qualified LSI fabrication technology. Thus, it is expected that MOS FETs will replace bipolar devices for high frequency application.

§5. Conclusion

Junction Termination technology is very important to realize high sustaining voltage Power MOS FETs with low on-resistance, because low resistivity and thin epi-layer are desirable for such devices. A highly reliable junction termination structure was presented in this paper. This structure enabled realizing 95% ideal junction breakdown voltage at a high manufacturing yield.

Another important design problem is to optimize source pattern and impurity diffusion profile. An exact two dimensional model was developed to solve these problems.

On the basis of the above techniques, 450 V sustaining voltage devices with 0.07–0.08 Ω·cm^2 on-resistance per unit active area were successfully developed.

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