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High Power Gate Turn-Off Thyristors

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High power gate turn-off thyristors (GTO's) are studied because of their gate turn-off capability in addition to the usual thyristor characteristics. GTO development, however, has suffered from difficulty in attaining high current gate turn-off capability. From the experimental results, maximum gate turn-off current I_{ATO} depends upon a factor (V_{J1}/ρ_{SPB}), as well as the n-base resistivity. On the basis of this principle success was achieved in realizing devices with more than 600 amperes of I_{ATO}. Various considerations were made for GTO design, together with numerous experiments in fabrication and characterization.

§1. Introduction

High power gate turn-off thyristor (GTO) development is one of the recent topics in the field of power electronics, because of their gate turn-off capability in addition to the usual thyristor characteristics. However, GTO development has suffered from difficulty in attaining high current gate turn-off capability. In several previous publications on high power GTOs, maximum gate turn-off currents (I_{ATO}) have been reported in the 50 to 200 ampere range.[1,2] This is assumed to be based on the fact that the anode current concentrates itself to a narrow portion beneath the cathode during gate turn-off. Thus, the current density there is increased prominently.

This paper describes not only design considerations for increasing I_{ATO} beyond the above values, but also the device characteristics, such as surge currents, latching currents, on-state voltages, switching speeds and turn-off gains.

Figure 1 shows a mesa-type GTO-segment configuration, including impurity doping profiles and other design parameters. An actual GTO-unit consists of a plurality of the segments, which are parallel-connected to each other.

In §2, discussions will be made first from the device doping profile viewpoint on increasing I_{ATO} design criteria and method of control common base current gain factor α_{npn}. In §3, GTO fabrication process will be discussed with specific emphasis on gold diffusion process, which contributes appreciably in controlling common base current gain factor α_{pnp}. In §4, various experimental results will

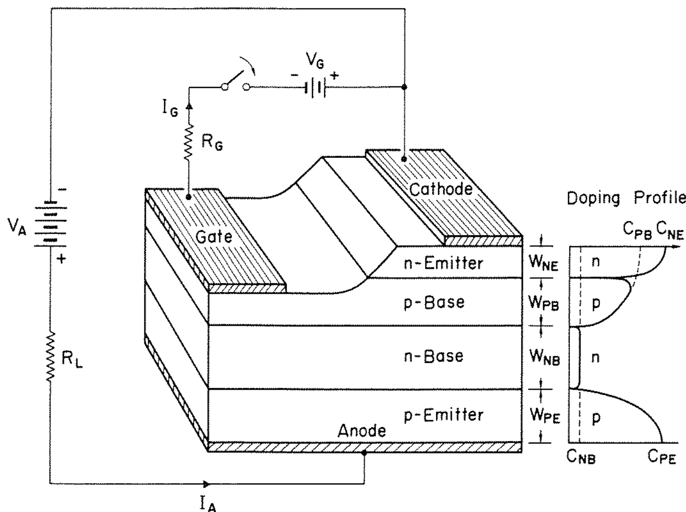

Fig. 1. GTO-segment configuration and doping profile.

be demonstrated and discussions will be made about possibilities and limitations in the frequency characteristics.

§2. Design Criteria on Doping Profile

2.1 *Relation between* I_{ATO} *and* V_{J1}/ρ_{SPB}

Up to the present, several authors mentioned the importance of the high cathode-gate junction reverse breakdown voltage (V_{J1}) and the low p-base sheet resistance (ρ_{SPB}) for the high gate turn-off capability.[2-4] Through extensive experiments, the authors found a strong relationship between I_{ATO} and the ratio (V_{J1}/ρ_{SPB}). Figure 2 shows approximately linear characteristics obtained from measurements on actual multiemitter devices.

Lateral voltage drop beneath the emitter area due to the gate current is not only proportional to ρ_{SPB}, but also restricted by V_{J1}. A large (V_{J1}/ρ_{SPB}) value allows a high current to flow from a squeezed on-region to a gate boundary, thus contributing to reducing anode current crowding during the gate turn-off, and to improving the gate turn-off capability.

Another important point is n-base resistivity dependence on I_{ATO}. This fact is probably due to the low electric field at the formed depletion region around the center junction J_2, because of a low n-base impurity concentration. This relation makes it possible to realize a high voltage high current device, such as 1300 V and 600 A, which are required for applications for the high power inverters.

The current redistribution among GTO

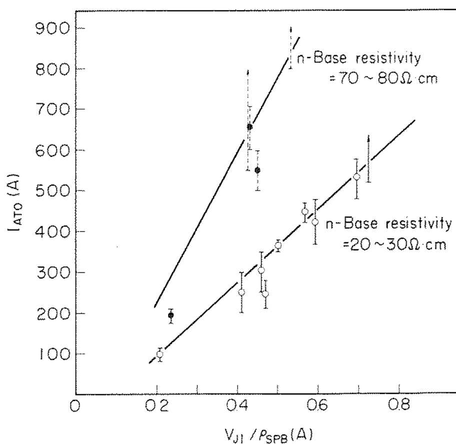

Fig. 2. Maximum gate turn-off currents vs. (V_{J1}/ρ_{SPB}) characteristics with n-base resistivity as a parameter.

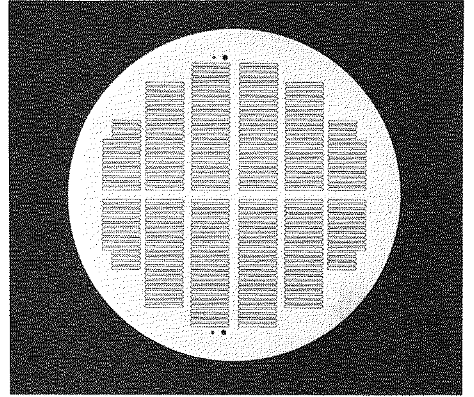

Fig. 3. Emitter pattern for a GTO-unit.

segments due to the non-uniformity of electrical characteristics, is reduced also by narrow emitter lateral width, as well as by a large (V_{J1}/ρ_{SPB}) value and a high n-base resistivity. As a result of numerous experimental fabrications and characterizations, the emitter pattern shown in Fig. 3 was determined.[5] It consists of 260 emitter fingers of 4 mm in length and 300 microns in width.

2.2 *Relation between* α_{npn} *and* C_{PJ1}

According to a well known two-transistor approximation, maximum gate turn-off gain is given by the formula:[6,7]

$$G_{off}(\max)=\frac{\alpha_{npn}}{\alpha_{npn}+\alpha_{pnp}-1}, \tag{1}$$

where α_{npn} and α_{pnp} are common base current amplification factors. It is assumed that the gate is connected to the p-base layer. From eq. (1) it appears desirable to make the alpha sum close to unity, while keeping α_{npn} sufficiently high.

Besides the gate turn-off capabilities, a high power GTO should reveal as good conduction characteristics as a usual thyristor. With respect to on-state characteristics, it is favorable to make α_{npn} as high as possible. Keeping α_{npn} high corresponds to making p-base thickness small, as well as to making carrier lifetime in p-base layer high. As described in §2.1, however, increasing I_{ATO} causes reduction in p-base sheet resistance, thus resulting in large p-base thickness. Besides, it is considered to be difficult to keep the carrier lifetime in p-base layer sufficiently high, even if the thermal processings are undertaken very carefully.

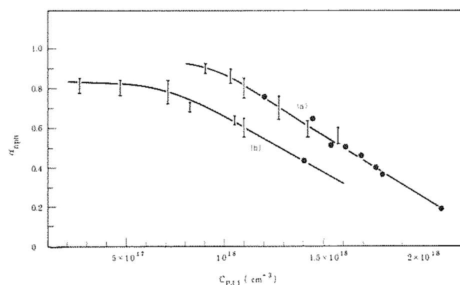

Fig. 4. Current gain α_{npn} vs. C_{PJ1} characteristics with the gold diffusion temperature as a parameter.

Therefore, a certain limitation will be imposed on α_{npn} value.

Another limitation on α_{npn} is imposed by concentration C_{PJ1}, which is defined as the extrapolated impurity concentration of *p*-base at J_1 junction. Figure 4 shows experimental α_{npn} vs. C_{PJ1} characteristics with gold diffusion temperature as a parameter, where α_{npn} is measured by Fullop's method,[8] and C_{PJ1} is estimated from the spreading resistance measurement. Line (a) is for gold diffusion temperature below 840°C, and (b) for the 860 to 880°C gold diffusion temperature range. In each case, the diffusion time was kept constant at 25 minutes.

As is shown in Fig. 4, α_{npn} is decreased by increasing C_{PJ1}, which is, to the authors' knowledge, a new result. It is assumed that the dependence on C_{PJ1} is due to reduction in emitter injection efficiency caused by heavy doping effect on both *n*-emitter and *p*-base.[9] From this result, keeping α_{npn} high corresponds to making C_{PJ1} sufficiently low, as well as making the lifetime in *p*-base high.

§3. Fabrication Processes

3.1 *General explanation*

In general, processes applied to the present GTO parallel those used in thyristor manufacture. Figure 5 shows a broad outline process flow for GTO fabrication. *N*-type silicon in the 60–80 ohm·cm resistivity range is chosen as the starting material in order to obtain more than 1300 V blocking voltage capability. Initially, *p*-type diffusant, such as gallium, will be doped onto both surfaces of an *n*-type raw wafer to construct the basic *pnp* structure. Using a vacuum gallium diffusion process, precise control of sheet resistance and junction depth can be attained.

1. P-type Diffusion
2. N-emitter Diffusion
3. Gate-region Etchdown
4. Oxidation for Junction Passivation
5. Gold Diffusion
6. Selective Oxide Removal
7. Alloying
8. Cathode and Gate Contact Build-up
9. Selective Contact Removal
10. Surface Contouring
11. Surface Passivation
12. Packaging

Fig. 5. Process flow for GTO fabrication.

The next step is a phosphorus deposition and its slumping to form an *npnp* four layer structure with the required cathode emitter junction depth and surface concentration.

Following this, the gate is etched down to a proper depth to subdivide the cathode emitter mesa fingers. After the phosphorus layer etching on the anode side, the wafer is oxidized to passivate the cathode emitter junction surface.

Gold is then evaporated and diffused from the anode side to control the carrier lifetime in the *n*-base layer. The wafer is then alloyed to a tungsten disk with the anode surface at the bottom. After the cathode-gate metallization, edges are beveled to realize the required blocking voltage capability.

Beveled wafer periphery is coated by silicone rubber, for junction surface protection. The wafer is finally mounted in a flat package and sealed-off. Figure 6 shows an actual view of a packaged device.

3.2 *Gold diffusion process*

Gold must be diffused into the device to reduce the carrier lifetime for achieving fast turn-off characteristics. The gold diffusion, while decreasing the carrier lifetime, also increases the forward voltage drop, junction leakage current and latching current. Accordingly, the gold diffusion must be under-

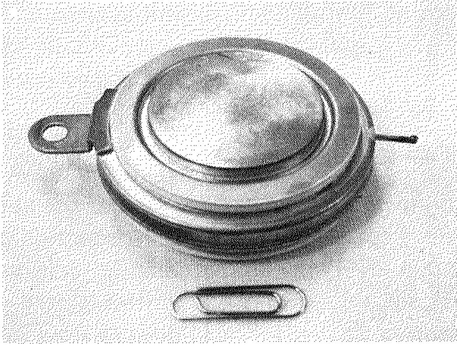

Fig. 6. A high power GTO.

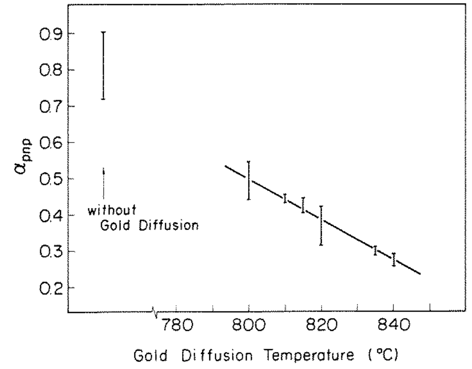

Fig. 7. Current gain α_{pnp} vs. gold diffusion temperature.

taken in a trade-off manner regarding these characteristics.

With respect to alphas, gold diffusion influences α_{pnp} alone for diffusion temperature below 840°C, as mentioned in §2.2. This is considered to be based on the fact that the gold solubility limit is comparable to the majority carrier concentration in the n-base region, and much less than that for p-base region.[5]

Figure 7 shows an experimental α_{pnp} vs. gold diffusion temperature characteristic for the 70 Ω·cm n-base resistivity and the 250 μm n-base thickness GTO units, where the diffusion time was kept constant at 25 minutes. α_{pnp} decreases linearly as diffusion temperature increases in the 800°C to 840°C temperature range. Using the figure, α_{pnp} will be decided so as to match α_{npn} value.

§4. Experimental Results

4.1 *Characterization*

Table I shows main characteristics for the fabricated devices. Forward blocking voltage is more than 1500 V, for the 20 Ω shunt resistance between cathode and gate. This resistance aids in avoiding the self-switching caused by the center junction leakage current.

Figure 8 shows an on-state voltage vs. anode current characteristic for developed GTO-units. On-state voltage is 1.8 volts at the 600 amperes anode current. Even for a high surge current of 3200 amperes, on-state voltage was shown to be less than 3 volts. These values are relatively low, in comparison to previously existing high power GTO's.[1,2,10,11] Latching current is less than 3 amperes, which is also sufficiently low considering the high gate turn-

Table I. High power GTO characteristics.
V_D: Anode-cathode voltage, t_g=Turn-on pulse width, T_j: Junction temperature, R_L= Load resistance, R_{GK}=parallel resistance between gate and cathode.

Test Terms	Typical Values	Test Conditions
Maximum gate turn-off current	600 A	see Fig. 9 $T_j=110°C$
Turn-on time	11 μs	$I_g=3$ A, $V_D=650$ V
Delay time	5 μs	$t_g=20$ μs, $T_j=25°C$
On-state voltage	1.8 V	$I_a=600$ A, $T_j=25°C$
Gate turn-off time	12 μs	see Fig. 9 $T_j=110°C$
Minimum DC gate trigger current	300 mA	$V_D=24$ V, $T_j=25°C$
Minimum DC gate trigger voltage	0.63 V	
Surge on-state current	more than 3500 A	50 Hz sinusoidal one-cycle peak
Gate-cathode breakdown voltage	14 V	$T_j=25°C$
Holding/Latching current	3 A	$T_j=25°C$, $I_g=3$ A $t_g=20$ μs, $R_L=5$ Ω
Forward blocking voltage	1500 V	$T_j=115°C$, $R_{GK}=20$ Ω

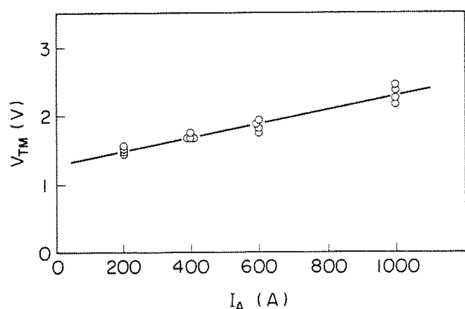

Fig. 8. On-state voltage vs. anode current characteristic.

off capability of the present devices.

Figure 9 shows a resistive load chopper circuit which was used to evaluate the gate turn-off characteristics.[5] The following two circuit factors are taken into consideration to achieve the full gate turn-off capability inherent to the test samples. One is the snubber circuit for switching power suppression. The other is the negative gate drive condition.

Figure 10(A) and (B) show typical switching waveforms during the gate turn-on and off transient, respectively. The gate turn-on time (T_{on}), as shown in Fig. 10(A), is limited by α_{npn}, which depends on the doping profile and the carrier lifetime. From various sample evaluation results, current rise rate was shown to increase as α_{npn} increases. The gate turn-off time (T_{off}), as shown in Fig. 10(B), consists of storage time (T_S) and fall time (T_f). Gate turn-off time, specifically the storage time, depends upon the on-state current and the

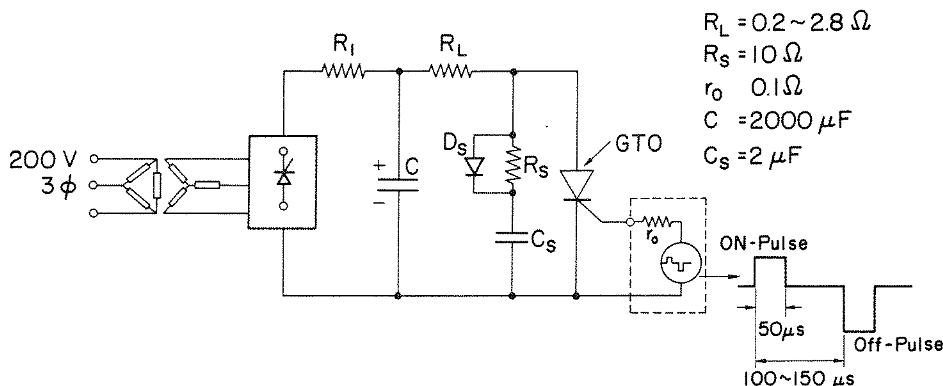

Fig. 9. Chopper circuit for gate turn-off characteristic evaluations.

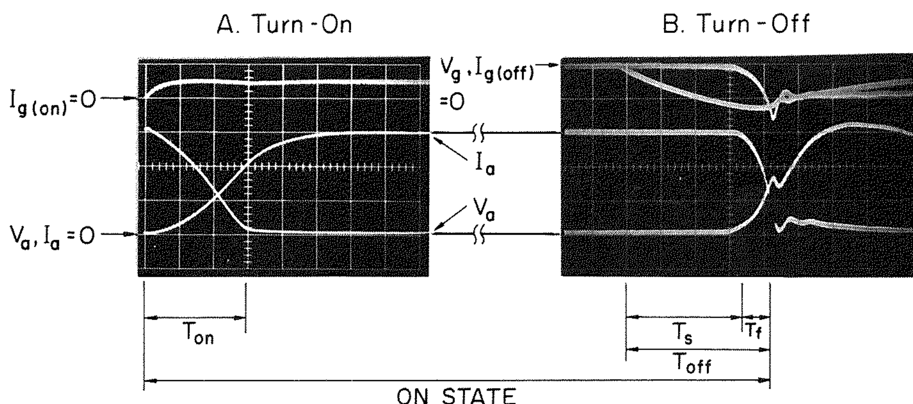

Fig. 10. Typical switching waveforms.
(A) Gate turn-on, (B) Gate turn-off.
V_a; Anode-cathode voltage (200 V/div.)
I_a; Anode current (200 A/div.)
t; Time (2 μs/div.)
(A): I_g; Gate current (10 A/div.)
(B): I_g; Gate current (120 A/div.)
V_g; Gate-cathode voltage (20 V/div.)

gate current rise rate (dI_G/dt), which is 30 A/μs in this example. Operational turn-off gain, defined as (I_A/I_{Gpeak}), also depends upon (dI_G/dt). This value is around 4. From other examples, operational turn-off gain of 6–8 was realized at the 600 amperes on-state current with the 10 A/μs gate current rise rate. Making (dI_G/dt) low, however, leads to an increase in the gate turn-off time, as well as an increase in the gate power dissipation.

An anode voltage spike, as shown in the fall time of Fig. 10(B), occurs due to a stray inductance of the snubber circuit. Endeavor was made to allocate the snubber circuit components as close to GTO-unit as possible, in order to minimize the inductance.

4.2 *High frequency characteristics*

I_{ATO} is restricted by two factors. One is the self turn-on behavior due to the tail current after the gate turn-off pulse disappearance. The other is the device destruction mainly due to the current crowding during the gate turn-off. It is at the latter case, as described in §2.1, that an increasing V_{J1}/ρ_{SPB} value improves the gate turn-off capability. I_{ATO}, in this latter case, depends upon the device operation frequency.

Figure 11 shows an example for a number of lower current rating test samples, specifically intended for the frequency characteristic evaluation. They have a relatively good frequency characteristic, compared to the high power type device developed. From a series of experiments for the frequency dependence of I_{ATO}, it appears that, for high frequency of around 10 kHz, I_{ATO} decreases with an increase in device carrier lifetimes, as well as increase in frequency, whereas for a low frequency of around 50 Hz, I_{ATO} scarcely depends upon these factors.[12]

Power dissipation per unit time during gate turn-off is more than ten times as large as that for steady on-state. Thus, power loss for the high frequency operation becomes extremely large, so that the gate turn-off capability reduces, as mentioned above. Introducing the carrier lifetime killer is the most convenient way to decrease switching losses, specifically loss due to tail current, which occupies a considerable part of the total losses in the device with long n-base carrier lifetimes.

The self switching phenomenon is frequently observed on devices with high carrier lifetimes and low holding current. The current at self switching depends strictly upon the gate turn-off pulse width, being increased by widening the off-pulse width. Generally, there is a minimum gate pulse width enough to turn-off a certain current. Thus, self switching is understood as a phenomenon in which the required turn-off pulse width is extremely large, because of large current amplification factors of the device.

The self switching is also sensitively influenced by the α_{pnp} value, as shown in Fig. 12, i.e. it can be avoided by reducing the carrier lifetime in the n-base. Therefore, the carrier lifetime control is very important, concerning frequency characteristics, gate turn-off charac-

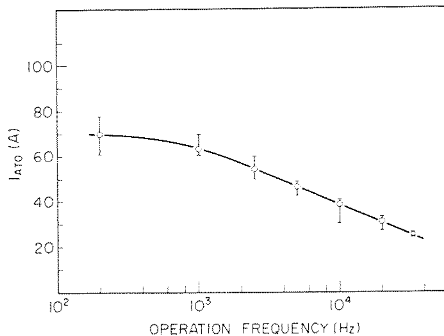

Fig. 11. I_{ATO} vs. operation frequency characteristic for test samples.

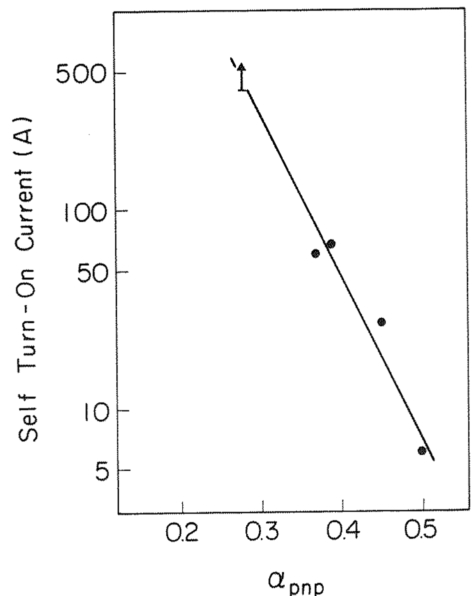

Fig. 12. Self turn-on current vs. α_{pnp} characteristic.

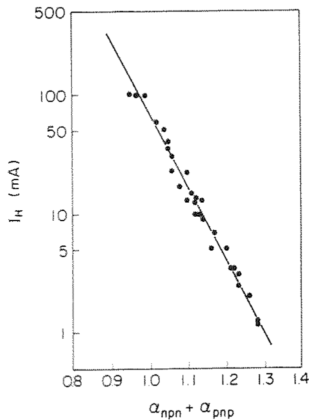

Fig. 13. Holding current vs. ($\alpha_{npn}+\alpha_{pnp}$) characteristic for GTO segments.

teristics and holding current. A large amount of gold doping improves frequency and gate turn-off characteristics, but increases holding current significantly. Figure 13 shows the holding current vs. the sum of α_{npn} and α_{pnp} characteristic. As a result, the gold diffusion condition should be determined in a trade-off manner regarding these quantities.

§5. Conclusion

Success was achieved in realizing GTO's with higher forward blocking voltages and gate turn-off currents, as well as with lower on-state voltages and latching currents than existing high power GTO's. Vital points for realizing these characteristics were found to be 1) optimization of the impurity concentration profile and 2) precise control of carrier lifetimes in the two base regions.

The GTO's thus developed have forward blocking voltages of more than 1500 V, maximum gate turn-off currents of more than 600 A, and on-state voltages of less than 1.8 V at 600 A, as well as latching currents of less than 3 A. In addition, speculations were made about possibilities and limitations in the frequency characteristic from the experimental results on another group of test samples. All of these results seem to promise prosperity for high power GTO's.

Acknowledgement

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