RAPID CONVERGENCE BIPOLAR-MOS COMPOSITE DEVICE MODEL--TONADDEII-- and ITS APPLICATION TO BIPOLAR-MODE MOSFETs(IGBT)

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Abstract

A rapid convergence bipolar-MOS composite device simulator, TONADDEII, has been developed. It was found that a combination of coupled method, complete Newton scheme, 9 point discretization and ILUBCG method enables rapid convergence for both static and transient solutions regardless of bias conditions. TONADDEII was applied to bipolar-mode MOSFETs(IGBT), analyzing N-buffer effects on electrical characteristics and why the bipolar-mode MOSFET safe operating area exceeds the theoretical limit for NPN bipolar transistors.

1. Introduction.

A rapid convergence bipolar-MOS composite device simulator, TONADDEII, has been developed. It reaches convergence within 4 or 5 Newton iterations regardless of bias conditions. It was confirmed for a number of devices that the inclusion of all the derivatives associated with three basic variables (p,n,ψ) in a Jacobian matrix for the Newton scheme is effective to accelerate convergence.

Conjugate gradient methods have been successfully applied to a single differential equation (decoupled method)[1]. The present paper shows that a combination of the complete Newton scheme (coupled method), ILUBCG method and 9 point discretization realizes a rapid convergence bipolar device simulator not only for static cases but also for transient and high voltage cases(more than 600V).

2. Composite device simulator--TONADDEII (TOshiba Numerical Analysis Program for Device DEsign)

TONADDEII is a general purpose two dimensional bipolar-MOS composite device simulator. It adopts the finite difference method, easily taking advantage of iterative solution techniques. It can deal with any device structure including SiO_2 and air regions.

The simulator includes various effects such as heavy doping effects based on effective Fermi statistics[2], SRH and Auger recombination, field dependent mobilities, carrier to carrier scattering[3] etc.

2.1 Solution technique

TONADDEII adopts a coupled method, a variable set(p,n,ψ) and a 9 point discretization method, which means that all variables associated with adjacent 9 grid points (A,B,C,D,E,F,G,H and I shown in Fig.1) appear in the discretized difference equations and are treated as variables also in Newton's iteration scheme. These three items are effective to accelerate convergence by including all the derivatives in the Jacobian matrix for the Newton scheme. For example, the

X-component of an electric field for point M (center of two grid points,B and H) must be calculated from 6ψ's associated with points A,B,C,G,H and I. Thus, the mobility derivatives associated with the adjacent 9 grid points must appear in the linearized difference equations. The obtained Jacobian matrix A for Newton's iteration has the form shown in Fig.2, where ⊠ denotes a 3 by 3 matrix. Originally, TONADDEII used a direct method to solve the large set of linearized equations: $A\delta x=b$. However, the direct solution method requires a large memory size and a long computation time, and is not practical for cases involving a large number of grid points.

This paper reports results of tests on BCG(biconjugate gradient),CGS(conjugate gradient squared), and CR(conjugate residual) methods, from viewpoints of computation time and memory size for coupled solutions, high voltage and high injection cases and time-dependent solutions.

Prior to applying the BCG/CR/CGS method, adequate scaling was carried out both column- and row-wise. Incomplete LU-decomposition was then carried out in the usual procedure, considering the Jacobian as a matrix composed of 3x3 sub-matrices.

$$A=L\ U+R, \quad \text{------------------------------(1)}$$

where L and U were assumed to have non-zero elements shown in Fig.3.

BCG/CGS/CR methods were then applied to one of the following three equations.

$$(LU)^{-1}Ax=(LU)^{-1}b,\quad L^{-1}AU^{-1}Ux=L^{-1}b,\quad A(LU)^{-1}(LU)x=b \quad \text{-----(2,3,4)}$$

In this paper, the BCG method using L,U matrices, as shown in Fig.3, is called ILUBCG(1,3). Similarly, ILUBCG(1,2) and ILUBCG(1,1) denote the method where x and y are ignored in Fig.3 and the method where x,y,v and w are ignored, respectively. For the cases of CGS and CR methods, the same notations are used.

Convergence characteristics for the BCG/CGS method, applied for static and transient problems, are shown in Figs.4 and 5, respectively. Although the CR method was tested for the same problems, convergence could not always be obtained.

In static analysis, ILUCGS(1,3) was the most efficient from the viewpoint of computation time[4]. However, in high voltage transient analysis, the ILUBCG(1,3) method was more stable and efficient than ILUCGS(1,3) and a larger time step increment Δt was allowable for the ILUBCG(1,3) method, as seen in Fig.5. Thus, ILUBCG seems to be the most reliable method for all the cases.

The typical CPU time, required to reach convergence using ILUBCG(1,2) for 1 Newton cycle in static analysis, was 2.5sec. (45 ILUBCG iteration) on a CRAY-XMP computer for a 70x61 grid point system.

Figure 6 shows Newton iteration number required to reach convergence vs. drain voltage characteristics, when TONADDEII was applied to simulate 600V Bipolar-Mode MOSFET current-voltage characteristics (see Fig.7 for device structure). TONADDEII reached convergence within 5 Newton iterations regardless of bias conditions to assure more than 5 digit accuracy in current continuity, whereas a conventional five point discretization method could not because it cannot take into account all of the derivatives such as mobility derivatives etc.

2.2 Time-dependent solution including outer circuit.

In order to simulate turn-off characteristics for bipolar-mode MOSFETs, efficient solution algorithms (see Fig.8) have been developed. These are 1)adequate initial guess generator, 2)automatic time step generator and 3)efficient outer circuit solution algorithm.

The automatic time step generator adopts a very simple but reliable method. The time increment Δt is repeatedly reduced to half its own value until all of the corrected $p+\delta p$ and $n+\delta n$ values become positive after initial Newton cycle for each new time step. Since an adequate judgement for the Δt value is carried out based on the results from the initial Newton cycle, CPU time can be greatly saved. The time increment Δt for the next time step is automatically set as twice the previous value when convergence is successfuly obtained.

3. Analysis of Bipolar-Mode MOSFET electrical characteristics.

The channel electron mobilty model, included in TONADDEII, adopts a modified Yamaguchi model. Instead of decomposing electric field into two components, vertical and parallel to the current vector, TONADDEII simply uses E_x and E_y in order to facilitate the inclusion of mobility derivatives in a Jacobian matrix. For vertical FETs, this approximation gives only a small error of less than 1% in total drain current for 12.5V gate voltage.

$$\mu_{ch}=\mu_0(|E_x|)(1+1.539\cdot 10^{-5}|E_y|)^{-0.5} \qquad \text{----------------------(5)}$$

This channel mobility is only applied for electrons in the channel region and in the accumulated layer beneath the gate electrode(see Fig.7).

Bipolar-mode MOSFETs (IGBT) are nearly ideal power devices, achieving large current capability and high switching speed, simultaneously. It was experimentally found recently that the power dissipation limit in terms of current voltage product far exceeds the theoretical limit ($2x10^5 W/cm^2$[6]) for NPN bipolar transistors[7]. Especially, bipolar-mode MOSFETs withstand $8x10^5 W/cm^2$ power dissipation for $10\mu sec$[7]. In this section, the reason for this will be analyzed together with carrier lifetime and N^+-buffer effects on'electrical characteristics.

Figures 9 and 10 show two sets of current voltage characteristics for the cases where electron and hole lifetime ratios (τ_n/τ_p) are 1.0 and 4.0, respectively. As the τ_n/τ_p ratio increases, high injection level lifetime over low injection level lifetime ratio $(\tau_n+\tau_p)/\tau_p$ also increases. This causes drastic transition from low injection level operation (MOSFET-mode) to high injection level operation (bipolar-mode) for low τ_p cases, resulting in an S-shape V-I curve as seen in a $0.03\mu sec.$ τp case in Fig.10.

Figure 11 shows calculated turn-off waveforms for the $\tau_n/\tau_p=4.0$ case. It was found for the cases of low carrier lifetimes that the anode voltage has already recovered to 200V before the gate voltage becomes below the threshold voltage Vth(=2.5V). This is significant, in that the electron current still flows across the

high electric field region (so called depletion layer) and that electrons and holes both exist even in the depletion layer when the anode voltage has already recovered to 200V. Thus, the net positive charge N^+ in the depletion layer is given by $q(N_D+p-n)$. The avalanche breakdown voltage limit V_{BD} is given by

$$V_{BD}=60(E_G/1.1)^{1.5}(N^+/10^{16})^{-3/4}, \quad (6)$$

and $$N^+=N_D+J_p/qv_p-J_n/qv_n, \quad (7)$$

where v_p and v_n denote hole and electron saturation velocities,respectively. Then, the avalanche breakdown limit voltage V_{BD} is related to the drain current I_D :

$$V_{BD}=60(E_G/1.1)^{1.5}[\{N_D+I_D/qv_pS_p-Ich(1/qv_pS_p+1/qv_nS_n)\}/10^{16}]^{-3/4}, \quad (8)$$

where Ich denotes the electron channel current and S_p,S_n the effective current conducting areas for hole and electron currents, respectively. If Ich is zero, Equation (8) reduces to the ordinary avaranche limit equation for PNP transistors. Equation (8) provides the possibility that the maximum power dissipation can exceed the theoretical limit for NPN or PNP transistors because of the contribution from the channel electron current, which neutralizes the depletion layer charge to some degree, as long as current concentration into a small part of the device area is not significant. This is possible in bipolar-mode MOSFETs because the electron base current to the PNP transistor portion is uniformly distributed by the MOS gate control.

Figure 12 shows calculated trade-off relations between forward voltage and fall-time with N-buffer doping as a parameter. A heavily doped N-buffer improves the trade-off relation for slow fall-time region. However,it deteriorates the relation for high switching speed region. The trade-off relation for the N^+-buffer is improved as the τ_n/τ_p ratio increases, as seen in Fig.12.

4. Conclusion

Rapid and stable convergences can be assured even for high voltage transient solutions by adopting a combination of the coupled method, complete Newton scheme, 9 point discretization, and ILUBCG method.

By applying TONADDEII to bipolar-mode MOSFETs, It was interpreted that the safe operating area for Bipolar-Mode MOSFETs can exceed the theoretical limit for NPN bipolar transistors.

References

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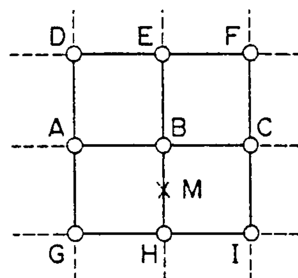

Fig.1 Grid system for difference equations.

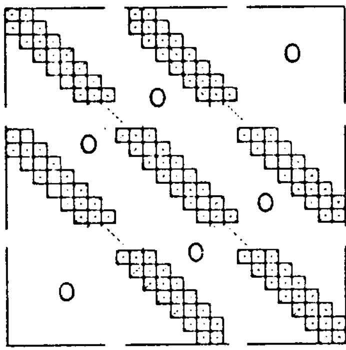

Fig.2 Jacobian matrix A, including all derivatives associated with adjacent 9 grid points. ⊠ represents a 3 by 3 non zero matrix.

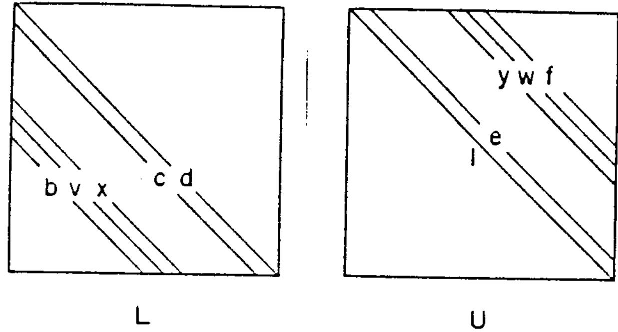

Fig.3 Non-zero elements for L, U matrices. Each line represents 3 by 3 sub-matrix line.

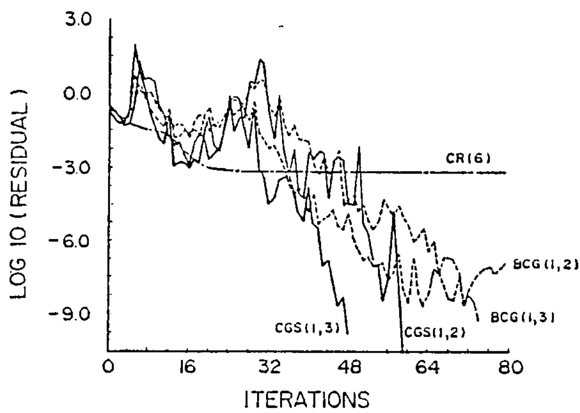

Fig.4 Convergence characteristics comparison for a static case.

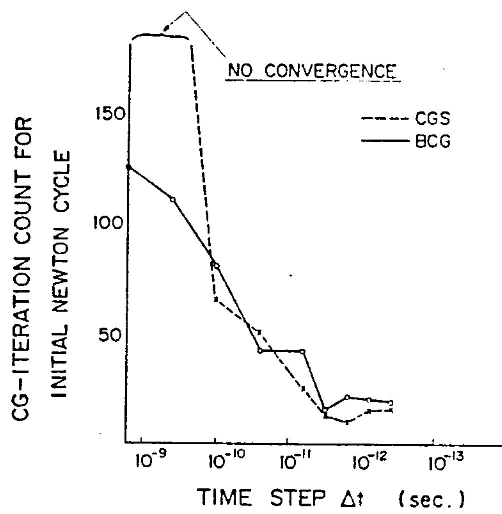

Fig.5 Convergence characteristics comparison for high voltage and transient cases. CG iteration number required for convergence in initial Newton cycle is shown as a function of time increment.

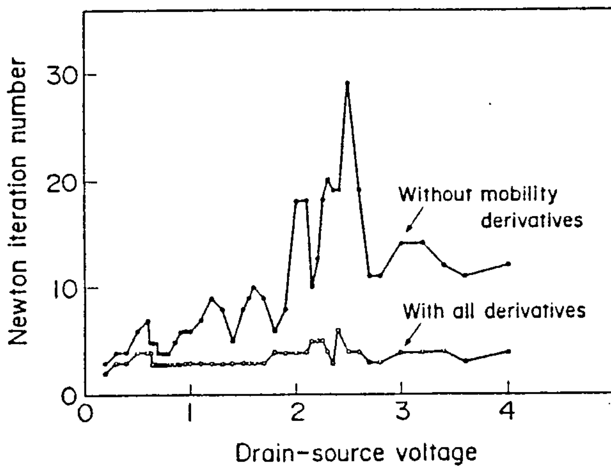

Fig.6 Newton iteration number vs. applied drain voltage, when the model simulates current voltage characteristics for a bipolar-mode MOSFET.

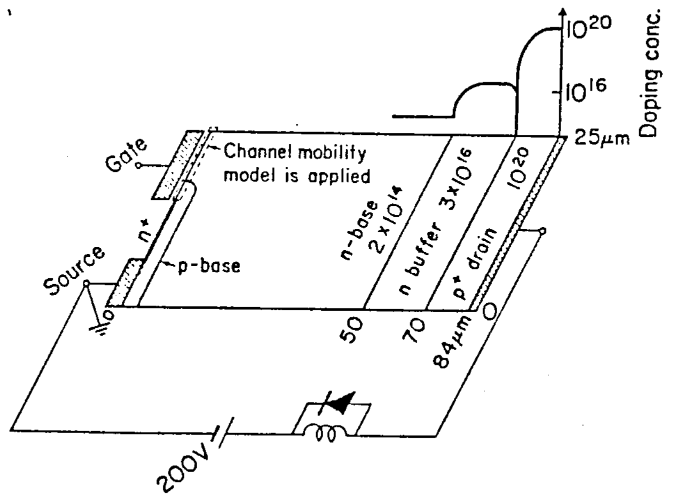

Fig.7 Analyzed bipolar-mode MOSFET structure and outer circuit.

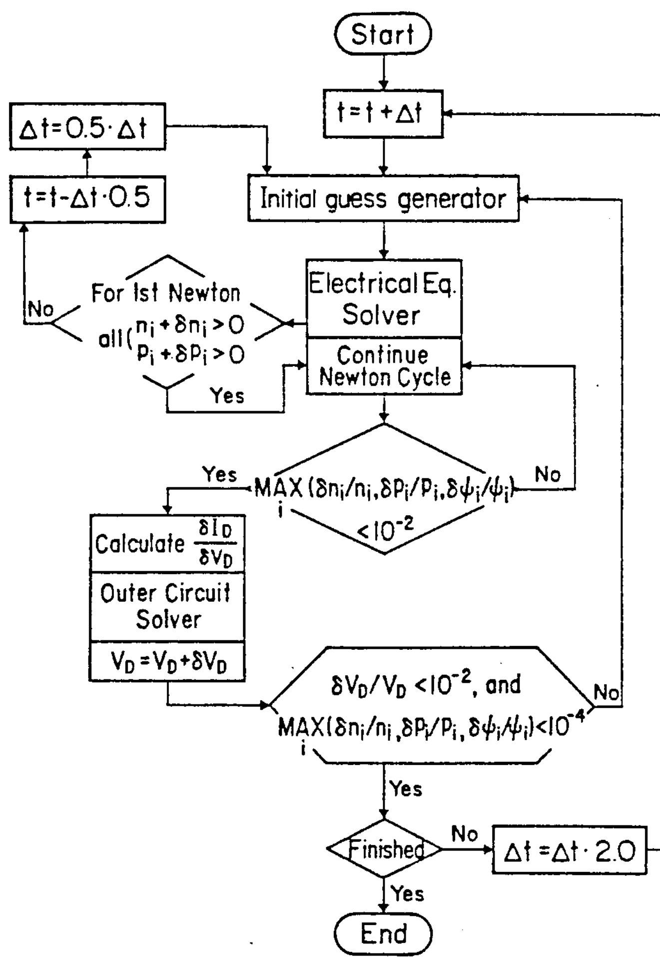

Fig.8 Flow chart for transient simulation.

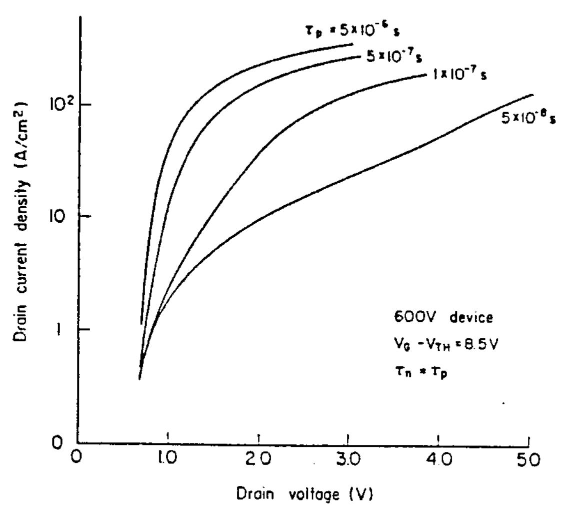

Fig.9 Current voltage curve for $\tau_n=\tau_p$ case with τ_p as a parameter.

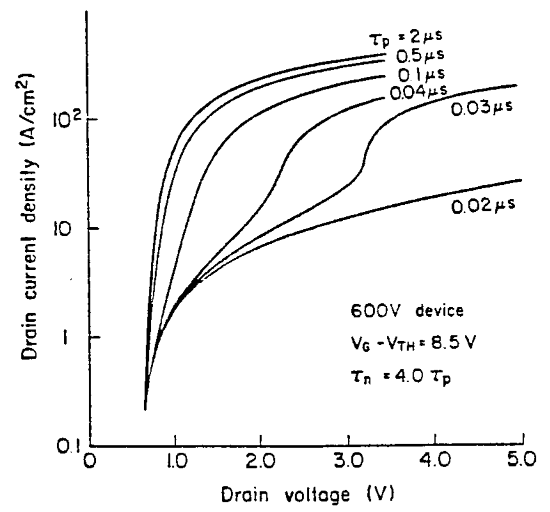

Fig.10 Current voltage curve for $\tau_n=4.0\tau_p$ case with τ_p as a parameter.

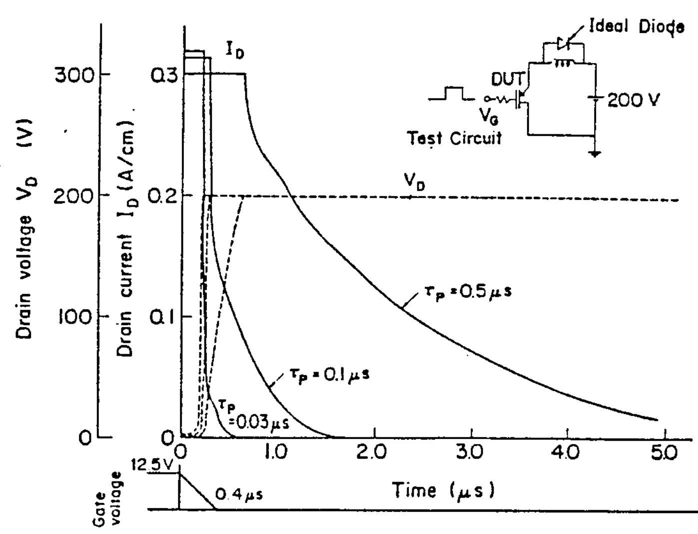

Fig.11 Simulated turn-off waveforms under an inductive load. Solid lines represent drain current and gate voltage waveforms and broken lines the drain voltage

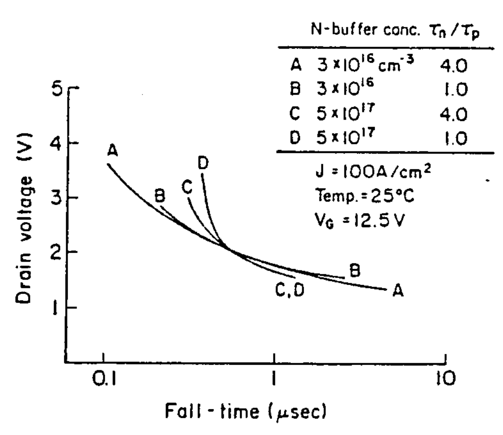

Fig.12 Calculated trade-off relations for various cases.