Safe Operating Area for 1200-V Nonlatchup Bipolar-Mode MOSFET's

AKIO NAKAGAWA, MEMBER, IEEE, YOSHIHIRO YAMAGUCHI, KIMINORI WATANABE, AND HIROMICHI OHASHI, MEMBER, IEEE

***Abstract*—This paper reports the safe operating area (SOA) for 1200-V nonlatchup bipolar-mode MOSFET's. The measured SOA limit, in terms of current density and drain-voltage product, reached 2.5×10^5 W/cm² for 125°C-case temperature and 10-μs pulse operation conditions. It exceeded even the so-called "avalanche limit" for n-p-n bipolar transistors when the measurement was carried out under 25°C-case temperature conditions. These SOA's enable device protection from an abnormally large drain-current surge.**

I. INTRODUCTION

THE BIPOLAR-MODE MOSFET, a new power MOSFET, appeared only several years ago [1], [2] and has evolved a great deal. It achieved a significantly low on-resistance [2], high voltage capability [3], and a high switching speed [4] along with MOS gate controllability. A variety of names such as COMFET [2], IGT [5], and GEMFET [6] were given to the same devices.

One significant problem associated with this device was latchup of the parasitic thyristor, which prevents device protection from abnormally large drain current in case of system failure. Regarding conventional transistors, protection circuits are used to reduce base currents to zero immediately after an abnormal increase in collector currents. The most serious case is where main loads become short circuited. In this case, collector currents increase so rapidly that no protection circuits can respond. Instead, the transistors themselves have to limit collector currents by increasing their forward voltage to as high as the electric-power-supply voltage, withstanding a large power dissipation for a short time interval so that protection circuits begin to work.

Recently, it was shown that nonlatchup operation can be achieved by a new design principle [7], setting the latchup current-density level far above the device saturation current for a gate voltage such as 20 V.

In the present paper, one method (the same as that used in [7]) for attaining this principle is presented. It will be shown that thusly designed bipolar-mode MOSFET's can be protected by the same type of protection circuits as those for bipolar transistors.

Manuscript received March 26, 1986; revised August 15, 1986.
The authors are with the Toshiba Research and Development Center, 1 Komukai Toshibacho, Saiwai-Ku, Kawasaki, 210, Japan.
IEEE Log Number 8611370.

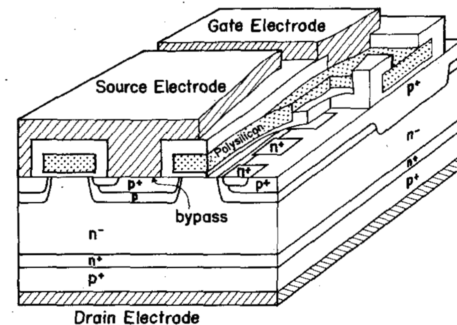

Fig. 1. Cross section of nonlatchup bipolar-mode MOSFET.

II. NONLATCHUP DESIGN AND ELECTRICAL CHARACTERISTICS

Fig. 1 shows a cross section of the developed nonlatchup bipolar-mode MOSFET. A part of the source n^+ layer is periodically eliminated, creating low-resistance bypasses for holes to reach the source electrode without passing under the source n^+ layer, effectively reducing the p-base resistance, which works as the shunting resistance for the parasitic n-p-n transistor. These hole bypasses simultaneously decrease the total channel width and, consequently, the saturation current. In order to further enhance the latchup current density, double p-base diffusion and a stripe source gate pattern were introduced. A shallow and high impurity concentration p^+ diffusion, which is carried out where part of the source layer is eliminated (bypass region), can greatly reduce the bypass resistance because it is not necessary to control the threshold voltage anymore in the bypass region. Thus, the hole-bypass structure, combined with a shallow diffusion, is a better method for reducing effective p-base resistance, compared with other methods such as a deep p-base or an additional deep p^+ diffusion [8].

The adopted stripe source gate pattern is superior to the widely used square patterns because the stripe pattern was found to be strongly effective to prevent local parasitic thyristor latchup [9]. Fig. 2 shows the effect of p-base diffusion depth on maximum controllable drain current when hole bypasses are not implemented. As the p-base diffusion becomes deeper, the maximum controllable current simply increases.

Implementation of all these combined technologies realizes nonlatchup operation, which means that static and

0018-9383/87/0200-0351$01.00 © 1987 IEEE

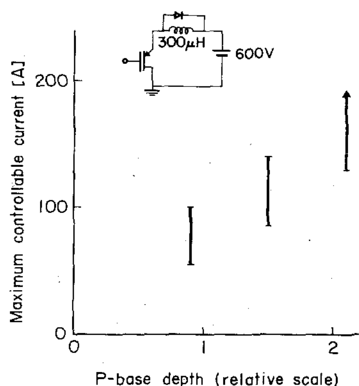

Fig. 2. Maximum controllable current versus p-base diffusion depth characteristics. Inserted diagram shows the circuit for maximum controllable current measurement.

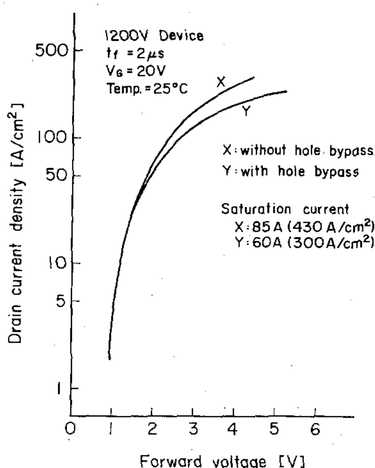

Fig. 3. Current–voltage curve comparison between devices with and without hole bypass structure.

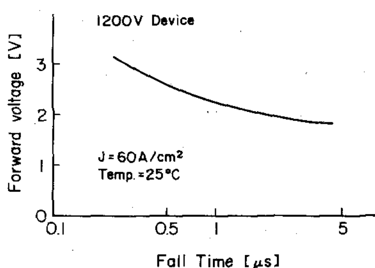

Fig. 4. Typical trade-off characteristics for 1200-V nonlatchup devices.

even dynamic parastic thyristor latchup never occurs for any condition if junction temperature is kept below 150°C and gate voltage is less than 20 V. These characteristics are described in more detail in the next section.

The present device design for nonlatchup operation sacrifices forward voltage drop for high current density level in some degree. Fig. 3 shows a comparison between current–voltage curves for devices with and without hole-bypass structures. The forward-voltage drop does not increase significantly at 60-A/cm^2 current density, which is set as the dc current rating for 1200-V devices. Fig. 4 shows typical trade-off characteristics between forward voltage versus fall-time. Although nonlatchup structure

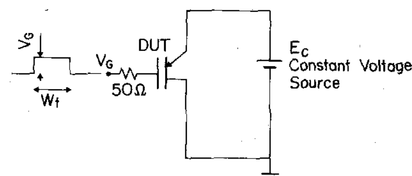

Fig. 5. Test circuit for short-circuited SOA measurement.

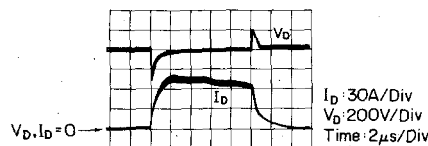

Fig. 6. Typical waveform for SOA measurement.

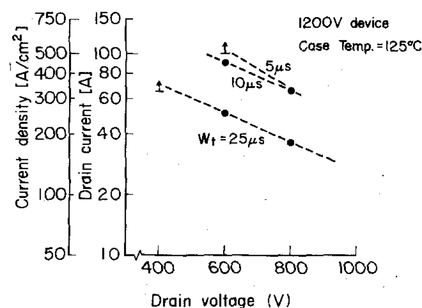

Fig. 7. Measured short-circuited SOA. Maximum drain current is plotted versus corresponding drain voltage with gate-pulse width as a parameter. The arrows means that the SOA limits are greater than those indicated values.

sacrifices forward voltage, a high switching frequency, such as 15 kHz, can still be attained in a reasonably low forward voltage for 60 A/cm^2 drain-current density. This 60 A/cm^2 current density is larger than those for 1000-V-rated conventional Darlington transistors (approximately 30 A/cm^2).

III. Safe Operating Area (SOA)

In this section, the safe operating area (SOA) will be presented from the viewpoint of device protection, as mentioned in the Introduction. A test circuit for this SOA measurement was set as shown in Fig. 5. A device under test was directly connected to a constant voltage supply, whose voltage was varied from 400 to 800 V. Then, 5- to 25-μs gate pulses were applied to the device. During the gate on-pulse, the devices were driven to stay in the current saturation region and then switched off at the end of the gate pulse. The gate voltage was changed within 500 ns from 20 to below −10 V. Forward voltage drop during the on-state was the same as the constant voltage supply voltage E_c. Maximum drain current was measured by slowly increasing the gate pulse voltage. The device case temperature was kept at 125°C during the measurement. Typical current voltage waveforms are shown in Fig. 6, where drain current gradually decreases during the on-state because of temperature increase within the device.

In Fig. 7, maximum drain currents at the end of the gate pulse were plotted versus the corresponding drain volt-

ages with the gate pulse width as a parameter. In the present paper, this kind of SOA (Fig. 7) is called a "short-circuited SOA" [10],[1] and is distinguished from the so-called forward SOA in the sense that the short-circuited SOA assures switching off. A short-circuited SOA is simply called SOA unless otherwise specified. Fig. 7 presents the results for devices with a 20-mm² active region and a 2-μs fall-time. Since device destruction occurred in the turn-off transients, the SOA was actually limited by switching characteristics such as maximum controllable current. Thus, if current–voltage locus for a device in the conduction state is within the SOA, it means that the device can be safely operated and even safely switched off. The SOA limit decreases as the conduction time width W_t (gate pulse width) increases. This is because the junction temperature increases during the on-state and because the maximum controllable current decreases as the temperature increases [3], [4]. This reason is further consistent with the fact that the measured SOA simply increases with decreasing case temperature as described below. The maximum power dissipation per 1 cm² reached 2.5×10^5 W/cm² for less than 10-μs pulse operation and 125°C-case temperature conditions as seen in Fig. 7. This power dissipation value exceeded 4×10^5 W/cm² when the measurement was carried out under 25°C-case temperature conditions. Since no second breakdown was observed in the steady state, the SOA limit lines in Fig. 7 approximately coincide with the constant power dissipation lines. It should be noted that the current–voltage curve for 20-V gate voltage is always below the SOA limit line for 10-μs pulse operation if the drain voltage is less than 800 V because the saturation current for 20-V gate voltage is 60 A at 125°C. This means that even if the drain current increases over the rated maximum current, devices can be protected from latchup because 1) drain current is limited by current saturation (channel pinchoff effects) and 2) it can be safely switched off by reducing the gate voltage to zero within 10 μs.

It was not confirmed that the measured SOA depends on the used gate resistance between the tested device and the gate circuit. Since a paper [5] mentioned the importance of the gate resistance, the used gate resistance was chosen to be sufficiently small so that it did not affect the turn-off time.

Fig. 6 indicates that, since in the turn-off transients the drain voltage exceeded the constant voltage supply voltage due to circuit stray inductance, its current voltage locus was outside the SOA limit line shown in Fig. 7 in the turn-off transients. This means that the SOA for switching transients is larger than the values given in Fig. 7.

Fig. 8 shows hole-bypass effects on a short-circuited SOA. The hole-bypass structures widen the SOA in addition to reducing saturation current. Thus, devices equipped with hole bypasses easily attain nonlatchup characteristics.

[1]Note that in [10] the term "forward SOA" is used instead of "short-circuited SOA."

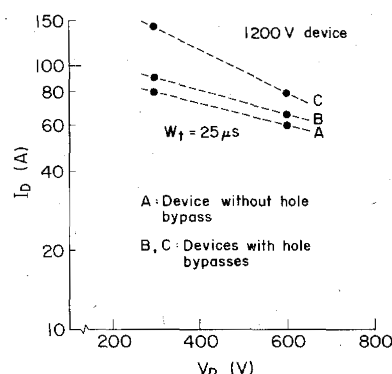

Fig. 8. Hole-bypass effects on short-circuited SOA. The bypass resistance for device *C* is lower than that for device *B*.

IV. Discussion

Since no second breakdown was observed during the on-state, only the SOA for switching transients is important. If a forward SOA is defined as the area that assures only steady-state operation and does not necessarily assure switching off, the forward SOA must be larger than the short-circuited SOA. In other words, a forward SOA is assumed to be limited by static latchup phenomena, which were never observed for any conditions in the present nonlatchup bipolar-mode MOSFET's if junction temperature was below a critical value and gate voltage was less than 20 V.

It was experimentally confirmed for n-p-n transistors that avalanche injection occurs in the collector region, when the drain-current density and voltage product exceeds a critical value such as 2.0×10^5 W/cm² [11]. Measured SOA limits for bipolar-mode MOSFET's exceeded this value especially for 25°C case temperature conditions and low carrier lifetime cases as mentioned in Section III. Similar avalanche injection phenomena were predicted to occur in the depletion region for bipolar-mode MOSFET's [10] for cases when all the current is carried by the p-n-p transistor portion after the channel electron current has completely ceased in the turn-off transients. A detailed theory is given in the Appendix. The measured SOA for 25°C seems to far exceed this theoretical limit also. The reason is under investigation.

Fig. 9 shows typical inductive switching waveforms when drain voltage was clamped by a freewheel diode. A 175-A drain current was switched off by a 20-mm² active region device. Fig. 10 shows the current–voltage locus corresponding to Fig. 9. The broken line in the figure is a theoretical border for avalanche injection given in the Appendix. The current density and voltage product reached 7×10^5 W/cm² in the turn-off transient.

It should be noted that the SOA for switching transients (maximum controllable current) is hardly affected by a negative gate bias application whereas those for bipolar transistors (RBSOA) are reduced significantly [12].

It is manifest that the measured SOA for bipolar-mode MOSFET's is greater than that for conventional bipolar transistors if a comparison is made for the same device area because allowable power dissipation for a 10-μs dc

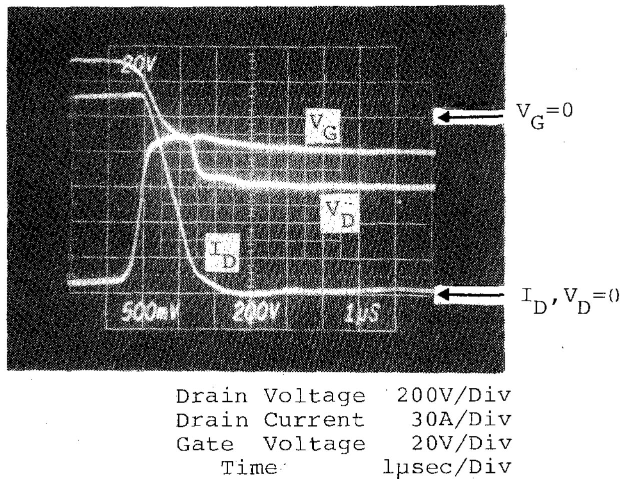

Fig. 9. Typical inductive load turn-off waveforms.

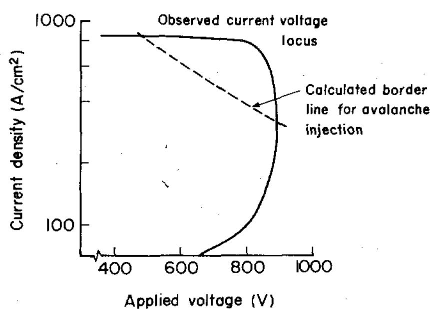

Fig. 10. Current–voltage locus corresponding to Fig. 9 and calculated border (broken line) beyond which avalanche injection may occur.

pulse was measured for a 1-cm^2 active region for bipolar-mode MOSFET's whereas the measured limit value 2×10^5 W/cm^2 for n-p-n bipolar transistors was for a 1-cm^2 emitter area [11]. Usually, the emitter areas in a bipolar transistor occupy only 30 or 40 percent of the total device area, whereas the active region occupies more than 60 percent of the device area. The superiority of bipolar-mode MOSFET's is more manifest for RBSOA.

V. Conclusion

Bipolar-mode MOSFET's achieved a sufficiently large SOA and complete compatibility with conventional power transistors when nonlatchup characteristics were realized by a hole-bypass structure and a stripe source gate pattern, etc.

Appendix

In the turn-off transients after channel electron current completely ceases, the net charge N^+ in the depletion layer is given by the sum of the donor and holes, which carries all the drain current. The net charge N^+, therefore, can be approximated by the following equation, assuming uniform hole current flow [10]:

$$N^+ = N_D + \frac{J(V_{th})}{qv_s} \ (\text{cm}^{-3}) \qquad \text{(A1)}$$

where N_D is the donor concentration (1×10^{14} cm^{-3} for 1200-V devices), v_s the saturated-hole velocity, and $J(V_{th})$ the drain-current density corresponding to a time when the gate voltage crosses the threshold voltage in the turn-off transients. Avalanche breakdown voltage simply decreases as drain-current density increases. The current–voltage relation for the avalanche breakdown can be approximately given by substituting (A1) into the following familiar expression for avalanche breakdown voltage:

$$V_{BD} = 60(E_G/1.1)^{3/2}(N^+/10^{16})^{-3/4}. \qquad \text{(A2)}$$

This $V_{BD} - J(V_{th})$ relation provides an avalanche injection limit for the device in the turn-off transients after channel electron current has completely ceased.

References

[1] B. J. Baliga, M. S. Adler, P. V. Gray, R. P. Love, and N. Zommer, "The insulated gate rectifier (IGR)," in *IEDM Tech. Dig.*, pp. 264–267, 1982.
[2] J. P. Russel, A. M. Goodman, L. A. Goodman, and J. M. Neilson, "The COMFET—A new high-conductance MOS-gate device," *IEEE Electron Device Lett.*, vol. EDL-4, pp. 63–65, 1983.
[3] A. Nakagawa, H. Ohashi, and T. Tsukakoshi, "High voltage bipolar-mode MOSFET's with high current capability," in *Ext. Abs. 16th Conf. Solid-State Devices Mater.*, pp. 309–312, 1984.
[4] A. M. Goodman, J. P. Russel, L. A. Goodman, C. J. Nuese, and J. M. Neilson, "Improved COMFETs with fast switching speed and high current capability," in *IEDM Tech. Dig.*, pp. 79–82, 1983.
[5] M. F. Chang, G. C. Pifer, B. J. Baliga, M. S. Adler, and P. V. Gray, "25 Amp. 500 volt insulated gate transistor," in *IEDM Tech. Dig.*, pp. 83–86, 1983.
[6] Designer's Data sheet DS 3621, Motorola Semiconductor Products Inc., Phoenix, AZ.
[7] A. Nakagawa, H. Ohashi, M. Kurata, Y. Yamaguchi, and K. Watanabe, "Non-latchup 1200 V 75 A bipolar-mode MOSFET with large ASO," *IEDM Tech. Dig.*, pp. 860–861, 1984.
[8] T. P. Chow and B. J. Baliga, "The effect of MOS channel length on the performance of insulated gate transistor," *IEEE Electron Device Lett.*, vol. EDL-6, pp. 413–415, 1985.
[9] A. Nakagawa and H. Ohashi, "600- and 1200-V bipolar-mode MOSFET's with high-current capability," *IEEE Electron Device Lett.*, vol. EDL-6, pp. 378–380, 1985.
[10] A. Nakagawa, Y. Yamaguchi, K. Watanabe, H. Ohashi, and M. Kurata, "Experimental and numerical study of non-latchup bipolar-mode MOSFET characteristics," in *IEDM Tech. Dig.*, pp. 150–153, 1985.
[11] H. Nishiumi, I. Takata, Y. Takagi, and S. Kojima, "High-power transistor modules for 440 V AC line voltage inverter applications," in *IPEC-Tokyo Conf. Rec.*, p. 297, 1983.
[12] D. L. Blackburn and D. W. Berning, "Some effects of base current on transistor switching and reverse-bias second breakdown," in *IEDM Tech. Dig.*, pp. 671–675, 1978.

*

Akio Nakagawa (M'82) was born in Hiratsuka City, Japan, on September 25, 1949. He received the B.Sc. and M.Sc. degrees in physics in 1972 and 1974, respectively, and the Ph.D. degree in electrical engineering in 1984, all from Tokyo University, Tokyo, Japan.

In 1974, he joined the Toshiba Research and Development Center, Toshiba Corporation, Kawasaki, where he has been engaged in the development of various power devices such as the GTO thyristor, low-loss high-efficiency diodes, power MOSFET's and bipolar-mode MOSFET's. Along with device development, he has been engaged in semiconductor device modeling. From September 1981 to February 1983, he was a Visiting Scholar in the Electrical and Computer Engineering Department of the University of Massachusetts,

Amherst. His research interests are mainly in semiconductor device development and modeling.

Dr. Nakagawa is a member of the Institute of Electronics and Communication Engineers of Japan.

*

Kiminori Watanabe was born in Kanagawa, Japan. He received the B.E. degree in electrical engineering from Science University of Tokyo, Japan, in 1983.

He joined the Toshiba Corporation, Kawasaki, Japan, in 1983, where he has been working in the area of power semiconductor devices.

Mr. Watanabe is a member of the Japan Society of Applied Physics.

Yoshihiro Yamaguchi was born in Fukushima, Japan, on April 30, 1952. He graduated from Fukushima Technical Senior High School in 1971.

In the same year, he joined the Toshiba Research and Development Center, where he has been engaged in the development of power devices such as GTO thyristors and light-triggered thyristors.

Mr. Yamaguchi is a member of the Institute of Electrical Engineers of Japan.

*

Hiromichi Ohashi (M'81) was born in Hamamatsu, Japan, on August 14, 1941. He received the B.S. degree in electrical engineering from Hosei University, Tokyo, and the M.S. degree in electrical engineering from Sophia University, Tokyo, in 1965 and 1969, respectively.

In 1969, he joined the Toshiba Research and Development Center, Kawasaki, Japan, where he was initially concerned with optical sensing devices development for an artificial satellite. Since 1972, he has been engaged in developing high-power new semiconductor devices, such as gate turn-off thyristors, light-triggered thyristors, bipolar-mode MOSFET's (IGBT), and so on. He is presently the Senior Researcher in the power semiconductor devices group of the Electron Devices Laboratory.

Mr. Ohashi is a member of the Institute of Electrical Engineers of Japan.