# A Study on GTO Turn-Off Failure Mechanism—A Time- and Temperature-Dependent 1-D Model Analysis

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*Abstract*—A 1-D model is presented for use in analyzing the GTO thyristor turn-off process, including the conduction region squeezing effects as well as the current due to temperature variation, i.e., thermal diffusion and the current due to bandgap variation with temperature change. The model simulates current-voltage characteristics for the current concentrated area, where the current density increases almost linearly with the anode voltage. It is found that the nonuniformity in the p-base sheet resistance is a significant cause for the current concentration because of the enhanced $dv/dt$ current due to the excess carrier removal from the highly injected n-base. The model also predicts the limitation to the anode voltage imposed on the device before the current is completely turned off.

## I. Introduction

RECENTLY, GTO's have gained much attention due to their achieving high self-turn-off capability as well as high blocking voltage [1], [2]. However, the turn-off process, including the failure mechanism, has not yet been fully analyzed in spite of their importance.

The GTO device reveals an interesting phenomenon in the turn-off process, so called conduction region squeezing, which was first analyzed by Wolley [3] in 1966. In 1974, Kurata [4] tried to simulate the process using a two-section charge control model. Then, in 1979, a 1-D numerical model was introduced by Naito *et al.* [5] to analyze the turn-off process.

In the present paper, an analysis is given upon the turn-off failure process with a high anode current by using a 1-D model. An effort is made to include the conduction region squeezing effectively in the 1-D model, based on results of an experiment [6], which was conducted by the authors in 1981, using infrared measurement. The assumptions adopted in the 1-D model are also confirmed by executing a 2-D model calculation [7] separately, which reveals the 2-D squeezing process in detail. Special efforts are also made on the analysis of the cause for the current concentrating into a small portion of the device in the turn-off process.

This paper deals with the theoretical part of the consecutive works. The experimental analysis will be published separately in the same journal [6].

## II. One-Dimensional Device Model

### A. Mathematical Model

In order to predict precise device characteristics, the model should include various higher order effects, such as heavy doping effects (HDE) [8]-[11], carrier degeneracy, mobility reduction due to carrier-carrier scattering [12] as well as electric field, Auger recombination, etc. There have been numerous publications regarding HDE and degeneracy [8]-[11]. However, the most suitable treatment for the numerical calculation is to introduce the following parameter $\omega$ for the effective band edge shift, taking both effects into account simultaneously [13].

$$N_{c0}\exp\frac{1}{kT_0}(q\omega_n + F_n - E_{c0}) \equiv \int \frac{\rho(E)dE}{1+\exp\frac{1}{kT_0}(E-F_n)} \tag{1}$$

where $E_{c0}$ shows the conduction band edge energy for non-doped silicon. Then, it is easy to derive the current equation (2) for electrons for the degeneracy case [13].

$$J_n = \mu_n kT_0\frac{\partial n}{\partial x} - q\mu_n n\frac{\partial}{\partial x}(\psi + \omega_n). \tag{2}$$

The classical Einstein relation still can be used. However, the real situation is that the deviating part of the current from the Einstein relation is removed from the diffusion term and is treated as if it were a drift term, which is expressed in terms of $\omega_n$ in (2). Parameter $\omega_n$ includes HDE and degeneracy simultaneously, and enables rapid calculation because it is not necessary to calculate diffusion coefficient and mobility ratio, any more.

If the temperature distribution inside a device is not uniform, two additional current terms have to be included. One is the so-called thermal diffusion [14], expressed by the following equation

$$qn\,D_T\frac{\partial T}{\partial x},\quad \left(D_T = \frac{k}{2q}\mu_n\right). \tag{3}$$

Coefficient $D_T$ can be expressed easily as seen in (3) if only accoustic scattering is considered for the major relaxation process. The other term comes from the bandgap change due to temperature variation and can be expressed by (4), assuming that the two band edges change equally.

$$-\frac{1}{2}q\mu_n n\frac{\partial \Delta V_G}{\partial x} = -q\mu_n ns\frac{\partial T}{\partial x}$$

$$2s = 2.82\times 10^{-4}\ (\text{V/deg})\ [15]. \tag{4}$$

This term is greater than (3) and has an opposite sign. Thus it should be included together with (3). The current equations

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to be solved are

$$J_n = \mu_n kT \frac{\partial n}{\partial x} - q\mu_n n \frac{\partial}{\partial x}\psi_e \tag{5}$$

$$J_p = -\mu_p kT \frac{\partial p}{\partial x} - q\mu_p p \frac{\partial}{\partial x}\psi_h \tag{6}$$

$$\psi_e = \psi + \omega_n + \left(s - \frac{k}{2q}\right) T \tag{7}$$

$$\psi_h = \psi - \omega_p - \left(s - \frac{k}{2q}\right) T \tag{8}$$

where $\omega_p$ is a similarly defined parameter for holes. Quantities $(\omega_n + sT)$ and $(\omega_p + sT)$ express the effective band edge shifts for electrons and holes at temperature $T$. $\omega_n$ and $\omega_p$ should be assumed to be equal because the same assumption was already used for the temperature dependent part $sT$ and can be proved not to introduce a large error [16].

In the following, the value $s$ will be shown to be constant if the doped impurity concentration is less than $1 \times 10^{19}$ $cm^{-3}$. From the definition, the following expression holds for the thermal equilibrium case.

$$n_i^2 = C T^3 \exp\left\{-\frac{1}{kT}[(E_{c0} - E_{v0}) - q(\omega_n + \omega_p + 2sT)]\right\}. \tag{9}$$

On the other hand, Slotboom *et al.* [11] showed that intrinsic concentration $n_i$ follows (10) if the doped impurity concentration is less than $1 \times 10^{19}$ $cm^{-3}$.

$$n_i^2 = 9.6 \times 10^{32}\ T^3 \exp -\frac{q}{kT}[1.206 - \Delta V_{g0}]. \tag{10}$$

Comparing (9) and (10), the following results are easily reached.

$$\omega_n + \omega_p = \Delta V_{g0} \tag{11}$$

$$s = \frac{k}{2q} \ln\left(\frac{9.6 \times 10^{32}}{C}\right). \tag{12}$$

Equation (12) indicates that value $s$ is a constant independent from the impurity concentration less than $1 \times 10^{19}$ $cm^{-3}$. Using (11), $\omega$ values are easily determined by experiments under the assumption that $\omega_n = \omega_p$.

Regarding carrier mobilities, there has been no simple empirical formula which treat their dependence on temperature, injected carrier density, impurity density etc. Thus the author made a tentative expression to include all of them. First, a simple expression was made so as to fit the temperature and impurity density dependence data [17], assuming different temperature coefficients for the impurity scattering and for the rest of the scattering mechanism. The carrier density is simply added to the impurity density with a proper weighting coefficient, assuming that the carrier-carrier scattering is basically the same as the impurity scattering.

Carrier lifetimes for electrons and holes are assumed to be the same and vary depending upon the impurity concentration. A value of 5 $\mu$s will be used for the lifetime value in the n-base, if not otherwise specified. The temperature dependence of the carrier lifetime is ignored because of its complexity and the lack of sufficient data.

### B. Solution Method

If two different effective potentials, $\psi_e$ and $\psi_h$, are introduced for electrons and holes, respectively, the current equations have exactly the same form as the conventional one. Then, the same discretization procedure can be applied under the following approximation: 1) The apparent diffusion coefficient between the two grid points is $\mu kT^M$, where $T^M$ is the average temperature between the two points. 2) The effective field defined by $(-\partial\psi_e/\partial x)$ is constant between the two grid points. The discretized current equation is given as

$$J_n(M) = \frac{q}{h(M)}[a_n(M)n(N) + b_n(M)n(N+1)]$$

$$\begin{cases} a_n(M) = \mu_n(M)\,\beta(M)/\{\theta(1 - \exp\beta(M))\} \\ b_n(M) = \mu_n(M)\,\beta(M)/\{\theta(1 - \exp-\beta(M))\} \end{cases}$$

$$\theta = q/kT^M,\ \beta(M) = \theta(\psi_e(N) - \psi_e(N+1)). \tag{13}$$

The heat equation has to be solved together with electrical equations (Poisson, current continuity equations). The best method for the problem is to treat the heat equation, separately because the interaction between heat equation and electrical equations is rather small. However, the simultaneous solutions for four equations can be obtained at each time step by the same procedure as the so-called Gummel's technique. The Newton cycles for electrical equations and for the heat equation are repeated several times at each time step until the simultaneous 4 solutions $(n, p, \psi, T)$ are obtained. When temperature correction $\delta T$ for a Newton cycle is large, the following updating process is adopted

$$T^{m+1} \leftarrow T^m + x \cdot \delta T \tag{14}$$

$(0 < x < 1.0)$.

The voltage control type boundary condition ($\psi$: specified) is applied to both emitter contacts. For the gate contact, the following special condition is applied [5].

$$J_G = \frac{E_G - [\psi(x_g) - \psi_0(x_g)]}{R_G} \tag{15}$$

with

$$\psi(x_0) = \psi_0(x_0)$$

where $x_g$ and $x_0$ denote the point where the gate contact is placed and the n-emitter surface, respectively. $\psi_0$ represents zero bias solution and $E_G$ and $J_G$ mean the gate electric source voltage and the gate current density, respectively.

Since this condition specifies the gate current value, which is given by (15), this can be referred to as the current control type condition.

It was found that the turn-off characteristics are very sensitive to the selection of the $x_g$ location. A larger gate current density is required to turn-off the device as $x_g$ goes remote from the center junction. This is because the stored charges in the p-base have to be extracted before those in the center junction

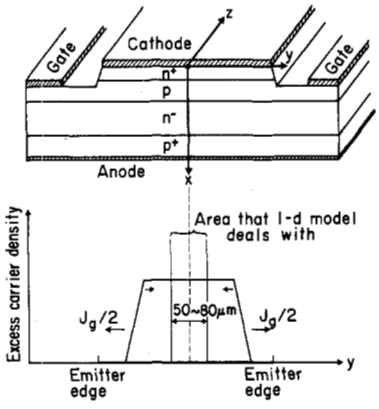


Fig. 1. Schematic diagram of the GTO thyristor and excess carrier change in the p-base.

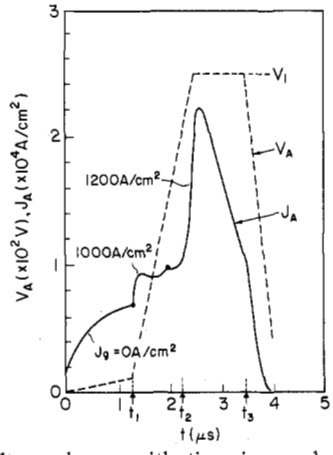


Fig. 2. Anode voltage change with time imposed on the device and calculated current density change with time for the current concentrated area.

are removed if $x_g$ is set remote from the center junction. On the other hand, the carrier density around the center junction is easily reduced and the device resistance increases more rapidly if $x_g$ is chosen near the center junction. This is a serious problem associated with the 1-D model. In this paper, the $x_g$ location is chosen to be at the highest impurity density point in the p-base because the gate current has to flow laterally in the p-base from the reduced conduction region to the gate metal in an actual device and most likely passes through the lowest resistance path.

### C. One-Dimensional Model

In this section, a one-dimensional model taking into consideration the conduction area squeezing is proposed. Fig. 1 shows the schematic carrier density distribution along the $y$-axis, which is defined in the same figure. The lateral gate current flows in the p-base, depending upon the carrier density gradient at the edge of the conduction region. While the conduction region is being squeezed, it can be assumed that the carrier density sufficiently inside the conduction region is not affected by the gate current, but is affected by the anode voltage increase caused by the reduction in the conduction region. In other words, when the periphery of the conduction region is turned off, the device resistance increases and causes an increase in the anode voltage through the external circuit equations, resulting in an increase in the current density in the conduction region. The validity of this assumption can be confirmed by the results of a 2-D model simulation [7]. Thus if attention is only paid to the center of the conduction region, the effects of the gate current can be ignored and only the anode voltage should be increased, corresponding to the decrease in the conduction region. When the conduction region is reduced to a certain limit (for example, the diffusion length for the carriers), the carrier density inside the conduction region begins to be extracted by the gate current. The conduction region width remains the same thereafter until the whole device is turned off. This fact was also confirmed by both experiment [6] and 2-D calculation [7]. The final width was estimated to be 80 $\mu$m from the experiment or 50 $\mu$m from the calculation. Based upon the above considerations, the 1-D model will be realized by the following assumptions.

1) Only a device portion as narrow as 80 $\mu$m (or 50 $\mu$m) where the final conduction region appears, is taken into consideration by the 1-D model.

2) Until a certain time; while the conduction area is being squeezed; only the anode voltage is increased.

3) Then, suitable gate current is applied to the device and the anode voltage rising rate is also increased. By the above process, the 3-D squeezing process for the conduction region can be effectively considered.

## III. Calculation Results

In this section, results calculated by the 1-D model are presented. Actual calculation procedures are as follows.

1) Obtain steady-state solutions for the anode current of 1500 A/cm$^2$.
2) Increase the anode voltage at a rate of 7.5 V/$\mu$s to express the conduction region squeezing.
3) After the anode voltage reaches 11.0 V, apply off-gate current of 1000 ~ 1200 A/cm$^2$ to the model and also increase the anode voltage at a rate of 200 V/$\mu$s.
4) Keep the anode voltage constant after it reaches 250 V.

This calculation is based on the experimental data, which was presented in Fig. 3 in [6]. The experiment was carried out under the high current condition so that a significant current concentration into a small portion of the device was brought about.

Fig. 2 shows the anode voltage waveform which was used for the calculation. Giving the anode voltage variation *a priori* is a rather crude approximation. However, this process can be justified by the following consideration: 1) The anode voltage change is based on the experimental results. 2) The voltage increase rate can be changed rather arbitrarily by the attached snubber circuit. Therefore, the calculated results can be considered to reflect the actual situation although there is a little unreality. Fig. 2 also shows the calculated current density change, which should be attributed to that for the current concentrated area. After 1.3-$\mu$s time elapse, the gate current density of 1000 ~ 1200 A/cm$^2$ is applied. Nevertheless, the anode current density increases monotonically until 2.7 $\mu$s have elapsed. This means that the used gate current density is not

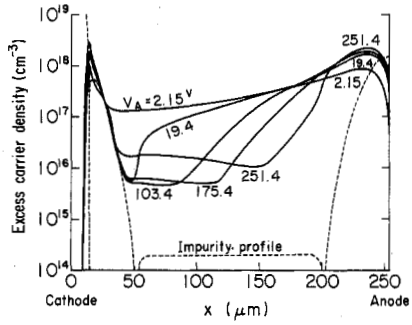


Fig. 3. Excess carrier distributions for various time steps denoted by corresponding anode voltages.

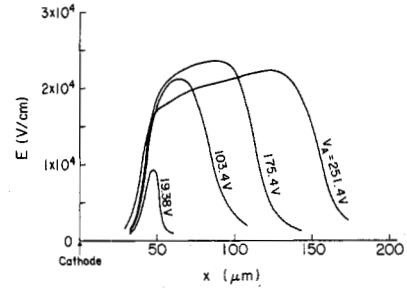


Fig. 4. Electric field distributions for various time steps denoted by corresponding anode voltages.

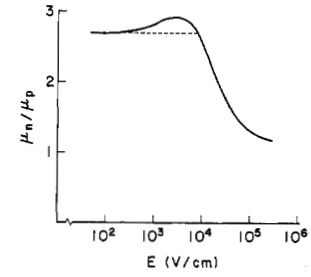


Fig. 5. Mobility ratio versus electric field characteristic generated by empirical formula used in the model.

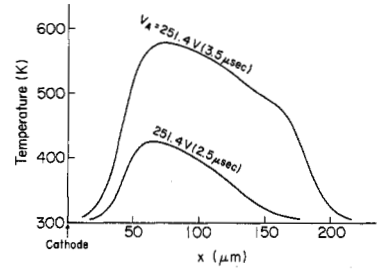


Fig. 6. Temperature distributions inside the device for the two time steps.

sufficient to turn off the device while the anode voltage is increasing. The applied gate current density is also determined, based on the same experiment, by measuring the gate current value and the corresponding conduction area from the change in the gate-emitter resistance as well as the infrared observation results. Fig. 3 shows excess carrier density distributions inside the device for the various anode voltages. The curve assigned as $V_F = 2.15$ V shows the initial state ($t = 0$). As the applied voltage increases, the excess carriers around the center junction are reduced due to the high electric field there. The interesting fact is that the high electric field magnitude does not exceed a certain value ($\sim 2.5 \times 10^4$ V/cm for the present case), but the high electric field region width extends toward the p-emitter as shown in Fig. 4. In the high electric field region, the current flows almost by drift so that the ratio of the electron current density over the hole current density $J_n/J_p$ is almost equal to the mobility ratio $\mu_n/\mu_p$. The mobility ratio tends to decrease monotonically from 2.7 to 1.2 as the electric field increases over $1 \times 10^4$ V/cm (see Fig. 5). Accordingly, the electric field magnitude is approximately determined by the ratio of $J_n/J_p$. In other words, if the current ratio $J_n/(J_n + J_p)$ at the center junction falls on a point between 0.73 and 0.55, the corresponding electric field, ranging from $1.0 \times 10^4$ to $1 \times 10^5$ V/cm, appears around the center junction as the anode voltage increases. However, if the ratio $J_n/(J_n + J_p)$ is below 0.55, the corresponding electric field exceeds $1 \times 10^5$ V/cm and will form a depletion layer at the center junction. The electric field in the present calculation is about $2 \times 10^4$ V/cm, which is far less than the electric field magnitude in the ordinary depletion layer. Thus the high electric field region easily extends far into the n-base even if the anode voltage is not high enough. In the high electric field region, carrier density is as low as $10^{15} \sim 10^{16}$ cm$^{-3}$ so that the recombination rate there is very small as compared with that in the rest of the region. It follows that the ratio $J_n/J_p$ does not change significantly within the high electric field region, resulting in fairly uniform electric field distribution. The wide high electric field region increases the device current because the carrier density decreases rapidly from the p-emitter towards the edge of the high electric field region and because this carrier density gradient becomes steeper as the high electric field region expands.

Calculated carrier density distributions (Fig. 3) show a good agreement with the corresponding experimental results presented in Fig. 3 in [6] in the following respects: 1) High carrier injections are seen near both emitters. 2) The carrier density inside the n-base realizes U-shape distribution because of the wide high electric field region. (Readers should be aware of the difference in the scales between the two figures. One is logarithmic and the other is the square of the density.)

Fig. 6 shows the calculated temperature distributions inside the device. The figure agrees well with the experimental results [6].

Analysis is continued as to Fig. 2. Anode current density decreases drastically after the anode voltage becomes constant (250 V). Thus it is the anode voltage increase rather than the anode voltage itself that most influences the current concentration during the turn-off process. This is because increasing the anode voltage causes an additional current flow due to the removal of the stored charge in the n-base because of the high electric field region expansion. The amount of carriers removed from the n-base is much larger than that due to the depletion layer expansion because the electric field in the depletion layer is much higher than that in the present high electric field region. This current works as positive gate current and makes the situation worse. The same result as in the present case was also observed in the following experiment. Fig. 7 shows several wave-

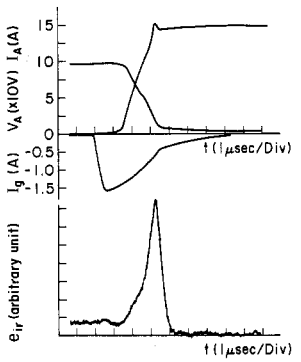


Fig. 7. Experimentally obtained turn-off waveforms and the infrared emission intensity change from the current concentrated area, which reflects the current density change there.

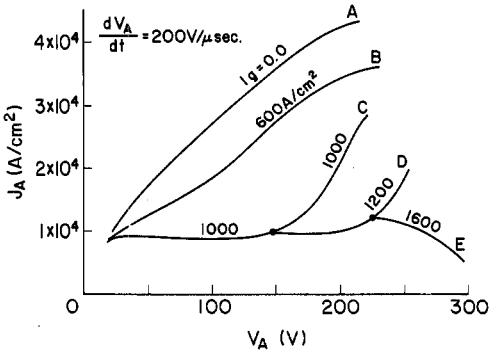


Fig. 8. Anode current density changes plotted versus corresponding anode voltages which change at the rate of 200 V/μs with gate current density as a parameter.

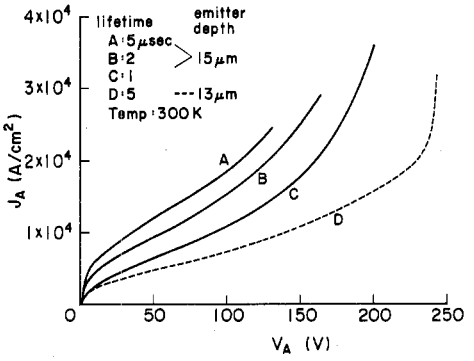


Fig. 9. Steady-state forward high current–high voltage characteristics.

forms obtained by an experiment similar to mentioned in [6]. The upper curves represent the anode voltage, anode currents, and the gate current, respectively. The lower trace shows the infrared intensity observed from the current concentrated area in the device. This is assumed to be in proportion to the current density there. It is easily recognized that the current density in the current concentrated area begins to decrease when the anode voltage reaches its peak value and its rising rate becomes zero. These experimental and calculated results clearly indicate that the turn-off failure is caused by the fact that there is always a place where the current density increases monotonically with the increase in the anode voltage because of the insufficient supplied gate current. The current density in the current concentrated area still can be decreased after the anode voltage becomes constant (either after it reaches its peak value or after the total device current is almost turned off). However, if the heat dissipation is sufficiently high in the current concentrated area, the thermally induced current becomes large enough as compared with the supplied gate current, causing turn-off failure. The same 1-D model can be utilized to simulate the above situation. The authors confirmed that if the temperature elevation is high enough (>700°C: $n_i^2 >> p \cdot n$), the device cannot be turned off by the ordinary gate current density. The critical temperature obtained from the model is not fully reliable because it is not clear how the carrier lifetime depends on temperature. However, the above stated failure mechanism is quite consistent with the experimental results presented in [6].

## IV. Analysis for the Current Crowding Case

If the device is a narrow, long rectangle and the turn-off characteristics are uniform throughout the device, then the turn-off process proceeds uniformly. The final conduction region is very narrow, but its length is almost as great as the emitter length. However, in an actual device, while the turn-off process goes on, the conduction region shrinks in the emitter length direction as well as in its width direction, resulting in the current concentration into a small region. These facts were observed by experiment [6], which confirmed that the current density in the area where the current concentration occurs increases linearly with the increase in the anode voltage.

In this section, a 1-D model is used to analyze the cause for the current concentration. Fig. 8 shows the anode current density changes for various gate current densities when the same anode voltage waveform as shown in Fig. 2 is applied.

Curve *D* in Fig. 8 shows the same calculated result as was given in Section III. It is recognized that the anode current density strongly depends on the gate current density. For example, a 20-percent difference in the gate current density causes more than 5000 A/cm² anode current density difference when the anode voltage reaches 150 V.

The next paragraph reports results obtained from an examination on the effects of the difference in the impurity profile, especially in the p-base impurity density. Fig. 9 shows the various steady-state current-voltage (*I-V*) characteristics for devices with two different doping profiles. For simplicity, the steady-state *I-V* characteristics are used instead of the transient characteristics. It is seen, from curves *A* and *D*, that the 2-μm emitter diffusion depth difference (all other diffusion parameters being the same) gives a large current density difference, which is much larger than the change due to the carrier lifetime difference (see curves *A*, *B*, and *C*).

In order to determine the significance of the p-base sheet resistance difference, a GTO device, which has a place whose p-base sheet resistance is 1.2 times as high as that for the rest of the device area, will be examined as an example. It can be expected that the current density of the squeezed conduction region in the 20-percent higher p-base sheet resistance area is much higher than that in the rest of the device area. This is because not only is the original device on-resistance lower, but also the 20-percent less gate current is supplied to the squeezed

conduction region in the 20-percent larger p-base sheet resistance area since the gate current has to flow through the p-base laterally from the squeezed conduction region to the gate metal. Thus the p-base sheet resistance difference brings about two causes for current concentration: 1) The device on-resistance difference (Fig. 9). 2) The supplied gate current difference.

On the other hand, temperature increase inside the device is usually considered to be the cause for the current concentration. However, this is not a main cause for the following two reasons: 1) The current density for a relatively high anode voltage usually decreases as temperature increases. 2) The temperature measurement results show that the current concentration begins before a significant temperature increase.

In the following, a more detailed analysis will be given for the reason behind the current concentration, which occurs while the anode voltage increases. Turn-off gain $G$ and current gain $\alpha_{\text{n-p-n}}$ for the n-p-n transistor portion are defined by the following expressions, using electron and hole current density values $J_{nc}, J_{pc}$ at the center junction.

$$G \equiv (J_{nc} + J_{pc})/J_g \tag{16}$$

$$\alpha_{\text{n-p-n}} \equiv J_{nc}/(J_{nc} + J_{pc} - J_g). \tag{17}$$

In the above expressions, the quasi-static approximation is adopted for simplicity and both the current due to the change in the stored charge and the displacement current are neglected. Equations (16) and (17) lead to (18).

$$\frac{J_{nc}}{J_{pc}} = \frac{\alpha_{\text{n-p-n}}(G - 1)}{G(1 - \alpha_{\text{n-p-n}}) + \alpha_{\text{n-p-n}}}. \tag{18}$$

In the high electric field region, $J_{nc}/J_{pc}$ is approximately equal to $\mu_n/\mu_p$ (under the high injection condition $n \cong p$).

$$\frac{\mu_n(E_h)}{\mu_p(E_h)} \cong \frac{\alpha_{\text{n-p-n}}(G - 1)}{G(1 - \alpha_{\text{n-p-n}}) + \alpha_{\text{n-p-n}}}. \tag{19}$$

This equation determines electric field magnitude $E_h$ in the high electric field region. On the other hand, the amount of carriers removed by the high electric field region expansion is given by (20).

$$\Delta n = n \frac{\partial W}{\partial t} = \frac{n}{E_h} \frac{\partial V_a}{\partial t} \tag{20}$$

where $W$ is the high electric field region width. The appropriate values, which were obtained from the calculation in Section III, can be used to estimate $\Delta n$. The value $q \cdot \Delta n$ is 160 A/cm$^2$ if $n \sim 10^{17}$ cm$^{-3}$, $E_h \sim 2 \times 10^4$ V/cm and $\partial V_a/\partial t = 200$ V/$\mu$s. This current is amplified by the 2 transistors and plays a key role in the current concentration.

Electric field $E_h$ depends on $G$ and $\alpha_{\text{n-p-n}}$ as seen in (19). As the p-base sheet resistance becomes higher, not only $\alpha_{\text{n-p-n}}$ but also $G$ become higher if the applied gate voltage remains the same. Equation (19) is a monotonically increasing function of both $G$ and $\alpha_{\text{n-p-n}}$. Thus if the p-base sheet resistance is higher, the appearing electric field $E_h$ is smaller and the high electric field region is wider for the same anode voltage. It follows that more carriers are removed from the n-base. These carriers become positive gate current and cancel a part of the negative gate current. These mechanisms are considered to sustain the anode current in the current concentrated area.

## V. Discussion

In this section, considerations are given to the maximum anode voltage which can be applied to the device. As the applied voltage increases, the anode current density increases drastically as seen in Fig. 9. These phenomena imply that there is a limitation to the applied voltage.

If the supplied gate current is insufficient, gain $G$ is high. Consequently, the value $E_h$ is low. Then, the high electric field region easily expands widely in the n-base and approaches the p-emitter. If the anode voltage further increases, the electric field in the high electric field region is forced to increase because the high field region cannot expand into the p-emitter. However, the electric field magnitude cannot be easily increased because it directly decreases mobility ratio $\mu_n/\mu_p$, thus current ratio $J_n/J_p$. Therefore, there must be a change in the total anode current density when the electric field magnitude increases. The ratio $J_n/J_p$ automatically decreases if the anode current density decreases, because $J_p$ includes the gate current density, which does not need to decrease. On the other hand, if the gate current is not sufficient, then the anode current density must increase rapidly with the increase in the anode voltage. This situation accelerates the current concentration because gain $G$ must decrease with the increase in the anode current density. This is very similar to the situation in Fig. 9.

If the device has fluctuations in the turn-off characteristics, it is necessary to avoid a high anode voltage large enough to cause the wide high electric field region in the n-base, before the anode current is completely turned off. This anode voltage can be estimated from (19) by setting $G \gg 1$. If the value of 0.67 is assumed for the $\alpha_{\text{n-p-n}}$, for example, the $E_h$ value is estimated to be $2 \times 10^4$ V/cm. Thus the maximum anode voltage can be predicted by the following equation.

$$V_a\,(\text{Max}) \cong E_h \cdot W_{NB}, \ (W_{NB}: \text{n-base width}) \tag{21}$$

This calculated value coincides with the actual critical anode voltage $V_1$ when the turn-off failure occurs [6].

The recent experiment by Nagano *et al.* [18] also supports this idea. The maximum controlable anode current drastically decreases as the applied anode voltage increases over the critical anode voltage.

## VI. Conclusion

A 1-D GTO turn-off model, effectively including the conduction region squeezing process, was presented. It was shown that the current term due to bandgap variation with temperature should be included as well as thermal diffusion term.

A turn-off process was simulated using the 1-D model, based on the experimental data from [6], revealing the following results:

1) In the case of high current turn off, the current density in the current concentrated area increases with the increase in the anode voltage, and eventually decreases after the anode voltage increase rate approaches zero.

2) The nonuniformity in the p-base sheet resistance was found to be a significant cause for the current concentration.

3) $dV/dt$ current due to the removal of stored charges in the n-base plays an important role on the current concentration.

4) There is a limitation to the anode voltage value applied in the turn-off process, which is far less than the static device breakdown voltage.

5) The 1-D model predicts that the turn-off failure can be caused by a local temperature increase which generates thermal current comparable to the gate current.

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# Surface Induced Latchup in VLSI CMOS Circuits

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*Abstract*—**Experimental as well as theoretical results on the latchup effect in CMOS structures with and without an epitaxial layer are presented. In structures with an epitaxial layer the critical current for latchup firing is two orders of magnitude higher and latchup is essentially surface controlled. The strong surface effect observed is a consequence of the gate influence of surface conduction of the field oxide MOSFET's and on current gains of the bipolar transistors. Latchup sensitivity can be decreased by increasing $p^+$/p-well and $n^+$/n-well spacing, by decreasing expitaxial layer thickness and by increasing substrate doping. In reducing the lateral dimensions, short-channel effects of the field oxide transistors imply the most severe limitations for latchup immunity.**

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## I. Introduction

HIGH-SPEED and high packing density CMOS needs reduced feature sizes and low parasitic capacitances and resistances. Lowering the doping concentration in the n- and p-well to achieve low junction capacitances and reducing the feature sizes is limited by the increasing latchup sensitivity. It is well known however, that latchup stability is strongly enhanced by the use of a lowly doped epitaxial layer on a highly doped substrate [1], [2], [3]. [4]. The gain, however, in stability due to epitaxy can be considerably reduced by surface fields induced by wiring lines crossing the p-well/n-well junction region which act as gate electrode on the top of the field oxide [5].

In this paper we present experimental as well as theoretical results on the latchup effect of CMOS structures with and without an epitaxial layer. It will be shown that latchup in

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