600- and 1200-V Bipolar-Mode MOSFET's with High Current Capability

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Abstract—**600-V 25-A and 1200-V 20-A bipolar-mode MOSFET's (T-BIFET) with 100-A and 75-A maximum current capability, respectively, have been developed, based on a new pattern design theory for high latch-up current density. It is also shown than an n^+-buffer layer improves a tradeoff between the forward voltage and the turn-off time, compared with an ordinary n-buffer layer.**

I. INTRODUCTION

A NEW POWER MOSFET, recently proposed by Becke and Wheatly [1], provides not only switching-on and -off capability by the MOS gate but also has a significantly lower on-resistance than a conventional power MOSFET. This new device is called IGT [2], [3], COMFET [4] or GEMFET [5]. In the present letter, another name, bipolar-mode MOSFET [6], [7] is used, being characterized by the unique source–gate structure and the double-diffused p^+-base, as shown in Fig. 1. It was reported [3] that at the early development stage, the parasitic thyristor was easy to latch-up, preventing a high-current turn-off capability of more than a few hundred amperes per 1 cm^2.

This letter shows, for the first time, that the latch-up current density is significantly influenced by the source–gate pattern, leading to an optimum pattern for a high-current turn-off capability. 600-V bipolar-mode MOSFET's equipped with an optimum pattern exhibited a large current handling capability of more than 100 A (500 A/cm^2) even at 125°C.

II. SOURCE-GATE PATTERN INFLUENCE ON LATCH-UP CURRENT DENSITY

A. Theory

As is shown in Fig. 1, the hole and electron current flows take different paths: electron current flows through the channel whereas hole current flows into the p-base to reach the source electrode. Thus, the hole current possibly flows more uniformly than the electron current. These assumptions could be justified by two-dimensional numerical simulations [8], which showed that, especially in the turn-off transient, the hole current flows completely uniformly because of the dV/dt current forming the depletion layer.

A part of the hole current flows from the drain to under the gate oxide, passes through the p-base beneath the source layer, and forward-biases the source–base junction by the voltage drop in the p-base due to the current flow. This part

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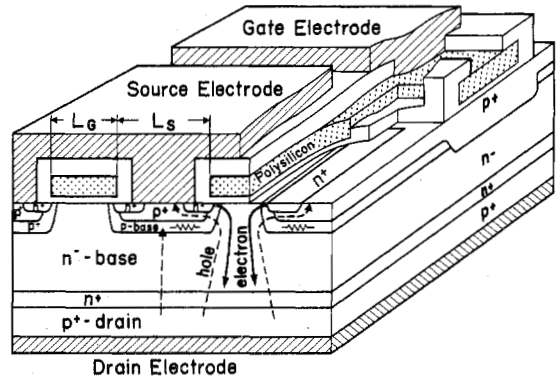

Fig. 1. Cross-sectional view for a bipolar-mode MOSFET.

of the hole current for unit channel width can be estimated for a stripe pattern case on the assumption of uniform hole current flow

$$I_b \cong \frac{L_G}{2} \cdot J_p \tag{1}$$

where J_p is the hole current density beneath the p-base or the gate oxide and L_G is gate polysilicon width, which is defined in Fig. 1. Current I_b causes a voltage drop V_b by passing through the p-base beneath the source layer

$$V_b = R_b \cdot I_b \tag{2}$$

where R_b is the channel to source electrode p-base resistance for unit channel width. If it is assumed that the gate controllability is lost when V_b exceeds a critical value V_{bi} (approximately the built-in voltage of the source–base junction) and electrons begins to be directly injected into the p-base, the maximum controllable current density for the steady-state case is expressed as

$$J_L = \frac{J_p}{\alpha_p} \cong 2V_{bi}/(\alpha_p \cdot L_G \cdot R_b) \tag{3}$$

where α_p is the common-base p-n-p transistor current gain. This simplified treatment were already found to be valid for the latch-up criteria in the light-triggered thyristor through a number of experiments [9].

In the turn-off transient, all of the current is assumed to be carried by holes beneath the p-base and the gate oxide for inductive load cases because the channel is gone and the drain voltage increases to keep the total current. Then, the

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maximum controllable current density for the turn-off transient J_M is given by setting $\alpha_p = 1$

$$J_M \cong 2V_{bi}/(L_G \cdot R_b). \tag{4}$$

Another set of equations can be derived similarly on the assumption that all the current flows only under the gate oxide layer

$$J_L' \cong V_{bi} \cdot W/(\alpha_p \cdot R_b) \tag{5}$$

$$J_M' \cong V_{bi} \cdot W/R_b \tag{6}$$

where W denotes the channel width for unit device area. Although these equations are based on the very simplified assumptions, they are strongly effective for device design.

B. Experiment

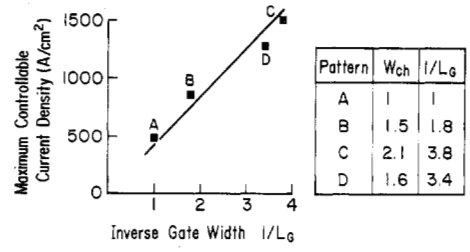
In order to check the validity of the equations, test devices with various stripe source–gate patterns were fabricated. Fig. 2 shows the results on the measured maximum controllable current density versus inverse gate width l/L_G. The inserted table in the figure shows total channel width W_{ch} and inverse gate width l/L_G for each pattern in a relative scale. It is seen that the maximum controllable current density is well proportional to inverse L_G. Thus, it is concluded that (3) and (4) are valid and that the gate width should be as uniform and narrow as possible throughout the device area to prevent localized latch-up. These results also conclude that patterns consisting of many source islands are not good for a large latch-up current density although they are suitable for conventional power MOSFET's, because gate polysilicon width cannot be uniform. It was found that more than 1000-A/cm^2 maximum controllable current density is easily attained by the stripe source pattern without sacrificing forward voltage drop.

III. HIGH-CURRENT BIPOLAR-MODE MOSFET'S

Large-area (6-mm^2 chip) bipolar-mode MOSFET's were fabricated based on the results mentioned in Section II [6]. A stripe source–gate pattern was adopted to realize large current capability. A heavily doped n$^+$-buffer layer was inserted between n$^-$-base and p$^+$-drain, improving the tradeoff between forward voltage and turn-off time as compared with a lightly doped ordinary n-buffer layer (see Fig. 3). For 600-V devices, more than 100-A drain current (500 A/cm^2) could be interrupted even at the elevated temperature of 125°C (see Fig. 4). Obtained electrical characteristics are shown in Table I.

IV. DISCUSSIONS

It was observed that a heavily doped n$^+$-buffer layer improves the tradeoff between the forward voltage and the turn-off time, as shown in Fig. 3. The reason is that the same switching speed can be obtained with a lower electron irradiation dose if a heavily doped n$^+$-buffer layer is used. The lower electron irradiation dose enables a more uniform



Pattern	W_{ch}	l/L_G
A	1	1
B	1.5	1.8
C	2.1	3.8
D	1.6	3.4

Fig. 2. Maximum controllable current density for turn-off transient versus inverse gate width l/L_G. The inserted table shows the channel width per unit device area (1 cm^2), W_{ch}, and inverse gate width l/L_G, for each pattern. All the design parameters except l_s and L_G were kept the same for A, B, C, and D.

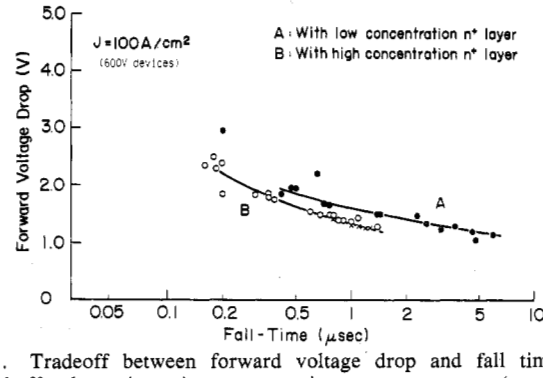


Fig. 3. Tradeoff between forward voltage drop and fall time with n$^+$-buffer layer impurity concentration as a parameter (n$^-$-epilayer conditions were kept the same).

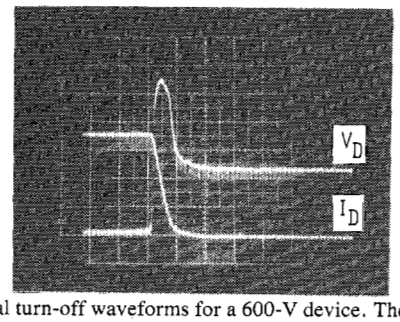


Fig. 4. Typical turn-off waveforms for a 600-V device. The device turned off 105-A drain current at 125°C with a 20 Ω load resistor. I_D: 30 A/Div., V_D: 100 V/Div., Time: 1 μs/Div. (Since no device protection circuits were used, surge voltage over 550 V due to the circuit stray inductance was clamped by the test device itself. A 10-Ω gate resistor was inserted between the gate terminal and the gate circuit.)

TABLE I
ELECTRICAL CHARACTERISTICS (FORWARD VOLTAGE VALUES ARE GIVEN FOR THE MAXIMUM dc CURRENT)

Device	1	2	3	4
Breakdown Voltage	600V			1200V
Forward Voltage	2.5V (at 25A)	1.5V (at 25A)	2.0V (at 25A)	3.0V (at 20A)
Turn-On Time	45ns	50ns	50ns	150ns
Fall-Time	0.8μs	0.8μs	0.3μs	1.5μs
Epi-Layer	50μm	45μm	45μm	90μm
Buffer-Layer	N	N$^+$	N$^+$	N
Maximum Controllable Current at 125°C.	more than 100A	more than 75A	more than 65A	more than 75A

** Device active region 20mm^{-2}

excess carrier distribution in the device, i.e., a resultant lower forward voltage drop. In addition, the electron channel mobility is not excessively reduced by the lower irradiation dosage. The n^+-buffer layer was only adopted for 600-V devices at present because of the difficulty in epitaxial growth.

V. CONCLUSION

600-V 25-A and 1200-V 20-A bipolar-mode MOSFET's with a large current capability have been developed, based on the pattern design theory for a high latch-up current. Adoption of a heavily doped n^+-buffer layer realizes a low forward voltage drop as well as a high switching speed.

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