Breakdown Voltage Enhancement for Devices on Thin Silicon Layer/Silicon Dioxide Film

Akio Nakagawa, *Member, IEEE*, Norio Yasuhara, and Yoshiro Baba

***Abstract*—Studies of high-voltage lateral device structures on a thin silicon layer over silicon dioxide have been carried out. It was found both theoretically and experimentally that over 600-V devices can be realized using a structure consisting of an n diffusion layer over 15-μm-thick high-resistivity n^- silicon layer over 3-μm silicon dioxide (SOI).**

A method is presented to enhance breakdown voltage by applying a large share of the voltage to the bottom oxide.

I. Introduction

DIELECTRIC isolation is a reliable technique for high-voltage power IC's, especially those IC's with a breakdown voltage above 500 V. Several techniques have already been proposed for such dielectric isolation [1], [2]. The key requirements for optimum dielectric isolation are the ability to pack devices at high density and the applicability of the technique to large-diameter wafers. Trenches are a very attractive means of isolation, but the trench depth is limited by the lack of good mask material for selective RIE and by difficulties in filling deep trenches.

This paper reports on 500-V device structures on a thin silicon layer over silicon dioxide substrate (SOI), in which isolation is achieved by a trench technique. It is shown that a combination of trenches and high-voltage devices on SOI has the potential for ideal dielectric isolation, leading to the possibility of future high-voltage high-current power IC's.

One important issue is how to ensure a high breakdown voltage, when a high-voltage device is isolated from a substrate at earth potential only by means of a thin oxide film. The substrate potential has a major influence on the device breakdown voltage through the thin oxide film when the silicon layer is completely depleted. This effect is not observed for high-voltage devices on conventional SOS (silicon on sapphire) layers, because the insulating layer is very thick.

It was shown [3] that ideal breakdown voltage can be achieved in fully depleted SOI diodes without junction curvature effects. In this paper, it is shown [4] that lateral diodes with an n diffusion layer surrounded by a p diffusion layer is a better candidate for high-voltage diodes on SOI layers than the counterpart structure (a p diffusion layer surrounded by an n diffusion layer), which was examined in [3]. A new technique to further enhance breakdown voltage is proposed. It is shown that the oxide interface charge contributes to device breakdown voltage enhancement. This is a result opposite to that presented in [3].

The realistic 500-V high-voltage device structures on SOI substrates are also investigated.

Manuscript received October 14, 1990; revised February 12, 1991.

A. Nakagawa and N. Yasuhara are with the Research and Development Center, Toshiba Corporation, 1, Komukai, Toshiba-cho, Saiwai-ku, Kawasaki 210, Japan.

Y. Baba is with the Microelectronics Center, Toshiba Corporation, 1, Komukai, Toshiba-cho, Saiwai-ku, Kawasaki 210, Japan.

IEEE Log Number 9100062.

II. Device Structure Optimization Using a Breakdown Voltage Simulator TONADDE II B

Fig. 1 shows the device structure studied which has an 8-μm deep n-type diffusion layer with a $2 \times 10^{17}/cm^3$ surface impurity concentration. The diffusion layer is formed on a thin silicon layer over a silicon dioxide substrate.

For simplicity, lateral diode structures were adopted to optimize the device structure. The breakdown voltage was calculated by estimating the ionization integral using the device simulator TONADDE II B [5].

It was found that more than 500-V breakdown voltage can be realized in the simple structure of Fig. 1, and that the potential drop across the 3-μm-thick bottom oxide is approximately 200 V.

If the device structure is optimized so that a larger portion of the applied voltage is shared by the bottom film of silicon dioxide, the breakdown voltage is enhanced. One way to do this is to form a positive charge layer at the interface between the thin silicon layer and the bottom oxide.

A. Shallow n Diffusion Layer on the Bottom Oxide

We propose two device structures, as shown in Fig. 2(a) and (b), where shallow n-type diffusion layers (typically less than 2-μm in diffusion depth) are formed directly on the bottom oxide. The source and drain electrode configurations are opposite in the two different structures. An appropriate impurity dose in the bottom n-type shallow diffusion layer improves the breakdown voltage. The ionized donors effectively shield the high electric field inside the bottom oxide layer as explained later.

0018-9383/91/0700-1650$01.00

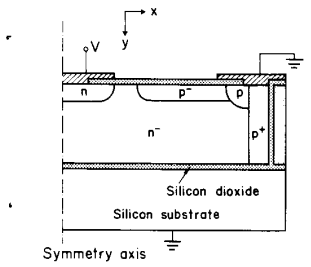

Fig. 1. Studied device structure.

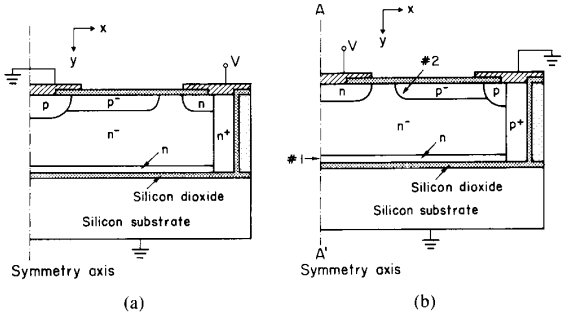

Fig. 2. Two proposed 500-V device structures for thin silicon layer/silicon dioxide/silicon substrate structures.

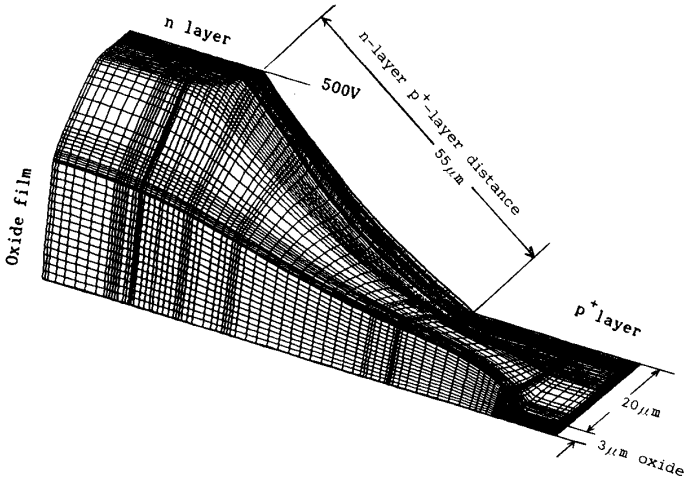

Fig. 3. Calculated potential distribution for the structure in Fig. 2(b).

Fig. 3 shows calculated results for a device with an 8-μm-deep n-type diffusion layer, as shown in Fig. 2(b). The 20-μm silicon layer is completely depleted and half of the applied voltage falls across the silicon dioxide film when a 500-V reverse voltage is applied to the optimized device in Fig. 2(b). The impurity dose in the bottom diffusion layer and the layer depth are both key parameters, in addition to the thicknesses of the bottom oxide film and the silicon layer, which are naturally factors with great influence on the device breakdown voltage.

Fig. 4 shows the electric field distribution along the symmetry axis A–A' of the calculated device for various values of total impurity dose S_D in the bottom shallow n-type diffusion layer. It is seen that the ionized donors in the shallow diffusion layer contribute to a rapid fall in electric field strength inside the silicon layer in the bottom oxide.

Fig. 5 shows the dependence of breakdown voltage on the impurity dose S_D for various thicknesses of silicon dioxide film. The impurity dose of the p^- surface resurf layer was adequately chosen so that avalanche breakdown was always observed at point 1 on the symmetry axis, as marked in Fig. 2(b). The reason for this is that the whole

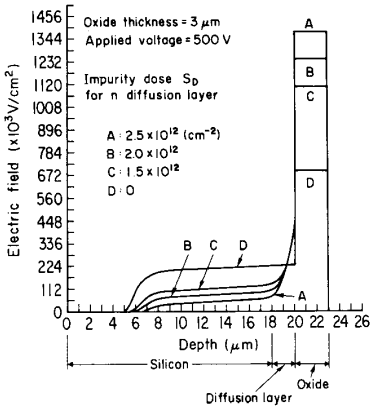

Fig. 4. Electric field distribution along the symmetry axis A–A'. A high electric field is successfully applied in the oxide film.

potential drop has to be supported vertically along A–A'. In other words, the calculated value is the ideal breakdown voltage supported by the remaining thickness of high-resistivity silicon layer beneath the n diffusion layer and by the bottom oxide film.

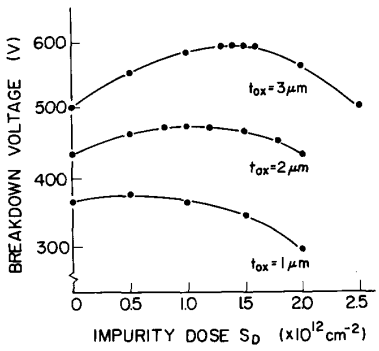

Fig. 5. Breakdown voltage versus impurity dose for shallow n-type diffusion layer characteristics in the structure of Fig. 2(b).

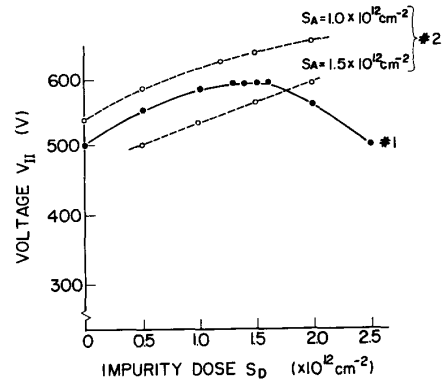

Fig. 6. Voltage V_{II}, which is defined as a voltage where an ionization integral equals unity, is plotted as a function of impurity dose S_D for a shallow n-type diffusion layer on 3-μm silicon dioxide film. The broken lines show V_{II} values determined by the ionization integral passing through point 2. S_A denotes impurity dose for the p^- resurf layer.

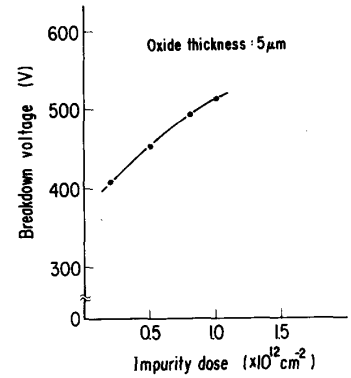

Fig. 7. Breakdown voltage versus impurity dose for shallow n-type diffusion layer characteristics in the structure of Fig. 2(a).

Generally, two high electric field peaks were seen around the points marked 1 and 2 in Fig. 2(b). The electric field peak at point 2 was caused by junction curvature effect. In the actual calculations, breakdown voltages were determined by evaluating all the ionization integrals, whose paths went through high electric field points including 1 and 2. For simple explanation, for each field peak point, the voltage V_{II} is defined as the applied voltage value where the ionization integral, passing through each field peak point, equals unity. The breakdown voltage is defined as the lowest V_{II} value.

In Fig. 6, V_{II} values are plotted as a function of the impurity dose S_D. The two broken lines show the V_{II} values, determined by the ionization integral passing through point 2, when the two different impurity doses S_A for the lightly doped p^- layer are assumed. It is easily seen that V_{II} values for point 2 are always greater than those for 1 (denoted by the solid line), if S_A value is set at 1×10^{12} cm^{-2}. Generally, an adequate impurity dose S_A was always available so that the device breakdown voltage was determined by the ionization integral, which passed through point 1.

It should be noted that even if there is a very high electric field peak, this does not cause avalanche breakdown, as long as the ionization integral is less than unity.

As the impurity dose S_D increased, the electric field inside the oxide increased, as seen in Fig. 4. Since the high electric field inside the oxide does not contribute to the ionization integral, the breakdown voltage can be increased by introducing a shallow diffusion layer on the bottom oxide. However, the n-type shallow diffusion layer was not thin enough to completely shield the high electric field inside the oxide film. Although the electric field rapidly fell in the shallow diffusion layer, an excessively large impurity dose S_D caused a sharp increase of electric field near the silicon and the bottom oxide interface. This finally caused the ionization integral to exceed unity, thus decreasing the breakdown voltage, as shown by the solid line in Fig. 6. The n-type shallow diffusion layer should be as thin as possible.

From Fig. 5, it was shown that a breakdown voltage of 580 V was obtained for a device with an 8-μm n^+ diffusion layer over a 12-μm remaining silicon layer over the 3-μm silicon dioxide film structure and a 2-μm shallow n-type bottom diffusion layer.

Fig. 7 shows similar results for the structure of Fig. 2(a). With this structure, a thicker silicon dioxide film of 5-μm was needed to obtain a breakdown voltage greater than 500 V. This was because all of the applied voltage had to be sustained by the bottom oxide alone if it was near the trench sidewall. A high electric field inside the oxide induced a high electric field inside the silicon near the interface and limited the breakdown voltage. The phenomena will be understood from Fig. 8, where equipotential lines are plotted.

The advantage of the structure of Fig. 2(b) over the structure of Fig. 2(a) can be understood by considering the effective junction boundary. In the structure of Fig. 2(b), the maximum electric field along A–A' inside the silicon is seen just on the bottom oxide. Although there is no actual p-n junction along A–A', the interface of the bottom oxide and the p^+ substrate is regarded as an effective junction for this device structure and constitutes a plane junction.

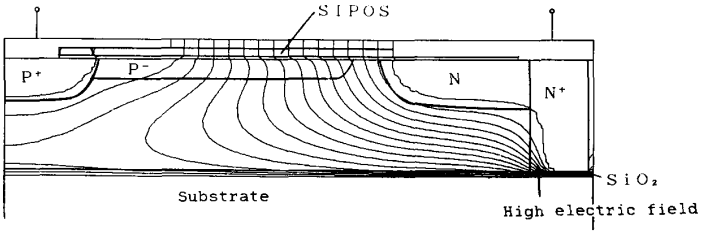

Fig. 8. Process flowchart for deep trench isolation.

The n-type shallow diffusion layer does not completely shield the high electric field inside the oxide film if the layer is not thin enough. Thus if a better means of forming a positive charge layer at the very interface between the silicon layer and the bottom oxide can be found, the device breakdown voltage will be further improved.

B. Effects of Interface Charge

It is well known that a positive charge exists at the silicon/oxide interface. The charge density is typically $5 \times 10^{10}/\text{cm}^2$ according to conventional silicon processes. This interface charge effectively increases the electric field strength inside the oxide film without affecting the field strength in the bulk silicon, thus simply enhancing the device breakdown voltage. For example, approximately 14-V enhancement in breakdown voltage is predicted, using (1), for a $1 \times 10^{11}/\text{cm}^2$ interface charge density if the bottom silicon dioxide film is 3 μm thick. This enhancement, δV, can be estimated by assuming that the total interface charge contributes to an increase in electric field inside the oxide.

$$\delta V = qQ_s W_{ox}/\epsilon \qquad (1)$$

where Q_s, W_{ox}, and ϵ are charge density, oxide thickness, and permittivity of the oxide. However, in actual devices, a part of the interface charge is consumed for the lateral electric field, and thus a 7-V breakdown voltage enhancement was obtained for the devices with $1 \times 10^{11}/\text{cm}^2$ interface charge density.

The interface charge increases breakdown voltage even for the structure of Fig. 2(a) when the p-diffusion layer and the substrate are both grounded and a positive bias is applied to the n-diffusion layer.

III. Experimental

Wafer direct-bonding [6] and deep trench techniques are a good combination for a high-voltage, high-density power IC structure. A relatively thick silicon layer is necessary to achieve a low on-resistance in high-voltage devices, and a 20-μm-deep trench technique has been developed for this purpose. The process flow chart for 5-in-diameter wafer fabrication is illustrated in Fig. 9. Initially, 20-μm-deep trenches are formed, using a deposited SiO_2 film more than 2 μm thick as a selective etching mask. After p^+ dopant deposition on the trench sidewalls, thermal oxidation and polysilicon filling are consecutively

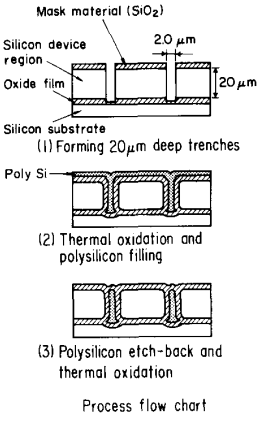

Fig. 9. Electric potential distribution for the device structure of Fig. 2(a), when 150 V is applied to the n^+ layer. A high electric field is seen at the portion indicated by the arrow.

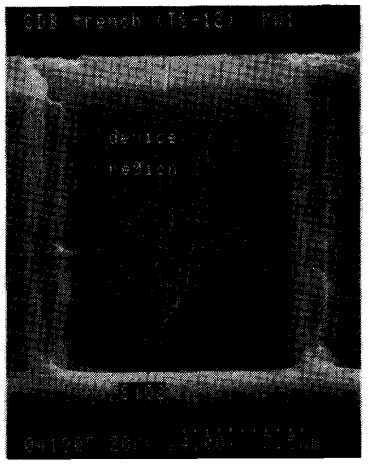

Fig. 10. 20-μm-deep trench-isolated silicon island.

carried out. The final smooth surface finish is attained by polysilicon etch-back using the RIE technique and thermal oxidation. Fig. 10 is a photograph of the resulting trench-isolated silicon island.

Lateral diodes with 5-μm-deep n-type diffusion layers with 1×10^{19} cm^3 surface impurity concentration were fabricated on the trench-isolated silicon on insulating substrates to check the effects of crystal defects associated with trench RIE on the breakdown voltage. An n-type

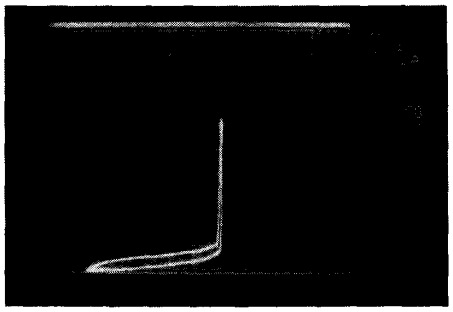

Fig. 11. Measured V-I characteristics for a device of Fig. 2(b).

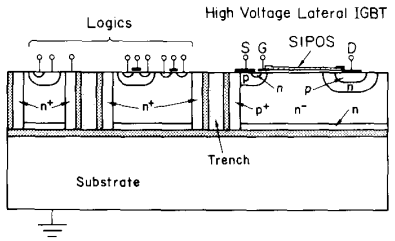

Fig. 12. Deep-trench-isolated power IC.

shallow diffusion layer on the bottom oxide was not adopted in this experiment. 580- to 620-V breakdown voltage was observed for the simple lateral diode structure of Fig. 1 with a 3-μm bottom oxide, as shown in Fig. 11. The leakage current was sufficiently small (less than 50 μA) and the measured breakdown voltage exceeded the calculated value of 550 V for the same structure, assuming a $5 \times 10^{10}/\text{cm}^2$ interface charge.

It should be noted that in Fig. 5, the calculated structure with $S_D = 0$ is the same as that for Fig. 1 and, consequently, the experimentally fabricated device structure. The only difference is the n-layer diffusion depth. The n-layer diffusion depth for the device analyzed in Fig. 5 is 8 μm, whereas that for the experimentally fabricated structure is 5 μm. Thus the theoretical breakdown voltage value for the fabricated structure is 550 V, and the calculated breakdown voltage for the corresponding structure in Fig. 5 is 500 V. The reason is that the fabricated structure has a thicker n-type high-resistivity layer.

The experimentally observed breakdown voltage is still larger than the calculated value of 550 V. Although the reason for the discrepancy between theory and experiment is not clear at present, one assumption is that the actual ionization coefficient is smaller than the used value [7].

The observed results verify that trench isolation causes no problem in high-voltage power IC's.

The proposed structure can be applied to various high-voltage lateral devices, including lateral IGBT's [8], and it makes dielectrically isolated power IC's a more promising prospect.

One conceptual future power IC structure is the one shown in Fig. 12, where the new high-voltage technique is applied to lateral IGBT's. CMOS logic circuits will be formed on a single silicon island and each bipolar logic area and high-voltage device will be isolated by trenches. The problem is that both p^+- and n^+-type trench sidewall diffusions have to be carried out into the same trench. This can be avoided, for example, by using two trenches. Another option is to adopt the device structure of Fig. 2(a) with a thicker bottom oxide film.

IV. Conclusion

Deep trench isolation combined with silicon wafer direct-bonding is a promising technique for future high-density high-voltage dielectrically isolated power IC's, which use more than a 5-in diameter and larger wafers. It was shown that a breakdown voltage exceeding 500 V can be obtained by a thin silicon layer on a silicon dioxide structure. It was further shown that a thin positive charge layer directly on the silicon dioxide film contributes to device breakdown voltage enhancement.

References

[1] J. D. Beasom, "A process for simultaneous fabrication of vertical NPN and PNP's, Nch and Pch MOS devices," in *1973 IEEE IEDM Tech. Dig.*, pp. 41-43.

[2] H. Ohashi, J. Ohura, T. Tsukakoshi, and M. Shimbo, "Improved dielectrically isolated device integration by silicon-wafer direct-bonding (SDB) technique," in *1986 IEEE IEDM Tech. Dig.*, p. 210.

[3] H. C. Chen, S. S. Li, R. M. Fox, and W. A. Krull, "Increased junction breakdown voltages in silicon-on-insulator diodes," *IEEE Trans. Electron Devices*, vol. 36, pp. 488-492, 1989.

[4] A. Nakagawa, Japanese Patent Application 62-43564, Feb. 26, 1987.

[5] I. Omura and A. Nakagawa, "A breakdown voltage simulator for semiconductor devices with depleted floating regions," in *Proc. 6th NASECODE*, 1989, pp. 372-377.

[6] M. Shimbo, K. Furukawa, K. Fukuda, and K. Tanzawa, "Silicon-to-silicon direct bonding method," *J. Appl. Phys.*, vol. 60, pp. 2987-2989, 1986.

[7] R. Van Overstraten and H. De Man, "Measurement of the ionization rates in diffused silicon p-n junctions," *Solid-State Electron.*, vol. 12, pp. 583-608, 1970.

[8] A. Nakagawa, Y. Yamaguchi, K. Watanabe, and T. Ogura, "Two types of 500 V double gate lateral N-ch bipolar-mode MOSFETs in dielectrically isolated P^- and N^- silicon islands," in *1988 IEEE IEDM Tech. Dig.*, pp. 817-820.