Single Chip Power Integration
----- High Voltage SOI and Low Voltage BCD -----

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Abstract:

Single chip power integration is attractive and effective in the various fields. For high voltage system integration, the key technology is dielectric isolation (high voltage SOI), which realizes a whole system in a single chip. A typical example is one chip inverter ICs, directly utilizing the ordinary AC line source. In the low voltage systems, such as mobile equipments, computer peripherals and automotive, BCD technology, integrating lateral DMOS with BiCMOS, is well suited for large-scale power system integration. The essential technology is robust and low on-resistance lateral DMOS design based on CMOS process.

The present paper focuses the SOI technology and the robust lateral DMOS design for single chip power integration

1. Introduction

Power system integration is paid attention especially in the two fields. One is high voltage power system, whose voltage range is 200 to 600V. High voltage DC systems tend to be used to improve energy efficiency. Home appliances have adopted DC motors, which are driven directly by the AC line source. EV and HEV adopted 150V or 300V DC voltage. 500V single chip inverter ICs [1] are typical examples for the high voltage power integration.

The other is low voltage power ICs for mobile equipment and computer peripherals. BCD technology [2], integrating power DMOS with BiCMOS devices, is evolving rapidly by taking advantage of the leading edge LSI technology. Robust and low on-resistance lateral DMOS design is essential for low voltage system integration.

The present paper deals with the key technologies for the high and low voltage power system integration.

2. High voltage power system integration

Power system integration in the high voltage range is getting important to improve system performance. For example, technologies for color plasma display panels have greatly advanced, and demands for PDP driver ICs [3] is increasing. Another application is motor control. Home appliances use a number of small motors, which can be directly controlled by the AC line source. Single chip inverter ICs are able to reduce system sizes and increase system performance.

Inverter-controlled medium scale DC motors are now widely applied to home appliances, such as washing machines, vacuum cleaners and air conditioners. For these applications, 15 or 20A rated IGBTs are required, and multi-chip modules are adopted. TM-IPM (transfer mould IPM) has been developed for this purpose.

In the automotive field, EV and HEV now adopt a high voltage battery of 150V or 300V [4]. 42V DC voltage system [5] will be introduced in conventional emission vehicles to improve energy efficiency.

Dielectric isolation is suitable for high voltage power ICs. Conventional DI method called EPIC has problems of high cost, large wafer warpage and difficulty in fabricating 6-inch wafers. The invention of wafer direct-bonding method [6], in 1985, made it possible to fabricate SOI wafers with thick buried oxide, and opened the application of SOI wafers to high voltage power ICs.

2.1 High voltage SOI technology [7]

High voltage lateral devices can be realized in SOI by utilizing a thick buried oxide as a voltage supporting material. Trench isolation enables high-density device integration of low voltage logic and control circuits together with high voltage devices.

Recently, 500V 3A three-phase one chip inverter ICs [8] have been developed for compressor motor control of refrigerators. The current rating of 5A for 500V power ICs is now assumed to be a critical upper limit for single chip integration.

IGBTs are suitable for high voltage output devices because of a large current capability for over 200V as seen in Fig.1. The output devices should be fabricated by conventional CMOS compatible process so that conventional circuit libraries can be utilized without changes.

The switching speed of power devices is conventionally controlled by introduction of a lifetime killer. However, lifetime control process is not compatible with conventional CMOS process. There are several means to control switching speed of power devices. One way is to use thin SOI layers. The switching speed of IGBTs improves as the SOI thickness decreases because carrier lifetime is effectively decreased by a large carrier recombination at the silicon dioxide interfaces. Another way is to reduce emitter efficiency of the p^+ drain or collector. The effective methods are (1) low dose emitter, (2) high dose n buffer or (3) forming an n+ layer in the p+ emitter [9].

Figure 2 shows a cross section of large current lateral IGBTs. Large current capability has been realized by adopting multiple surface channels.

2.2 SOI Device Breakdown Voltage

SOI power ICs are classified into two categories from the view point of SOI wafer structure. The difference is whether there is a buried n^+ layer on the buried oxide. The maximum breakdown voltage is limited to below 150V if n^+ buried layer exists because SOI layer thickness is limited to practically available trench depth.

If there is no buried layer, SOI layer is fully depleted by application of a high voltage. A high breakdown voltage is realized in relatively thin SOI since the thick buried oxide and the depletion layer both share the applied voltage.

It is widely recognized that SOI device breakdown voltage is determined by the so-called SOI-Resurf principle [10]. For optimized SOI diodes, the breakdown voltage is limited to that of the 1-D MOS diode portion as illustrated in Fig.3, consisting of n^+/n^-/oxide /substrate. Figure 4 shows measured SOI device breakdown voltage as a function of SOI layer thickness with buried oxide thickness as a parameter [11]. The calculated breakdown voltages of 1-D MOS diodes are shown together. A 500V breakdown voltage can be obtained with a 13μm thick SOI with 3μm thick buried oxide.

It is very difficult to achieve a high breakdown voltage exceeding 600V in SOI because a thicker buried oxide layer of 4μm or more is required in the conventional SOI structure.

In 1991, the author proposed a new high voltage SOI device structure, which is free from the above constraints [12]. The proposed new SOI diode is characterized by a SIPOS (Semi-insulating Poly-crystalline Silicon) layer, which is inserted between the silicon layer and the buried oxide. The SIPOS layer effectively shields the influence of the substrate bias, and a 1200V breakdown voltage can be realized by only 2.0μm thick buried oxide with 1.0μm thick SIPOS layer.

2.3 500V 3A 3-phase inverter ICs and further challenges for larger current capacity power ICs

This section reports recent development of 500V 3A three-phase inverter ICs and shows the possibility of further increasing current capacity of high voltage power ICs.

As the cost of the power IC chip is the first priority for consumer application, great efforts have been made to reduce the chip size of the developed IC chip.

The lateral IGBT on-resistance has been improved by adopting (1) finer multi-channel design [13], (2) reduced JFET effects by phosphorous implant under the poly-silicon gate and (3) thicker aluminum interconnection layers.

Figure 2 shows the cross section of the improved multi-channel LIGBTs, which have been developed for 500V 3A single chip three-phase inverter ICs. Shallow n-type implant layers are formed under the poly-silicon gate to reduce JFET resistance by using the same channel implant as that used for PMOS threshold voltage control.

The p-well size is reduced from 8mm down to 5mm by adopting 0.5μm fine alignment tolerance. The drain (collector) p^+ emitter size was also reduced to 16μm. The unit LIGBT cell size was reduced to 140μm, which is 87% of the conventional multi-channel LIGBTs [13].

A large current capability of 175A/cm^2 current density was realized in the new LIGBTs for 3.0V forward voltage and 300nsec fall-time, which is 35% improvement, compared with that of conventional multi-channel LIGBTs

Short-circuit withstanding capability of the developed LIGBTs was successfully achieved. The new LIGBT withstands load short-circuit current of 8A for 8μsec at room temperature.

Figure 5 shows a developed 500V 3A single chip inverter IC [8] for compressor motors of refrigerators. The motors were driven by electrically detecting the rotor position without using hall sensors.

Further improvement in forward voltage of lateral IGBTs is possible by adopting further finer lithography. Figure 6 shows the predicted LIGBT V-I

characteristics if the 0.6μm design rule is applied. 17% reduction in forward voltage will be possible.

2.4 High Temperature Operation of SOI power ICs.

The leakage current of SOI devices simply reduces as the SOI layer becomes thinner [14]. Small leakage current enables high temperature operation of SOI power ICs. It was experimentally shown that IGBTs can be operated at a switching frequency of 20kHz at 200 °C, if they are fabricated in thin SOI of less than 5μm [15]. Maximum operating temperature of analog circuits in SOI increases as the SOI layer becomes thinner.

We demonstrated 200 °C operation of 250V 0.5A three-phase 1 chip inverter ICs fabricated in 5μm thick SOI layer [16]. CMOS circuits on SOI were found to be capable of operating at 300 °C. We used CMOS based analog circuits with a minimum number of bipolar transistors. It was found that the bandgap reference circuit operated at 250 °C. We confirmed that the single chip inverter IC operated a DC brushless motor at 200 °C. The carrier frequency was 20kHz.

2.5 Possibility for large system integration

For less than 100V applications, the required thickness of buried oxide layer is less than 1μm. The warpage of the SOI wafers is very small, thus fine lithography can be applied. SOI is well suited for integration of an MPU together with BiCMOS analog circuits and lateral DMOS.

In 1995, we experimentally demonstrated that 4 bit MPUs, vertical npn, pnp and 60V power DMOS were able to be integrated in 2μm thick SOI wafers [17]. 60V DMOS was fabricated, using CMOS p-well without using diffusion self-alignment process. Completely the same masks and fabrication process as those used for 4 bit MPUs on bulk wafer were used. Thus, the same 4 bit MPUs were simultaneously fabricated both on SOI and bulk wafers.

One of the characteristic features of the proposed SOI power IC structure, shown in Fig.7, is that there are no buried layers for bipolar transistors. It was found that vertical npn and pnp transistors fabricated on the n-well and p-well layers exhibited sufficiently good characteristics. The current gains h_{FE} obtained for the vertical npn and pnp transistors were 80 and 30, respectively.

A prospective application of the technology is the automotive field, which requires large current DMOS outputs. Conventional pn junction isolated power ICs are frequently used for these applications, however, the reliability of junction isolation is not sufficient. SOI DMOS power ICs will be used where high reliability is required.

3 Low voltage power system integration -- BCD technology

Lateral DMOS was invented by Tarui in 1974 [18]. In the 70's, the main application field of lateral DMOS was plasma display driver. DMOS concept evolved into vertical DMOS and opened vast application field in discrete power devices.

In the 80's, the on-resistance of vertical DMOSFET was reduced year by year with the advance in fine lithography in LSI technology. As the technology of micro-lithography further advanced, the on-resistance of lateral DMOS became lower than that of bipolar transistors.

With the introduction of a 0.6μm design rule, lateral DMOS has become predominant over the wide voltage range from 20V up to 150V. Mixed technology, called BCD, integrating BiCMOS and DMOS, is now widely accepted for the low voltage power ICs.

Many studies have been performed on the development of low on-resistance 20V to 60V DMOS for a variety of applications such as automotive systems and computer peripherals. Especially, battery operated mobile equipment and computer peripherals have opened a large application field of low voltage power ICs.

3.1 Advantage of lateral power MOSFET

For above 60V breakdown voltage range, the vertical DMOS structure with upside surface drain contact has conventionally been used. However, recently, the lateral DMOS structure has been paid attention for the entire voltage range. This is because LDMOS on-resistance can be simply improved by adopting finer lithography.

Figure 8 shows how the LDMOS on-resistance depends on the design rule. It is seen that the on-resistance of 60V LDMOS reduces, depending on the design rule. This motivated us to push the technology of lateral DMOS instead of up-drain vertical DMOS. It is possible that power ICs with LDMOS outputs will cover a large current capacity up to 10A.

3.2 Lateral DMOS based on BiCMOS compatible process

Figure 9 and 10 shows cross-sectional views of developed 60V and 25V lateral DMOS on n-epi wafer with n^+ buried layers [19,20]. The fabrication process

is completely compatible with 5V BiCMOS process. The channel region is not formed by the conventional DSA (diffusion self-align) process but by the same process as that for the CMOS channel.

The 60V DMOS is characterized by the n^+ sinker, which electrically connects the drain and the buried layer. The p-well diffusion layer is depleted both by the n-drift and the n-epi layers. The structure is effective to increase the breakdown voltage and to reduce the on-resistance of the lateral DMOS.

The 60V DMOS design was optimized together with 30V bipolar transistors

3.3 Rugged LDMOS Design for large safe operating area and ESD

Conventional RESURF LDMOS has a drawback that the breakdown voltage degrades as the drain current increases, and that the I-V curve shows snapback characteristics. Adaptive RESRF concept [20] was proposed to achieve a high on-state breakdown voltage under a large drain current flow condition.

Figure 12 shows calculated I-V curves of conventional 30V LDMOS with on-resistance of 15.7 milliohm mm^2. The device breakdown voltage for 5V gate voltage is only 13.9 V. The reason why the on-state breakdown voltage degrades is that, in the RESURF layer, the net effective positive charge is reduced by the existence of a large amount of negative electron charges due to a large drain current. Thus, the net positive charge in the depleted Resurf layer deviates far from the optimized value. The net positive Resurf charge under the drain current of I_D is expressed by $P_{Resurf\ dose}$ - I_D/qv_s, where $P_{Resurf\ dose}$ denotes the original Resurf dose, v_s the electron saturation velocity.

Figure 11 shows the new LDMOS, adopting 2 step Resurf layers (adaptive Resurf layers). The impurity dose of the added second Resurf layer is chosen to be the value of $P_{Resurf\ dose} + I_D/qv_s$, which is typically 2 or 3 times greater than the optimum value of the conventional Resurf layers. The adaptive Resurf provides the optimum positive Resurf charge under the existence of a large drain current flow.

Figure13 shows the calculated I-V curves for the new LDMOS adopting the optimized 2 step adaptive Resurf layers. The breakdown voltage of about 20V is still retained at the on state of 5V gate voltage.

The same design concept can be applied to non-RESURF n-drift LDMOS. Complementary 25V LDMOS for analog applications was developed, using 0.6 μm BiCMOS process. The device structure is shown in Fig. 10.

Typical I-V characteristics of the fabricated n-channel and p-channel LDMOS are shown in Fig.14 and 15, respectively. n-ch and p-ch LDMOS achieved high on-state breakdown voltages, 33 V for n-channel and 50V for p-channel at the gate voltage of 5.0V. The values of specific on-resistance are 27.5 milliohm mm^2 for n-channel and 111 milliohm mm^2 for p-channel LDMOS, respectively.

n-channel LDMOS withstands load short-circuit condition for 1msec at 150°C under the drain voltage of 14V. The maximum controllable current capability is 17.1A/mm^2 under an unclamped inductive load (500μH) at room temperature.

60V LDMOS was also developed based on the 2 step Resurf concept and 0.8um design rule. The 60V LDMOS has on-state breakdown voltage of 45V, and the static breakdown voltage is 70V. The device has been adopted as output devices in 40V rated commercially available BCD power ICs.

The developed 60V and 25V LDMOS exhibit high ESD endurance capabilities both for machine and human body models.

3.4 Further improvements in future MOSFETs.

In 1999, we proposed 20V lateral trench gate MOSFETs, shown in Figs.16 & 17, which have successfully achieved a record low specific on-resistance 13 milliohm mm^2 [21].

Conventionally, trench gate structures have been used for vertical trench MOSFETs, where channel current flows vertically on the trench sidewalls. The unique feature of the lateral trench gate MOSFETs is that the electrons spread from the source layer into the channel regions, induced both on the trench terraces and on the trench sidewalls, and that the electrons flow laterally on the trench sidewalls from the source to the drain.

The lateral trench MOSFETs were fabricated, using the standard 0.6μm CMOS process with an additional trench gate formation process. The fabricated device achieved 13 milliohm mm^2 of on-resistance with the breakdown voltage of 25V, which is the lowest on-resistance ever reported.

The lateral trench gate MOSFET is can be improved by introducing a trench contact for the drain electrode. A very low on-resistance of 7.8 milliohm mm^2 with a 25V breakdown voltage is predicted by device simulations for the new device structure.

The author assumes that a deep sub-micron design will further reduce specific on-resistance of low voltage power MOSFETs of less than 10V. A DC/DC converter is now integrated in system LSIs, and CMOS itself is used as power output devices. Power CMOS will be used as very low voltage power MOSFETs.

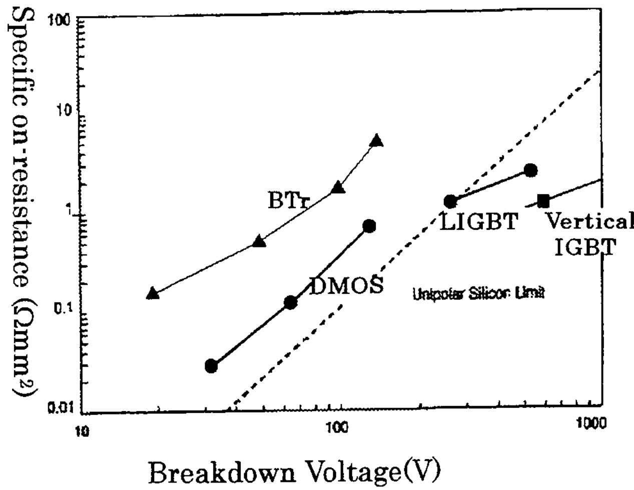


Fig.1 Specific on-resistance of typical power devices as a function of breakdown voltage.

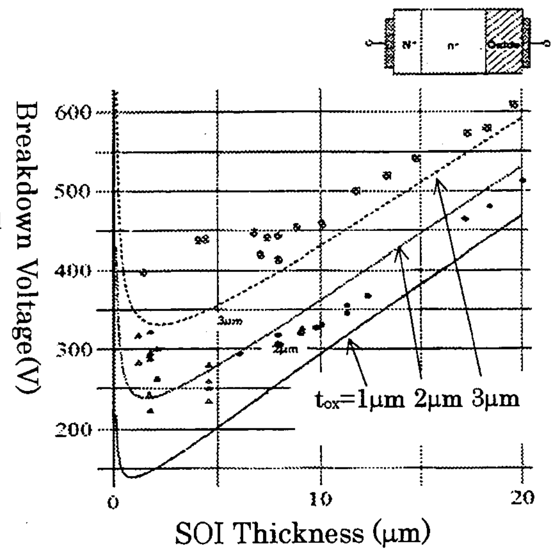


Fig.4 Theoretical (solid and broken lines) and experimental (dots) breakdown voltage vs. SOI layer thickness with buried oxide thickness as a parameter.

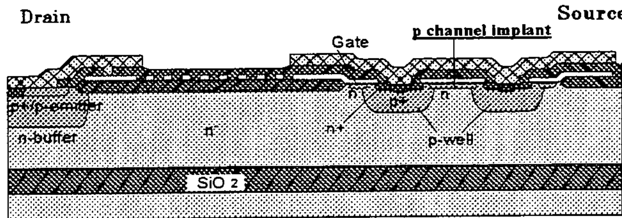


Fig.2 Cross section of 500V 3A lateral IGBT.

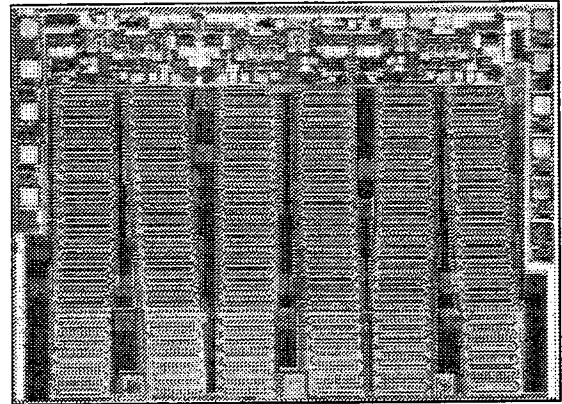


Fig.5 500V 3A inverter IC chip.

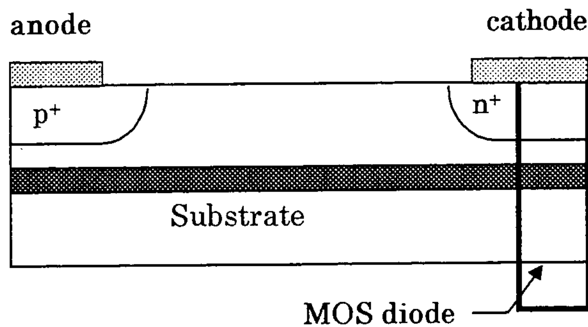


Fig.3 SOI diode structure, showing that 1-d MOS diode portion substantially determines SOI diode breakdown voltage.

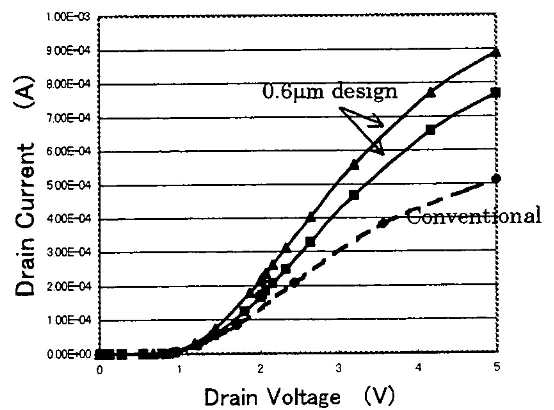


Fig.6 Improvement in LIGBT characteristics by finer design.

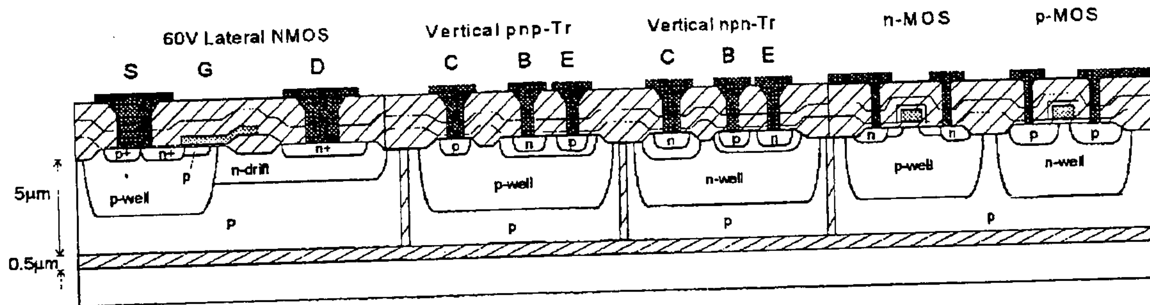


Fig.7 Cross-sectional view of developed 60V BCD power ICs in 2μm thick SOI.

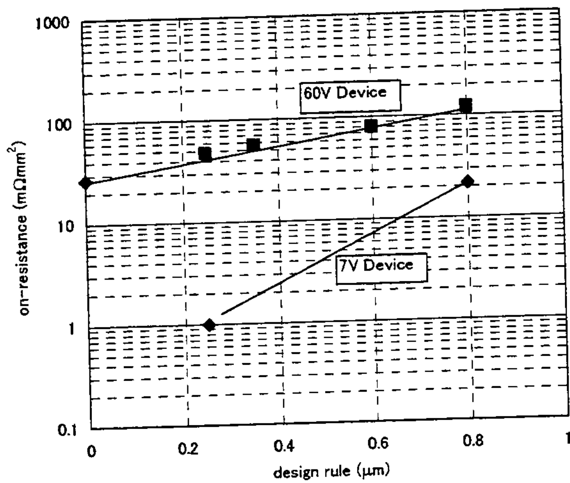


Fig.8 Predicted dependence of on-resistance on design rule.

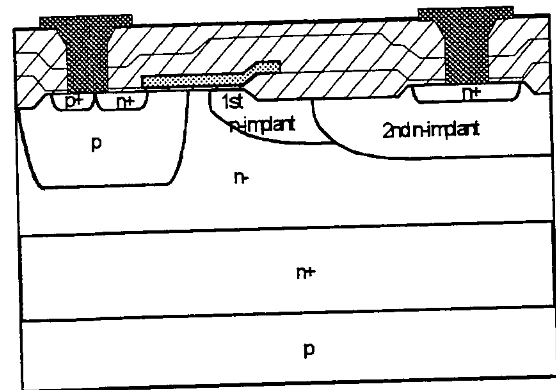


Fig.10 Cross-sectional view of a 2-step n-implant structure LDMOS. 2nd n-implant layer improves on-state breakdown voltage.

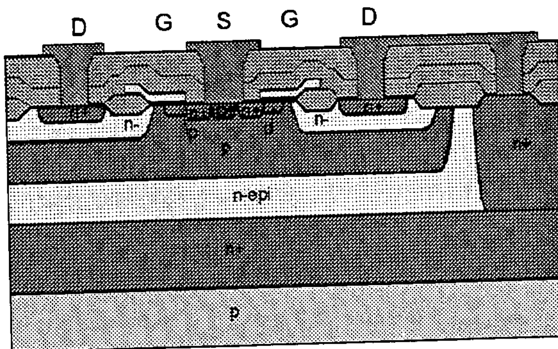


Fig.9 Cross-sectional view of 60V LDMOS.

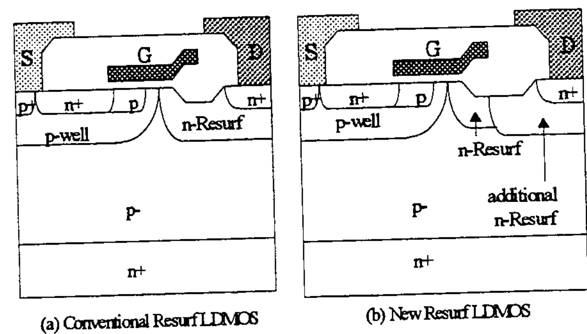


Fig.11 Cross-sectional view of (a) conventional Resurf LDMOS and (b) new Resurf LDMOS.

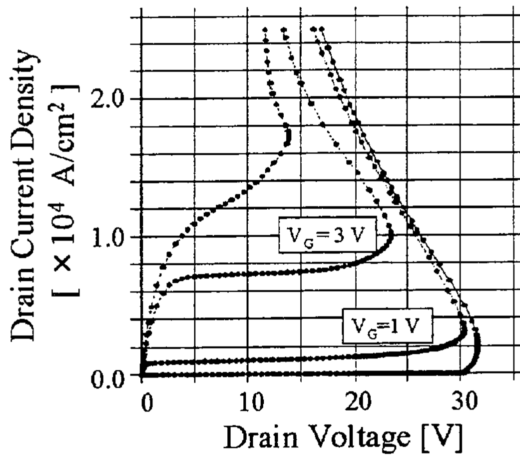


Fig.12 Typical I-V curves of conventional LDMOS, showing snapback characteristics.

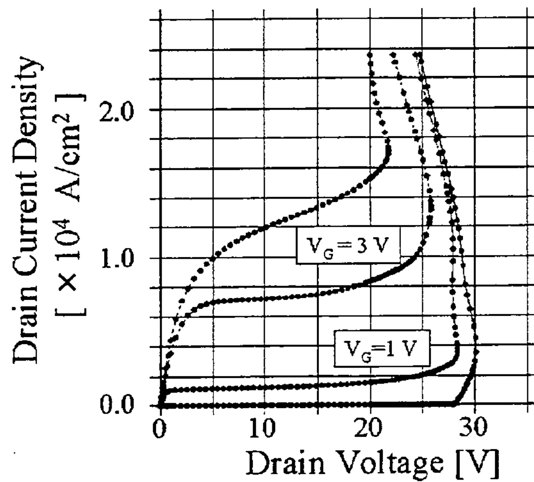


Fig.13 I-V curves of New LDMOS with 2 step Resurf layers.

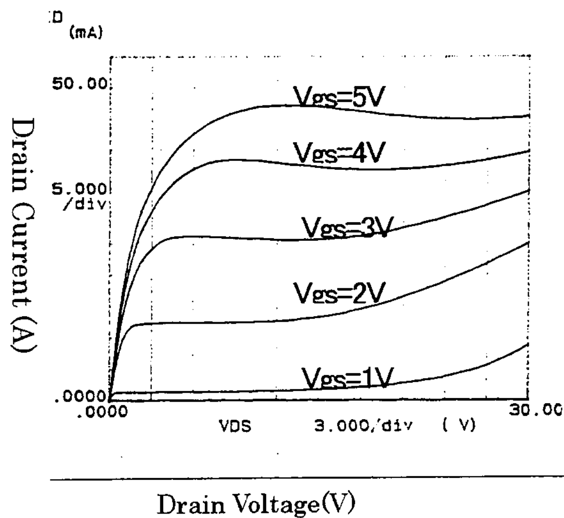


Fig.14 The measured I-V characteristics of N-ch LDMOS

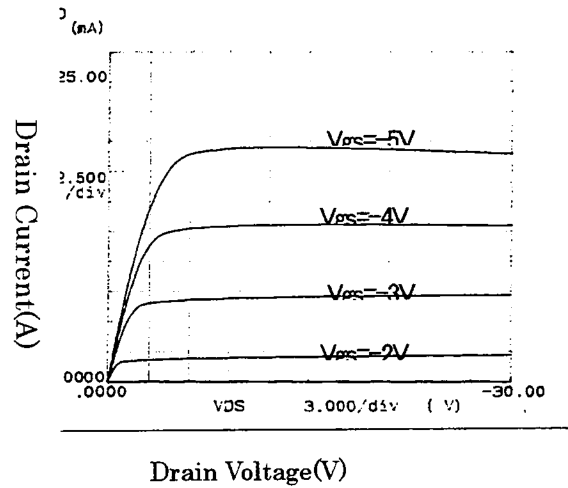
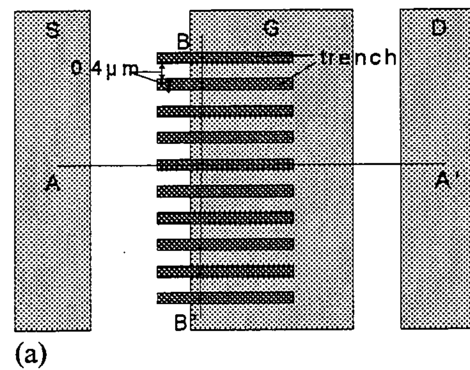
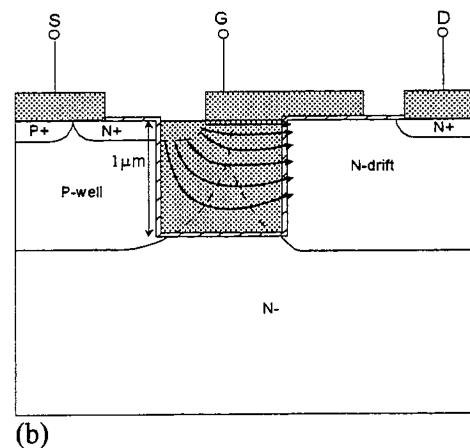


Fig.15 The measured I-V characteristics of P-ch LDMOS



(a)



(b)

Fig.16 Top view (a) and Cross sectional view (b) of lateral trench MOSFET.

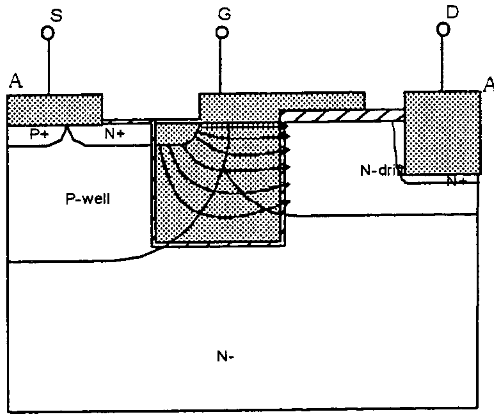


Fig.17 Improved lateral trench MOSFET with drain trench contact.

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