High-Frequency 6000-V Double-Gate GTO's

Tsuneo Ogura, *Member, IEEE,* Akio Nakagawa, *Member, IEEE,* Masaki Atsuta, Yoshio Kamei, and Katsuhiko Takigami

Abstract—**A double-gate GTO, which has an additional gate on the n-base layer, has been proposed to realize high-frequency operation for high-power inverters. The double-gate structure has further been combined with an n-buffer structure to realize narrow n-base width. A forward-blocking voltage of 6000 V was obtained, even at 150°C, when the second gate was shorted to the anode electrode. In order to reduce turn-on and turn-off switching losses, the dependence of these losses on a time interval between two gate triggering pulses has been investigated. It was found that the turn-off loss of approximately 1/20th of that for a conventional GTO was achieved by adjusting the time interval between the two gate triggering pulses.**

I. Introduction

HIGH-POWER gate turn-off thyristors (GTO's) have received much attention as key switching devices for high-power inverters. To broaden the application coverage of GTO PWM (Pulse-Width Modulation) inverters, it is necessary to develop higher frequency GTO's, operating at above 3 kHz. The main problems in realizing this requirement for the high-power GTO's are a significant increases in on-state voltage and switching power loss caused by an increase in n-base width to sustain high blocking voltage. In order to attain high blocking voltage simultaneously with low switching power loss, various device structures have already been proposed [1]–[5]. Furthermore, high-power GTO's with a combination of an n-buffer and an anode-shorted structure have already been proposed [6], [7]. This structure is most suitable for high-frequency operation among those proposed structures. However, the maximum operational frequency, even with this GTO, was still limited to less than 1 kHz, because of its large turn-off switching loss.

In this paper, a double-gate GTO is proposed to attain high blocking voltage, simultaneously with low turn-off switching loss. The device was fabricated on a 33-mm-diameter silicon wafer, using a conventional diffusion process. A 6000-V forward-blocking voltage characteristic at high junction temperature is presented experimentally. A turn-off gate triggering timing for the double-gate GTO is discussed to realize higher frequency operation. An experimental result, comparing the turn-off loss for the double-gate GTO with that for the conventional GTO, is given. A turn-on triggering characteristics for a double-gate triggering case is compared with that for a single-gate triggering case. Total power loss is calculated as a function of operational frequency, to clarify an advantage of the double-gate GTO.

Manuscript received October 1, 1990; revised April 12, 1992. The review of this paper was arranged by Associate Editor T. P. Chow.

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IEEE Log Number 9206107.

II. Experimental Results

A. Forward-Blocking Characteristics

Generally, GTO's are categorized into three main groups: reverse-blocking, anode-shorted, and n-buffer structures. The n-buffer structure is the most suitable to achieve high-frequency operation in high blocking voltage GTO's, because the n-base width for the n-buffer structure is the narrowest among these three structures [6]. Therefore, the double-gate structure has been combined with the n-buffer, as indicated in Fig. 1. A p-n-p-n structure, combined with the n-buffer structure, has the first gate on the p-base layer, fabricated by the same mesa process as that for the conventional GTO's. Furthermore, a second gate is placed on the n-buffer layer, surrounding a p-emitter layer. The n-emitter and p-emitter layers are electrically separated from these gates by the mesa structure.

A forward-blocking voltage of 6000 V was realized by a 550-μm n-base with the n-buffer, even at 150°C, when the second gate was shorted to the anode electrode, as indicated in Fig. 2. Leakage current was 1 mA at 6000 V, approximately 1/10th of the value for conventional anode-shorted GTO's. This is because the hole injection from the p-emitter layer was suppressed by shorting between the second gate and the anode electrode. Owing to the fact that a maximum allowable junction temperature for the conventional anode-shorted GTO's is 125°C, the double-gate GTO operates at 25°C higher junction temperature than the conventional GTO's.

B. Turn-Off Characteristics and Tradeoff Relation

It is necessary to reduce turn-off switching loss to realize high-frequency operation for high-power GTO's. The major turn-off switching loss is due to a peak tail current and a tail time at turn-off period. It is, therefore, necessary to decrease these two values without much increase in the on-state voltage. The peak tail current results from the stored charge in the n-base at the initial stage for the tail period, and the tail time corresponds to the time required to recombine the stored carriers in the n-base.

The turn-off waveforms for the double-gate triggering were compared to those for the single-gate triggering, as

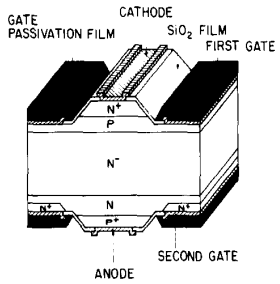

Fig. 1. Cross-sectional view of one element for double-gate GTO.

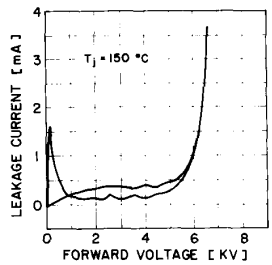

Fig. 2. *V-I* characteristics at 150°C for double-gate GTO, when second gate was shorted to anode electrode. The two leakage current curves are attributed to lead inductances and possible minor imprecision in calibration of test equipment.

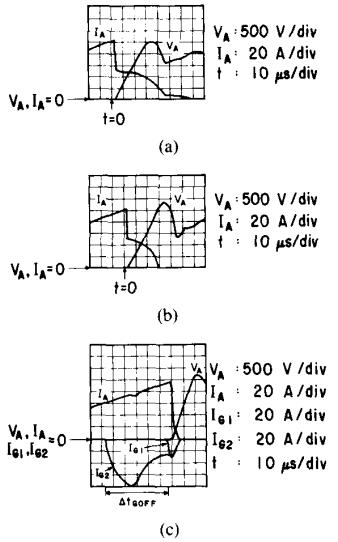

Fig. 3. Turn-off waveforms for double-gate GTO for anode voltage (V_A) and anode current (I_A) at τ_{NB} = 107 μs (a) when only first gate is reverse-biased at t = 0, (b) when first and second gates are simultaneously reverse-biased (Δt_{GOFF} = 0 μs) at t = 0, (c) when Δt_{GOFF} = 55 μs.

shown in Fig. 3(a)–(c), when n-base lifetime (τ_{NB}) is 107 μs. Fig. 3(a) shows the turn-off waveforms for the anode voltage (V_A) and anode current (I_A), when only the first gate was reverse-biased during the turn-off period. This turn-off condition is the same as the turn-off condition for the single-gate GTO's. The first gate sweeps away the excess carriers in the p-base and around the center junction. The high n-base lifetime, however, results in the high value of peak tail current, such as 52 A, as is shown in Fig. 3(a). For single-gate GTO's, it has been pointed out that the amount of excess carriers in the n-base at the initial stage for the tail current is nearly equal to that of the excess carriers at the on-state [8]. This large amount of excess carriers results in this large tail current, as seen in Fig. 3(a). For single-gate GTO's, a lifetime reduction technique has usually been employed to reduce the tail current. However, a short carrier lifetime brings about an increase in the on-state voltage. Therefore, it is difficult for the single-gate GTO's to operate at higher frequency, such as at more than 1 kHz.

The first and second gates for the double-gate GTO sweep away the excess carriers in the p-base and n-base. Fig. 3(b) shows the turn-off waveforms for the same device as Fig. 3(a), when the first and second gates were simultaneously reverse-biased. From comparison with Fig. 3(a), the tail time was reduced to less than 1/2. Even in this triggering case, however, the peak value for the tail current was almost equal to that in the single-gate turn-off case. The amount of excess carriers in the n-base at the on-state was much larger than that in the p-base, so that only a small amount of the excess carriers was swept away from the n-base before the recovery of the center junction. Therefore, it is necessary to sweep away excess carriers in the n-base before the recovery of the center junction to reduce the peak tail current.

The turn-off switching loss for the double-gate GTO was greatly reduced by adjusting a time interval (Δt_{GOFF}) between the turn-off gate pulse triggering times for the first and second gates. The turn-off waveforms for the anode voltage, anode current, first gate current (I_{G1}), and second gate current (I_{G2}) for the 55-μs time interval case are shown in Fig. 3(c). It is clearly seen that the peak tail current was greatly reduced from a value of 52 A for the single-gate turn-off condition to a value of 18 A, by introducing a time interval, such as 55 μs, even at high n-base lifetime. From these figures, it is assumed that the second gate sweeps away the excess carriers in the n-base, before sweeping away the excess carriers in the p-base by the first gate.

The turn-off loss dependence on the time interval for two n-base lifetime cases is shown in Fig. 4. There is an optimum value of the time interval for a give n-base lifetime, at which the turn-off loss reaches a minimum. This figure also shows that this optimum time interval is reduced by decreasing the n-base lifetime.

The on-state voltage for the double-gate GTO's was compared with that for the single-gate GTO's. Fig. 5 shows the experimental relations between the n-base lifetime, controlled by the electron irradiation, and the on-state voltage for the double-gate GTO's and single-gate GTO's with identical n-base and n-buffer layers. As is shown in this figure, the same relation for the double-gate GTO's and the single-gate GTO's was obtained. It can be concluded that the small p-emitter area, caused by the mesa structure for the second-gate portion, does not affect the on-state voltage in the double-gate GTO's.

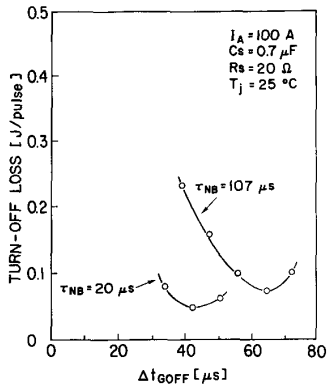

Fig. 4. Turn-off switching loss dependence on the time interval (Δt_{GOFF}) between two turn-off gate pulse triggering times for double-gate GTO at two different n-base lifetime cases.

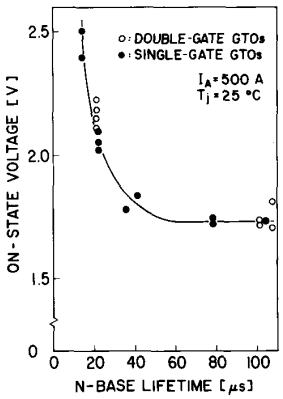

Fig. 5. On-state voltage dependence on n-base lifetime for double-gate GTO's and single-gate GTO's with identical n-base and n-buffer layers.

Fig. 6 shows a comparison in the tradeoff relations between the on-state voltage and the turn-off switching loss for the double-gate GTO's at an optimum turn-off triggering condition and the single-gate GTO's with n-buffer and anode-shorted structure, which has the smallest turn-off switching loss among the single-gate GTO's [6]. As is shown in this figure, the turn-off switching loss was reduced to approximately 1/20th of that for the single-gate GTO by the double-gate turn-off operation. This is because the turn-off loss was decreased by adjusting the time interval between the two gates, in addition to the second-gate portion not increasing the on-state voltage.

Fig. 7 shows typical 400-A turn-off waveforms for the anode voltage, anode current, first-gate current, and second-gate current during the turn-off transient. This device can turn off a larger anode current than 400 A.

C. Turn-On Characteristics

Turn-on switching characteristics for the second-gate triggering case was compared with that for the first-gate triggering case. The double-gate GTO was successfully turned on by applying forward bias to one of the two gates.

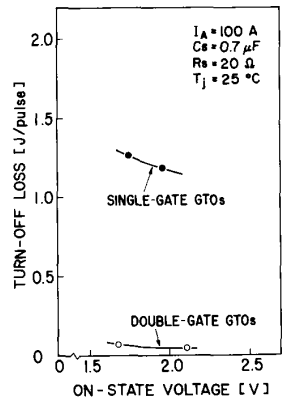

Fig. 6. Tradeoff relations between on-state voltage and turn-off switching loss for double-gate GTO's and single-gate GTO's with n-buffer and anode-shorted structure [6].

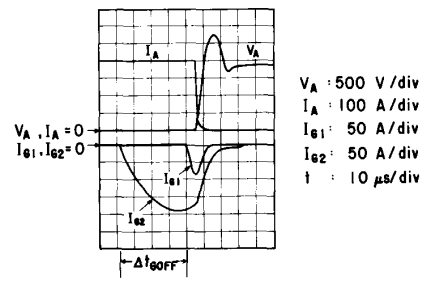

Fig. 7. Typical turn-off waveforms for anode voltage (V_A), anode current (I_A), first-gate current (I_{G1}), and second-gate current (I_{G2}) for double-gate GTO.

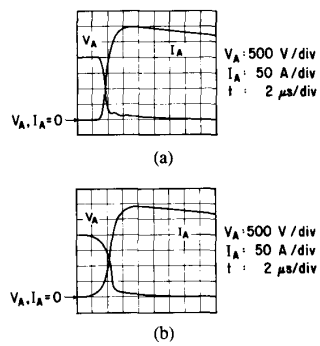

Fig. 8. Turn-on waveforms for anode voltage (V_A) and anode current (I_A). (a) First-gate triggering case. (b) Second-gate triggering case.

Fig. 8 shows the turn-on waveforms for the double-gate GTO (Fig. 8(a)) triggered by the first gate and (Fig. 8(b)) triggered by the second gate, respectively. The anode voltage for the second-gate triggering case decreased more slowly than that for the first-gate triggering case. These turn-on characteristics are a distinctive feature for the second-gate triggering case.

Fig. 9 shows turn-on loss dependence on an initial rate of a gate current rise, for the first-gate and second-gate triggering cases. The turn-on loss for the first-gate trig-

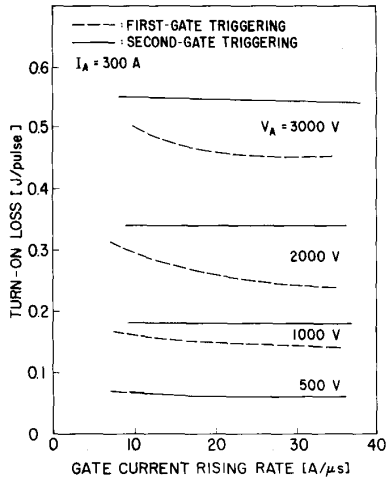

Fig. 9. Turn-on switching loss dependence on gate current rising rate for first-gate triggering and second-gate triggering at four different anode voltage cases.

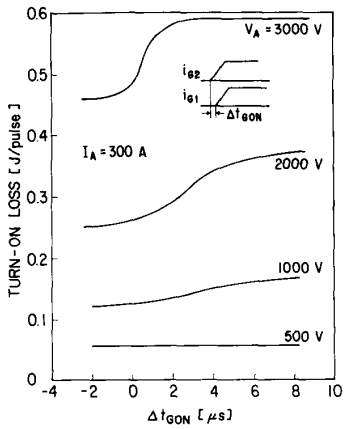

Fig. 10. Turn-on switching loss dependence on the time interval (Δt_{GON}) between two turn-on gate pulse triggering times for double-gate triggering at four different anode voltage cases.

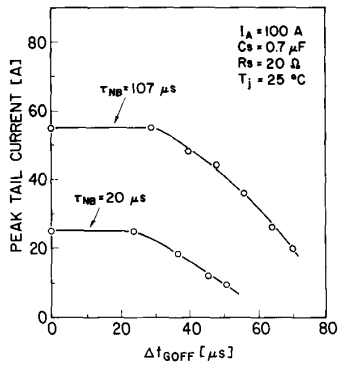

Fig. 11. Peak turn-off tail current dependence on the time interval (Δt_{GOFF}) between two turn-off gate pulse triggering times for double-gate GTO at two different n-base lifetime cases.

gering case decreased with an increase in the gate current rising rate, in the less than 20-A/μs range. In contrast to this, the turn-on loss for the second-gate triggering case was hardly affected by the gate-current rising rate. This figure also shows that the turn-on loss for the first-gate triggering case was smaller than that for the second-gate triggering case in the high gate current rising rate range.

It was found that the turn-on switching loss was changed by a time interval (Δt_{GON}) between the two turn-on gate pulse triggering times for the first and second gates. The turn-on loss for the double-gate triggering case dependence on the time interval is shown in Fig. 10. By comparison with Fig. 9, it was found that the turn-on loss was reduced by the double-gate triggering in the small anode voltage range, such as 500 and 1000 V. However, the turn-on loss, in the anode voltage range of more than 2000 V, was almost equal to that for the first-gate triggering case.

III. Discussion

It was observed that the turn-off loss was greatly reduced by a large time interval between first- and second-gate triggering pulses, such as 55 μs. This reduction was mainly caused by the reduction in the tail current. The relation between the time interval (Δt_{GOFF}) and the peak tail current for two n-base lifetime cases is shown in Fig. 11. As is obvious from this figure, the peak tail current was reduced by decreasing the n-base lifetime and increasing the time interval by more than a certain value, such as 24 and 30 μs. This time interval required to reduce the peak tail current is attributable to the time to eliminate a saturation charge in the n-base. The p-n-p transistor portion is switched from the active to the saturation mode at the on-state. While the GTO operates in the saturated mode, not only the emitter but also the collector injects. As a result, the total charge consists of the charge due to the emitter injection and an additional charge due to the collector injection which is called saturation charge [9]. In the saturation range, the saturation charge does not affect the collector current. In order to remove the transistor out of saturation, it is necessary to sweep away the saturation charge. It is assumed that a certain time interval, such as 24 and 30 μs, was required to decrease the peak tail current. The amount of the saturation charge increases with increasing anode current, so that the time interval must be adjusted to decrease the turn-off loss, corresponding to the anode current.

As mentioned above, the peak tail current decreases with increasing time interval between the first and second gate triggering pulses. On the contrary, the turn-off loss increases with increasing time interval at long time interval range, as is shown in Fig. 4. At this range, the p-n-p transistor portion is assumed to be switched from saturation into active mode by sweeping away saturation charge from the second gate. In this condition, the on-state voltage increases without much decrease in the anode current,

resulting in the high turn-off loss. It is, therefore, necessary to trigger the first gate to reduce the anode current by recovering the center junction after a certain time interval from the second gate triggering to minimize the turn-off loss.

The turn-off gain for the second gate was small, such as 1.25 and 2.1, as is obtained in Figs. 3 and 7. The turn-off gain (G_{OFF}) for the second gate is theoretically given by

$$G_{OFF} = \frac{\alpha_{pnp}}{1 - \alpha_{pnp} - \alpha_{npn}}$$

where α_{pnp} and α_{npn} are current amplification factors for the p-n-p and n-p-n transistors, respectively. In this equation, the numerator of the fraction is different from that for the first-gate turn-off gain [10]. The α_{pnp} is small as compared to α_{npn}, so that the turn-off gain for the second gate is small, as compared to that for the first gate. Consequently, a large amount of second-gate current was required to decrease saturation charge in the n-base, as is shown in Figs. 3 and 7.

It was pointed out that the turn-on loss was reduced by the double-gate triggering in the low anode voltage range, but was not reduced in the high anode voltage range. This difference can be explained by the carrier injection mechanism at the turn-on stage. Let us consider the behavior of the thyristor in its forward blocking mode, to which a gate voltage is applied. In the first-gate triggering case, initially the electrons inject from the n-emitter to the n-base. In the low anode voltage case, the injected electrons diffuse through the undepleted n-base layer to the p-emitter, accompanied by hole injection from the p-emitter. This transit time results in a turn-on delay. In the double-gate triggering case, the p-emitter forward-biased by the second gate injects holes into the n-base. As a result, short turn-on delay is realized by the double-gate triggering. This short turn-on delay causes a small turn-on loss in the low anode voltage range. In the high anode voltage range, where the whole n-base layer is depleted, the injected electrons from the n-emitter by the first-gate triggering drift across the depletion layer to the p-emitter without diffusing through the undepleted n-base layer. For the above reason, it is assumed that the double-gate triggering only reduces the turn-on loss in the range where the whole n-base layer is not depleted.

A small total power loss was realized by the double-gate GTO, even above 1-kHz operational frequency. A maximum operational frequency for the double-gate GTO's was estimated from the experimental results. A total power loss, which consists of the on-state voltage, turn-off loss, and turn-on loss, was calculated for the double-gate GTO's and the single-gate GTO's. Fig. 12 shows the total power loss dependence on the operational frequency for the double-gate GTO's and the single-gate GTO's. The small turn-off loss obtained by the second-gate operation, leads to a great reduction in the total power loss at above 1 kHz.

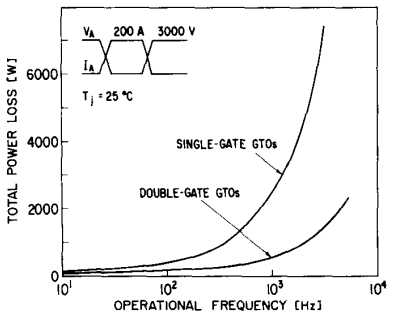

Fig. 12. Comparison in total power loss between double-gate GTO's and single-gate GTO's with n-buffer and anode-shorted structure [6].

IV. Conclusion

A 6000-V double-gate GTO, which has a second gate on an n-buffer, has been developed to achieve low switching loss for high-power PWM inverters. A 6000-V forward-blocking voltage was realized, even at 150°C junction temperature. The turn-off switching loss was reduced to approximately 1/20th of that for a single-gate GTO by adjusting the triggering times for the first and second gates. The turn-on loss for the double-gate triggering case was almost equal to that for the first-gate triggering case in the anode voltage range of more than 2000 V. A small total power loss was realized by the reduction in turn-off loss, even at above 1-kHz operational frequency.

Acknowledgment

The authors wish to thank Dr. Ohashi for support of this work.

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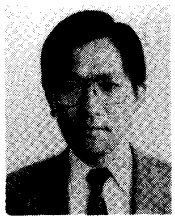

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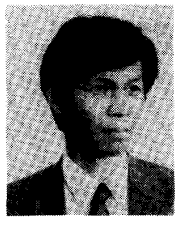

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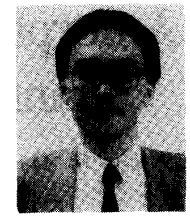

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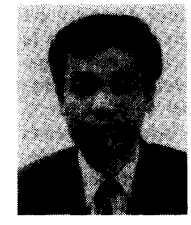

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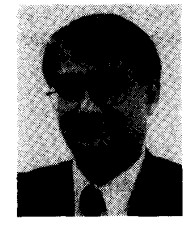
Mr. Kamei is a member of the Institute of Electrical Engineers of Japan.



Katsuhiko Takigami was born in Tomioka, Japan, on January 10, 1942. He graduated from the Takasaki Technical High School in 1960.

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