6000-V Gate Turn-Off Thyristors (GTO's) with n-Buffer and New Anode Short Structure

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***Abstract*—6000-V gate turn-off thyristors (GTO's) were developed for high-power inverters and choppers. In order to attain a high blocking voltage, simultaneously with low turn-on and turn-off losses, a combination of an n-buffer layer and a cylindrical anode short structure were implemented. A 550-μm n-base width, achieved by the n-buffer structure, can decrease turn-on loss to approximately 2/3, compared to a conventional anode short structure. The proposed structure is effective in sweeping away excess carriers during turn-off transient without increasing an on-state voltage very much. An average anode current of 200 A can be continuously switched at 900-Hz operational frequency by a 33-mm-diameter device. A simultaneous diffusion process for p-base and n-buffer layers was proposed and implemented to realize the newly developed device structure.**

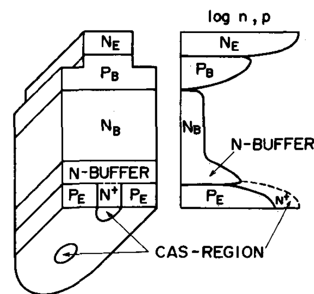

Fig. 1. Structure and impurity profile for new anode structure.

I. Introduction

HIGH-power gate turn-off thyristors (GTO's) have received much attention as a key switching device for high-power inverters and choppers. For these applications, 4500-V GTO's have already been developed [1], [2]. However, it is desirable to develop higher voltage and larger current GTO's to make these power systems still smaller. The main problem for developing higher voltage GTO's is a sensitive increase in the on-state voltage and switching power dissipation caused by the increase in n-base width. For example, for a GTO with the reverse capability, a thick n-base width, such as 1100 μm, is required to realize a 6000-V forward-blocking voltage. In order to attain high blocking voltage, simultaneously with low switching power losses, various device structures, such as anode short, n-buffer, amplifying gate, and p^+-p^- anode emitter structures [3]–[8], have already been proposed.

This paper proposes a new anode emitter structure, consisting of n-buffer and *c*ylindrical *a*node *s*hort (CAS) structures. The n-buffer structure can realize a 6000-V forward-blocking voltage with an approximately 550-μm n-base width. The CAS structure is effective in sweeping away excess carriers during turn-off transient without much increase in the on-state voltage. The fundamental characteristics for a 6000-V GTO with this new structure are described. The device was fabricated on a 33-mm-diameter silicon wafer, using conventional impurity diffusion technique only.

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II. New Anode Structure

A new anode short structure, combined with an n-buffer, has been proposed to reduce turn-off switching power loss. A simplified cross section for the one element of the proposed GTO structure is shown in Fig. 1. This GTO consists of $P_E N_B P_B N_E$ layers, n-buffer layer and anode short (CAS) region. The anode short structure for this GTO was formed by a small n^+ layer to make contact between n-buffer layer and anode electrode. The diameter for the CAS region is 60 μm. The CAS portions area is less than 1% of the total area for the p-emitter layer. A large amount of gate current is required to trigger this proposed GTO, if the anode short area is as large as that of the conventional GTO's [2], [3]. This is because the shorting resistance for the n-buffer layer is much smaller than that for the conventional GTO's. Therefore, the small CAS structure was introduced at the anode side position to increase gate triggering sensitivity. This section presents design consideration and fabrication process for this new structure.

A. n-Base Width

Generally speaking, there are three varieties of GTO structures: the reverse blocking, anode short and n-buffer structures. While the anode short and n-buffer structures do not have the reverse blocking capability, these GTO's

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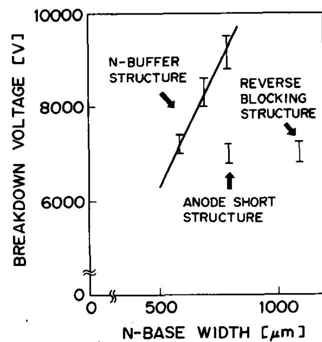

Fig. 2. Relation between n-base width and forward-blocking voltage for three GTO structures.

can be used for the most of the applications. The n-base widths for these three GTO's are compared, because the n-base width is an important device parameter in realizing low switching loss and low on-state voltage characteristics in GTO's.

The n-base width for the reverse blocking GTO must be sufficiently greater than the depletion layer width for maximum applied voltage to suppress a leakage current for the blocking state. This is because the leakage current increases as the applied voltage increases with a corresponding increase in a current gain for the p-n-p transistor portion of the GTO. For the anode short structure, the n-base width can be reduced to almost the same value as the depletion layer width, since the current gain is essentially zero in the forward blocking state. In contrast to these two structures, the n-buffer structure can realize an almost flat electric field distribution in the n-base, because the n-buffer layer prevents the depletion layer expansion and low impurity concentration n-base can be used. The same forward blocking capability can theoretically be obtained by a half of the n-base width, compared with the anode short structure. From these facts, it is concluded that the n-buffer structure is the most suitable, especially for high blocking voltage GTO's. Fig. 2 shows experimental results concerning n-base width versus forward-blocking voltage for these three structures. As is evident from this figure, the n-base width for the n-buffer structure is reduced to approximately 55% of that for the reverse blocking structure, and to approximately 75% of that for the anode short structure.

Forward blocking V-I characteristics at 25°C for the n-buffer GTO with 550-μm n-base width are shown in Fig. 3. A sufficiently small leakage current can be achieved by the n-buffer structure, even at a high junction temperature, such as 125°C.

B. n-Buffer Concentration

The n-buffer concentration dependence on device characteristics was investigated to realize an optimum design for the n-buffer layer profile. Fig. 4 shows the experimental results for the dependence of p-emitter injection efficiency (γ) and on-state voltage (V_T) on the total electric charge in the n-buffer layer (Q_N). The p-emitter injection efficiency was determined by comparison between

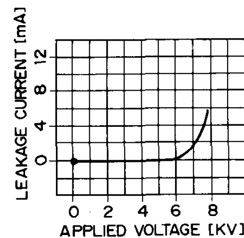

Fig. 3. V-I characteristics for n-buffer structure at 25°C junction temperature.

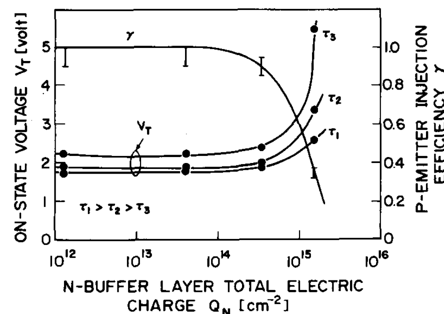

Fig. 4. n-buffer layer total electric charge dependence on p-emitter injection efficiency and on-state voltage.

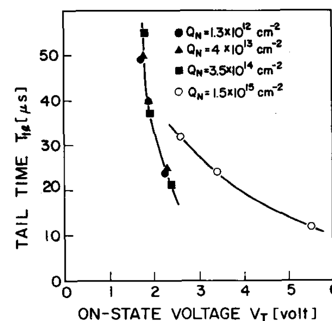

Fig. 5. Relation between tail time and on-state voltage at four n-buffer layer total electric charge values.

a current amplification factor for the p-n-p transistor portion without n-buffer and that with n-buffer, assuming the p-emitter injection efficiency without n-buffer is unity. In this experiment, the device parameters, such as p-emitter, n-base, p-base, and n-emitter doping profiles and dimensions, are constant. Therefore, the decrease in the p-emitter injection efficiency and the increase in the on-state voltage is caused by the increase in the n-buffer total electric charge. This figure shows a decrease in the p-emitter efficiency and also the increase in the on-state voltage at more than 10^{14} cm^{-2} Q_N.

The relations between tail time (T_{tl}) and on-state voltage in four Q_N value cases are shown in Fig. 5. The varied parameter for each Q_N value cases was carrier lifetime in the n-base, controlled by the electron irradiation. As is shown in Figs. 4 and 5, a better tradeoff relation between tail time and on-state voltage was obtained, when the

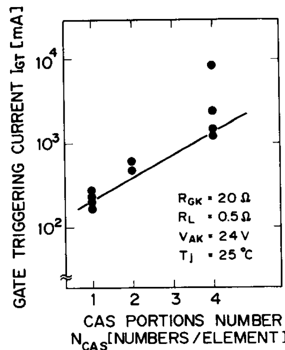

Fig. 6. CAS portions number dependence on the gate triggering current.

p-emitter efficiency was assumed to be unity. It can be concluded that Q_N must be controlled to less than 10^{14} cm^{-2}.

C. Cylindrical Anode Short Structure

The CAS portions number can be changed to control the anode shorting resistance. Fig. 6 shows the relation between the CAS portions number (N_{CAS}) and the gate triggering current (I_{GT}). As is evident from this figure, I_{GT} rapidly increases with the increase in N_{CAS}, I_{GT} can be characterized by

$$I_{GT} = \frac{V_j}{R_{sg} * \alpha_{npn}} \quad (1)$$

where V_j is a critical forward voltage for the diode, consisting of the p-emitter and the n-buffer layers, R_{sg} is the shorting resistance between these layers, and α_{npn} is a current amplification factor for the n-p-n transistor. When N_{CAS} is unity, R_{sg} is estimated to be 3.2 Ω, from Fig. 6, by assuming $V_j = 0.6$ V and $\alpha_{npn} = 0.95$. Similarly, R_{sg} is approximately 0.63 Ω for the case when $N_{CAS} = 4$. In the CAS structure, R_{sg} can be easily controlled by appropriately designing N_{CAS}. The change in R_{sg} value has only a small effect on the on-state voltage, since the CAS portion area is very small. This means that the CAS structure is superior to the conventional structure in designing the shorting resistance.

D. Fabrication Process

A simple process technique, using only conventional diffusion, has been applied to realize ideal blocking capability for a larger than 3-in-diameter wafer. Fig. 7 shows the three main diffusion steps. First, boron and phosphorus are implanted into a high-resistivity wafer from the cathode and anode sides, successively. Then, boron and phosphorus are simultaneously diffused into both sides of the wafer to form the p-base and n-buffer layers, as is shown in Fig. 7 (a). Boron is selectively diffused into the anode side to form the p-emitter layer (b). Next, phosphorus is diffused into both sides of the wafer to form the n-emitter layer and the CAS portion (c). After these main diffusion steps, chemical etching, and gate metallization processes were implemented in the same way as fabrication technique for the conventional GTO's.

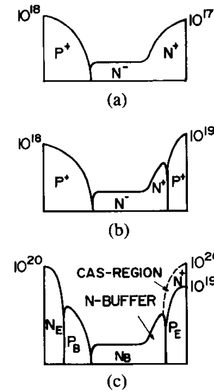

Fig. 7. Main fabrication process steps for new anode structure. (a) Simultaneous diffusion for p-base and n-buffer layers. (b) Diffusion for p-emitter layer. (c) Diffusion for n-emitter and CAS layers.

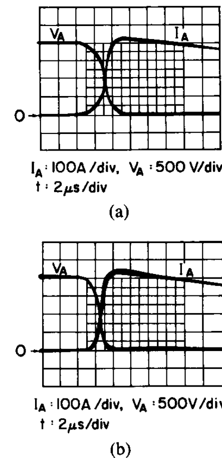

Fig. 8. Typical current and voltage waveforms during turn-on transient for (a) conventional anode short and (b) n-buffer structures at 25°C junction temperature.

Finally, main junction protection is applied to realize 6000-V forward blocking voltage for a 33-mm-diameter GTO. The advantages of this process are summarized as follows:

1) An ideal blocking capability for a larger than 3-in wafer has been realized.

2) A short diffusion time has been achieved by simultaneous diffusion for the p-base and n-buffer layers.

3) A fine anode short structure, such as 60-μm diameter CAS region, has been realized by a thin p-emitter layer, fabricated after the main drive-in process.

4) Process costs can be reduced, since only the conventional diffusion technique has been applied.

III. Switching Characteristics

A. Turn-On Characteristics

Fig. 8 shows typical current and voltage waveforms during turn-on for two types of 6000-V GTO structure, with 10-A gate currents. The top indicates the conventional anode short structure without the n-buffer and the

bottom shows the n-buffer structure. The turn-on power dissipations with time lapse, calculated from these two figures, are shown in Fig. 9. By integrating the turn-on power dissipation with respect to time, it can be seen that the n-buffer structure can reduce the turn-on loss to approximately 2/3, compared to the conventional anode short structure. It is reasonable to consider that the narrow n-base, achieved by the n-buffer structure, can decrease turn-on switching power loss in 6000-V GTO's.

B. Turn-Off Characteristics

In this paragraph, the turn-off characteristics for new anode structure will be discussed in detail. The conventional anode short structure does not exhibit a longer tail time than the reverse blocking structure, since the anode shorted portion has the effect of sweeping away the excess carriers during turn-off transient. However, the reduction in the shorting resistance for the conventional anode short structure can be realized by the decrease in the p-emitter area. This not only causes the tail time to decrease, but also causes the on-state voltage to increase. As mentioned before, at the new anode structure, it is easy to reduce shorting resistance, merely by using a small shorted area, so that the tail current can be easily decreased without an increase in the on-state voltage.

The transistor charge control model was adopted to estimate the relation between the tail current and the shorting resistance, assuming that only the p-n-p transistor portion is in an active state. The excess charge (Q_b) in the n-base is given by

$$\frac{dQ_b}{dt} = -\frac{Q_b}{\tau_b} - I_s \tag{2}$$

where τ_b is the hole lifetime in the n-base, and I_s is the current through the shorting resistance. The I_s value is related to shorting resistance R_{st} in the tail period by the following equation:

$$I_s = \frac{V_j}{R_{st}}. \tag{3}$$

The tail current (I_{tl}) is given by the following equations [9]:

$$I_{tl} = \frac{Q_b}{\tau_c} \tag{4}$$

$$\frac{\tau_b}{\tau_c} = \frac{\alpha_{\text{pnp}}}{1 - \alpha_{\text{pnp}}} \tag{5}$$

where τ_c is a minority-carrier transit time for the n-base and α_{pnp} is a current amplification factor for the p-n-p transistor. Combining (2), (3), and (4), the tail current is given as

$$I_{tl} = \frac{1}{\tau_c}\left\{\left(\tau_c I_{tl0} + \tau_b \frac{V_j}{R_{st}}\right) e^{-(t/\tau_b)} - \tau_b \frac{V_j}{R_{st}}\right\} \tag{6}$$

where I_{tl0} means the initial tail current value. Fig. 10 shows a comparison between experimental results and calculated results in two N_{CAS} cases. The measured parameters used are: $I_{tl0} = 36$ A, $\tau_b = 40$ μs. And the fit parameters used are: $\tau_c = 93$ μs, $V_j = 0.6$ V, $R_{st} = 0.05$ Ω for $N_{\text{CAS}} = 2$, $R_{st} = 0.025$ Ω for $N_{\text{CAS}} = 4$. This figure shows that experimental results can be explained well by the proposed charge control model. As is obvious from this figure, the tail current can be reduced by increasing N_{CAS}. Fig. 11 shows the relation between shorting resistance and tail time (T_{tl}), calculated using the above equations and parameters. From this figure, it is considered that T_{tl} can be reduced by decreasing R_{st}.

The relation between N_{CAS}, turn-off power loss (E_{OFF}) and on-state voltage (V_T) is shown in Fig. 12. A strong relation was observed between N_{CAS} and E_{OFF}. In contrast to this, N_{CAS} has no effect on V_T, since the CAS area is relatively small, compared to the p-emitter area, as previously mentioned. Fig. 13 shows the tradeoff relation between E_{OFF} and V_T for the CAS structure and the other two structures. This figure was obtained by varying the n-base lifetime. As is shown in this figure, the CAS structure has the best tradeoff relation among these three structures. Furthermore, it is concluded that the tradeoff rela-

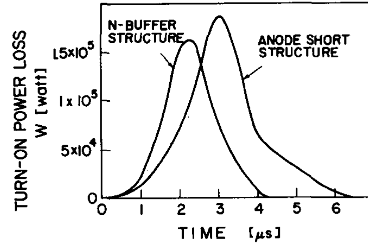

Fig. 9. Change in turn-on power dissipation with time lapse for conventional anode short and n-buffer structures at 25°C junction temperature.

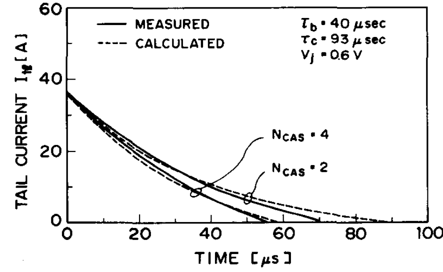

Fig. 10. Change in tail current with time lapse for new anode structure.

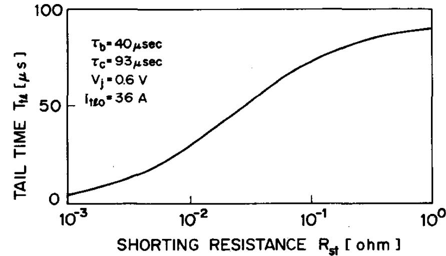

Fig. 11. Relation between shorting resistance and tail time for new anode structure.

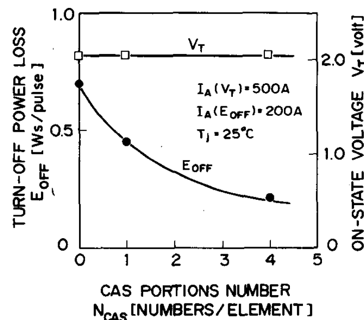

Fig. 12. CAS portions number dependence on turn-off power loss for I_A (anode current) = 200 A and on-state voltage for I_A = 500 A.

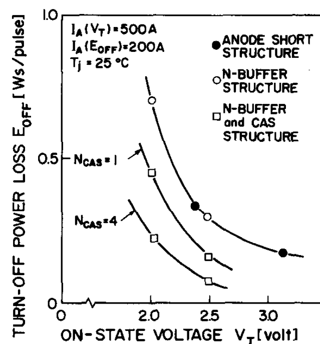

Fig. 13. Relation between turn-off power loss for I_A = 200 A and on-state voltage for I_A = 500 A.

tion in the CAS structure can be improved by increasing N_{CAS}.

C. Operational Frequency

The total power loss for the newly developed 33-mm-diameter GTO, which includes conduction and switching power losses as a function of the operation frequency, is shown in Fig. 14. The switching waveform is also shown in this figure. In the case of a press pack package cooled by water, the maximum allowable power loss is approximately 1100 W for a 33-mm-diameter GTO. Therefore, a 200-A practical anode current can be continuously switched at an operational frequency of approximately 900 Hz.

D. Maximum Turn-Off Current

Fig. 15 shows typical waveforms for the anode current (I_A), anode voltage (V_A), and gate current (I_G) for the newly developed 33-mm-diameter GTO during turn-off transient. In this test circuit, the load was inductive and a snubber circuit, consisting of a diode, resistance, and capacitance, was used. As is shown in this figure, this device can turn off more than 700-A anode current at 125°C junction temperature.

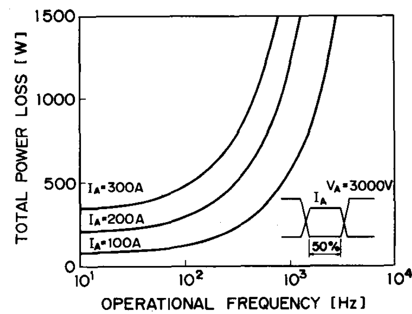

Fig. 14. Total power loss versus operational frequency for new anode structure GTO.

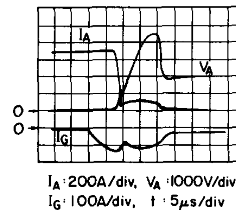

Fig. 15. Typical turn-off waveforms for anode current (I_A), anode voltage (V_A), and gate current (I_G) at 125°C junction temperature for new anode structure GTO.

IV. Conclusion

A new anode short structure, consisting of an n-buffer and a cylindrical anode short, has been developed to realize low on-state voltage and small turn-on and turn-off power losses for 6000-V blocking voltage GTO's. This device, fabricated on a 33-mm-diameter wafer, can handle a 200-A anode current at approximately 900-Hz operational frequency, and can turn off more than 700-A anode current at 125°C junction temperature. Ideal blocking voltage, short diffusion time, fine anode short pattern, and process cost reduction have been achieved by ion implantation and simultaneous diffusion for the p-base and n-buffer layers.

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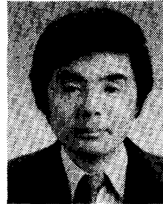

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