Numerically Predicated On-Resistances for 450-V GaAs Power SIT's Operated in the Bipolar Mode

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Abstract—**Electrical characteristics for 450-V GaAs power SIT's were numerically simulated. It was shown that GaAs SIT's can be operated in the biopolar mode even for low carrier lifetime cases. The on-resistances will be less than $\frac{1}{3.5}$ of those for silicon power MOSFET's and can be further reduced in the biopolar-mode operation.**

I. Introduction

Silicon power MOSFET's [1] are characterized by their high switching speed, low gate drive power, and large ASO. The only demerit is that the device suffers a high on-resistance when a high breakdown voltage over 1000 V is designed. GaAs power devices [2] were proposed to avoid this drawback because the electron mobility of GaAs is 5 times as high as that of silicon.

In the present brief, the electrical characteristics for 450-V GaAs SIT's are numerically simulated in order to evaluate the performace of the devices. SIT structures [3] were adopted because a further reduction in the on-resistance would be realized if biopolar-mode operation [4] is possible. First, SIT structures for more than 450-V breakdown voltages were determined, based on an actual fabrication process. Then, forward electrical characteristics were calculated for four SIT structures.

II. Calculation of Breakdown Voltage

Fig. 1 shows the four SIT structures considered. Reasonable design parameter values were adopted, assuming an actual fabrication process for the buried p-base layer, which is formed by ion implantation and annealing on an epitaxial n^- layer over an n^+ substrate before successive eptaxial n^- layer growth. Thus, the p-base thickness b should be limited to a small value such as 1 or 2 μm. The other parameter values will be inferred from the table in Fig. 1.

The breakdown voltage is limited either 1) by avalanche multiplication or 2) by the increase in the leakage current flowing over the potential barrier of the gate depletion layer, whose barrier height is decreased by the increase in the drain voltage V_D. The approximate electrostatic potential ψ can be determined by solving only the Poisson equation, based on appropriate assumptions on the quasi-Fermi levels [5]. The leakage current density J_r for the case 2) above was estimated by using only the ψ values as follows [6]:

$$J_r = -qD_n n_i \left[1 - \exp\left(-q\frac{V_D}{kT}\right)\right] \frac{Z^*}{L^*}$$

Manuscript received March 25, 1985; revised, August 21, 1985.

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IEEE Log Number 8405981.

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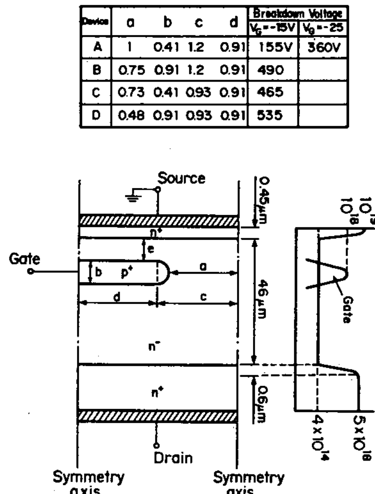


Device	a	b	c	d	Breakdown Voltage	
					V_G=-15V	V_g=-25
A	1	0.41	1.2	0.91	155V	360V
B	0.75	0.91	1.2	0.91	490	
C	0.73	0.41	0.93	0.91	465	
D	0.48	0.91	0.93	0.91	535	

Fig. 1. Modeled SIT structure and calculated breakdown voltage (values for a, b, c, and d are shown in relative scale).

$$\frac{Z^*}{L^*} = \left[\int\left[\int \exp\left(\frac{q}{kT}\psi\right) dx\right]^{-1} dy\right]^{-1}$$

all the device area. (1)

The adopted criteria for the breakdown voltage is either that the value of the ionization integral reaches unity or that the leakage current J_r exceeds 1 mA/cm^2. The calculated breakdown voltage values for the four SIT structures with the gate voltage V_G of -15.0 V are shown in Fig. 1. The breakdown voltage for the device A is determined by the increase in J_r in (1). Thus, the breakdown voltage for the -25 V gate voltage case is also shown, where the breakdown voltage was determined by avalanche multiplication. Devices B, C, and D attained more than 450-V breakdown voltages.

III. Electrical Characteristics Simulation

An ordinary two-dimensional device model [7] was used to simulate the steady state current-voltage characteristics. The impurity dependent hole lifetime τ_h was included in the model according to the following equations, which were based on experiment [8]:

$$\frac{1}{\tau_h} = \frac{1}{\tau_i} + \frac{1}{\tau_B}$$

$$\tau_i = 10^{-9}\left(\frac{10^{19}}{N_D + N_A}\right)^{0.75} \quad \text{(s)}$$

$$\tau_B = 5\ \mu\text{s}$$

$$\tau_e = \tau_h. \tag{2}$$

The electron lifetime τ_e was assumed to be the same as the hole lifetime. A relatively high carrier lifetime of 1.4 μs was assigned to the high-resistivity n$^-$ layer according to (2). A high carrier lifetime is difficult to attain in GaAs at present although it has been observed experimentally [8]. Low carrier lifetime cases (τ_B = 10 ns) were also calculated for comparison.

The carrier mobility is given by the following expressions, which include so-called negative differential mobility:

$$\mu_n = \frac{\mu_n^0 + 2.34 \times 10^{-8}E^3}{1 + 2.925 \times 10^{-15}E^4} \quad (\text{cm}^2/\text{V}\cdot\text{s})$$

$$\mu_p = \frac{\mu_p^0}{1 + 6.67 \times 10^{-8}\,\mu_p^0 E}$$

$$\mu_n^0 = \frac{5700}{1 + 1.8 \times 10^{-9}(N_D + N_A)^{0.51}} + 1500$$

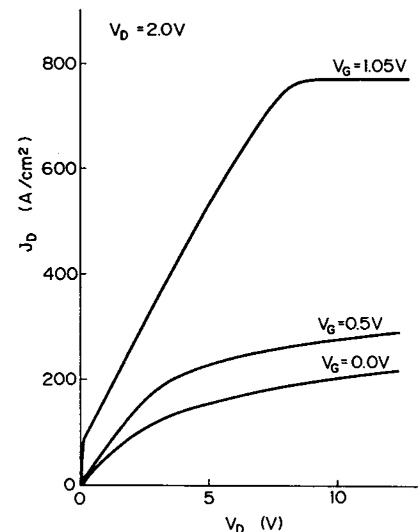


Fig. 2. Current-voltage characteristics for device C.

$$\mu_p^0 = \frac{330}{1 + 2.1 \times 10^{-9}(N_D + N_A)^{0.496}} + 50. \tag{3}$$

Electron drift velocity calculated from (3) has a peak value of 1.9 $\times$ 10^7 cm/s (N_D = 4 $\times$ 10^{14} cm^{-3}) for the critical electronic field, 3.8 $\times$ 10^3 V/cm as well as high field saturation velocity 8 $\times$ 10^6 cm/s.

A direct method was used to solve the linearized difference equations. The convergence criteria was that the relative errors ($\delta n/n$, $\delta p/p$, $\delta\psi/\psi$) $\leq 10^{-5}$.

Fig. 2 shows calculated current-voltage characteristics for device C, which has a 47-μm epi layer of 4 $\times$ 10^{14} cm^{-3} impurity concentration and 465-V breakdown voltage. The on-resistance for V_G = 0.0 V is 0.021 $\Omega\cdot$cm^2 for unit area. It decreases as the gate voltage increases. This is because the built-in depletion layer around the channel region gradually disappears and the channel opening becomes wide, as the gate voltage increases from 0 to 0.9 V.

No manifest current saturation was seen in unipolar-mode operation within the calculated drain source voltage range because the electrostatic potential barrier in the channel region is lowered with the increase in the drain voltage.

Approximate criteria (see the Appendix) for the bipolar-mode operation are given by (4) if the ambipolar diffusion length L is greater than the length $e/2$ in Fig. 1.

$$\sqrt{p\cdot n} \cong n_i \exp\frac{q}{kT}V_G > N_D(=4\times10^{14}\ \text{cm}^{-3})$$

$$L > e/2. \tag{4}$$

These yield the following conditions if carrier lifetime of 10 ns is assumed:

$$V_G > 0.9\ V, \qquad e < 10\ \mu\text{m}. \tag{5}$$

The current-voltage curve for V_G = 1.05 V is also shown in Fig. 2. Note that these characteristics are calculated with constant gate voltage conditions. A slightly different curve will be obtained if calculations are done with a constant gate current condition. For the initial low resistance region of the current-voltage curve (V_G = 1.05 V), both source and drain junctions are forward biased and whole n$^-$ layer is filled with excess carriers. For the adjacent linear region of the current voltage curve, the operation mode is similar to that of bipolar transistors, which operate in the condition of base widening. Most of the voltage drop occurs in a part of the n-base, where excess carriers are swept out. "Current-induced base" thickness reduces, and the carrier density gradient becomes steeper as the drain voltage increases, resulting in a linear increase in the drain

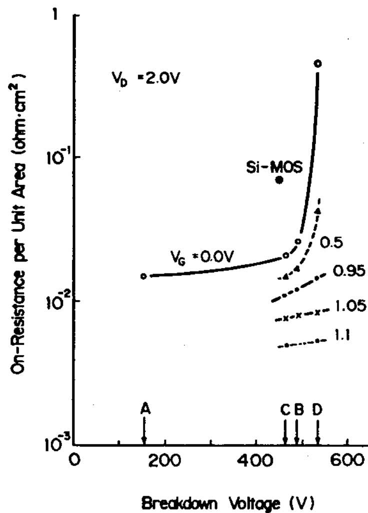


Fig. 3. On-resistances plotted against device breakdown voltage. On-resistance for the present state-of-the-art 450-V power MOSFET is plotted for comparison.

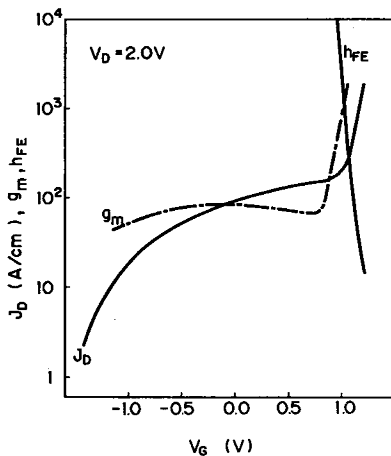


Fig. 4. Various device characteristics versus gate voltage.

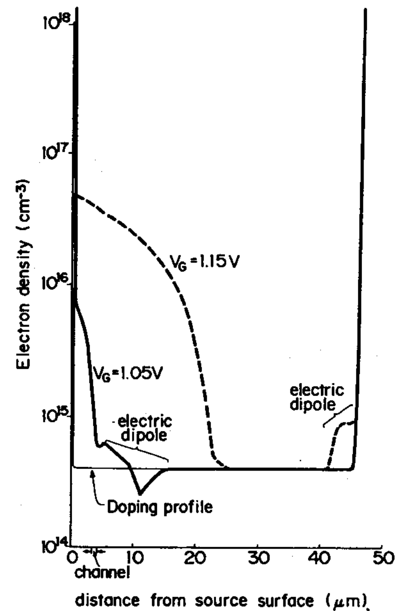
current with the drain voltage. For the current saturation region, a high electric field region appears at the base-drain junction. This corresponds to the active operation for biopolar transistors. The current saturation mechanism for this case is discussed in Section IV.

In Fig. 3, the on-resistances are plotted against device blocking voltages for each of the four devices. The on-resistance for the unipolar-mode operation ($V_G < 0.9$ V) increases as the breakdown voltage increases and the device approaches the normally-off device. In bipolar-mode operation, the on-resistance is almost independent of the breakdown voltage.

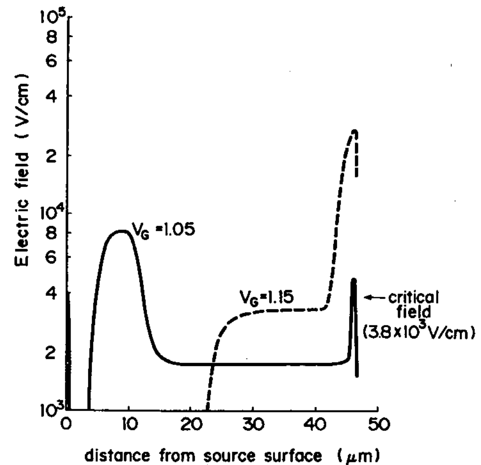
The on-resistance for the present state-of-the-art 450-V power MOSFET is also shown in Fig. 3 for comparison. On-resistances for 450-V GaAs SIT's are less than $\frac{1}{3.5}$ of that for the 450-V power MOSFET and can be decreased to less than $\frac{1}{10}$ of that for the power MOSFET if the bipolar-mode operation is introduced.

Various electrical characteristics are plotted versus gate voltage in Fig. 4. Low carrier lifetime cases were also calculated and were found to hardly change the electrical characteristics shown in Fig. 4 except current gain h_{FE} (defined by J_D/J_G), which is decreased by one order of magnitude if a carrier lifetime of 10 ns is used as the τ_B value in (2). Since h_{FE} is usually required to be more than 10, the proper bipolar-mode operation range for the gate voltage is given as follows from Fig. 4:

$$0.9 \text{ V} < V_G < 1.2 \text{ V}. \tag{6}$$



(a)



(b)

Fig. 5. (a) Electron density distribution along symmetry axis through center of channel. (b) Electric field distribution corresponding to Fig. 5(a).

IV. Discussions

In bipolar-mode operation, two types of current saturation were observed in the course of the calculation. When the drain current density is below the value of qV_SN_D (where V_S is the peak electron velocity and N_D is the n$^-$ layer donor concentraction), most of the voltage drop occurs in the high field region beneath the p-base layer. The high electric field region consits of two layers: an accumulated layer and a depleted layer, forming an electric dipole. This example is seen in the $V_G = 1.05$ V and $V_D = 12.0$ V case in Fig. 5(a) and (b). In the region where the electric field exceeds the critical value, electron density accumulation results from current continuity.

When the drain current density reaches the value qV_SN_D, a large electric field exceeding the critical field appears across the n$^-$-n$^+$ junction unless whole n$^-$ layer is filled with excess carriers. This example is seen in the $V_G = 1.15$ V, $V_D = 12.0$ V case in Fig. 5(a) and (b). The electric field in the remaining part of the high resistivity drain region remains around the critical value. This situation yields a large electron accumulation layer (electric dipole) in the vicinity of the n$^-$-n$^+$ junction, preventing the drain current from exceeding the critical value qV_SN_D. It should be noted that the drain current can exceed the critical value only in the case that the whole

n^- layer is filled with a large amount of excess carriers with a high gate voltage.

V. Conclusion

Electrical characteristics for 450-V GaAs SIT's with buried p-base layers were numerically simulated. On-resistance values for the calculated GaAs SIT's were less than $\frac{1}{3.5}$ of those for silicon power MOSFET's, although they were not strictly optimized. The on-resistance values can be further decreased if the device is operated in the bipolar mode even for a 10-ns low carrier lifetime case.

Appendix

The electron and hole density is given by:

$$p \cdot n = n_i^2 \exp \frac{q}{KT} (\phi_p - \phi_n) \tag{A1}$$

where ϕ_p and ϕ_n denote the electron and hole quasi-Fermi levels, respectively. The hole and electron quasi-Fermi level difference equals the gate-source voltage V_G if the voltage drop in the n^- region between the source and the p-base is small. This condition is satisfied if the ambipolar diffusion length L is greater than half of the n^- layer thickness between the source and the p-base.

$$L > e/2. \tag{A2}$$

Conductivity modulation is significant if the hole density is greater than the background doping N_D.

$$p > N_D. \tag{A3}$$

The following condition is derived from (A3) with (A1) and the high injection condition, $n \cong p$:

$$p \cong \sqrt{p \cdot n} \cong n_i \exp \frac{q}{kT} V_G > N_D. \tag{A4}$$

The condition (A2) is not necessarily required for the bipolar-mode condition. However, it is preferable from a device design viewpoint.

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