Simulation studies for short-circuit current crowding of MOSFET-Mode IGBT

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***Abstract*—It was experimentally found that the short-circuit withstanding capability is degraded for MOSFET-mode IGBTs, whose anode efficiency is low and the ratio of electron current over hole current is greater than the mobility ratio. New destruction mechanism of MOSFET-Mode IGBT is proposed in this paper by using large scale TCAD simulations. It is found, for the first time, that current filaments are observed during the short-circuit operation in spite of homogeneous electron channel current flow and completely symmetric cell structure. The calculated results agree well with previously reported experimental results.**

I. Introduction

The short circuit withstand capability is still an essential topic of the IGBT development. In previous works, several mechanisms for short-circuit destruction were proposed for conventional IGBTs[2][3][6] with sufficiently high anode efficiency. During the short-circuit operation of conventional IGBTs, high electric field region appears in the cathode-side of N-base.

MOSFET-Mode IGBT[1] is defined in such a way that the anode efficiency $\gamma(=J_p/J)$ is less than γ_{MOS}, which represents $\mu_p/(\mu_p+\mu_n)$. γ and γ_{MOS} are defined at the N-base N-buffer junction according to [4]. The γ_{MOS} value dynamically changes as the electric field or the lattice temperature changes inside the device because the mobility μ_p and μ_n are functions of electric field and temperature.

The net charge ρ in the high field region can be calculated with the donor density N_D.

$$\rho = N_D + p - n = N_D + \left(\frac{\gamma}{v_h} + \frac{\gamma - 1}{v_e}\right)\frac{J}{q}$$

$$= N_D + \left(\frac{v_h + v_e}{v_h v_e}\right)(\gamma - \gamma_{MOS})\frac{J}{q} \quad (1)$$

$$\gamma_{MOS} = \frac{\mu_p}{\mu_p + \mu_n} = \frac{v_h}{v_h + v_e} \quad (2)$$

where v_e and v_h are saturation velocities. For the high electric field case, γ_{MOS} is given by Eq.(2). When anode efficiency γ is less than γ_{MOS}, the second term in Eq.(1) is negative, and the net charge ρ becomes negative for sufficiently large current density J. Once the net charge becomes negative, the peak high electric field region appears in the anode side of the N-base as shown in Fig. 1. This suggests different destruction mechanism[4][5]. The measurement result of maximum short-circuit capability is shown in Fig. 2.

In order to analyze the destruction mechanism of 1200V MOSFET-mode IGBTs, TCAD simulations of a half cell and completely symmetric 8 IGBT cells have been performed with taking into account self-heating.

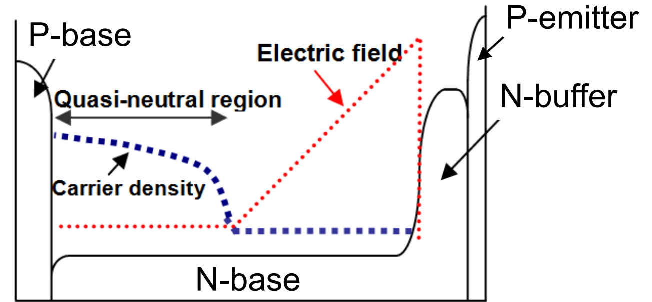

Fig.1. Electric field distribution during short-circuit operation of MOSFET-mode IGBT. High electric field region appears in the anode side for high current density cases.

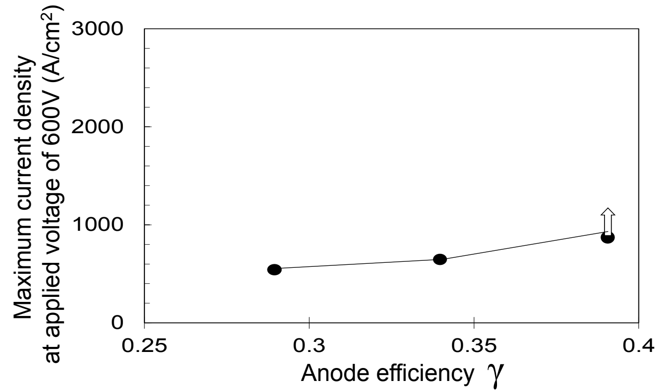

Fig.2. Measured short-circuit withstand capability[4].

II. TCAD Simulation Setup

TCAD Sentaurus Device is used for 2D and 3D simulation. In order to generate the 8-cell IGBT structure for TCAD simulation, the half cell structure with 10um width was firstly created. Then, it was reflected and copied laterally for 16 times. Thus, the doping profiles and the MOS channel structures are completely homogeneous. The N-base thickness is 120um. The doping concentrations for the P-emitter and the N-buffer are set such that the injection efficiency is less than 0.27 at the rated current density to realize MOSFET-Mode operation. The number of the mesh points of the 2D structure is approximately 100,000.

The 3D structure is created by stretching the 2D structure for 40um in the depth direction. To suppress the computation time, coarser meshes than the 2D structure are used. The number of the mesh points of the 3D structure is

approximately 1,000,000. To compare the calculation results between 3D and 2D, another similarly coarse meshes are also created for the 2D structure. The number of the mesh points of the coarse 2D structure is approximately 60,000.

Device simulation is performed with taking into account self-heating. The thermal resistance of 0.3K/W is set between the anode electrode and the heat-sink. The heat-sink temperature is set at 300K. The simulation includes lattice temperature dependence, high field saturation and carrier-carrier scattering mobility degradation models. The University of Bologna avalanche model[7], which is well calibrated for wide range of the lattice temperature, is adopted.

III. Results and Discussion

A. 2D Simulation Results

It is shown in Fig. 3 that the 8-cell structure with V_G=15V shows quicker lattice temperature increase during the short-circuit operation than the half cell. This is caused by current filamentation in the case of the 8-cell structure in spite of homogeneous electron channel current flow, as shown in Fig. 4. In the 8-cell case, the peak current density per chip is around 2,000A/cm^2 but the actual highest electron current density reaches 20,000A/cm^2 as shown in Fig. 5. Inside the current filament, the higher electron current density induces larger impact ionization in the N-base N-buffer junction, resulting in higher collector current peak in the 8-cell structure, compared with the half cell case. The high lattice temperature of 1,350K has been observed inside the current filament as seen in Fig. 3.

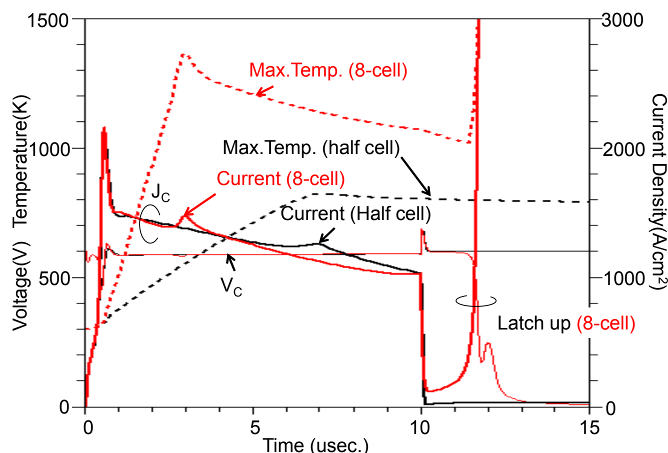

Fig.3. Comparison of the short-circuit waveforms and maximum lattice temperature change, between the half cell and the 8-cell structures when VG=15V. The 8-cell structure shows quicker temperature increase than the half cell structure. This is caused by current filamentation.

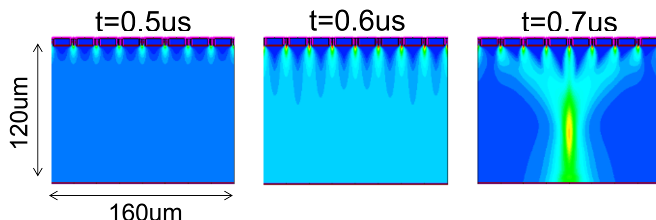

Fig.4. Electron current density distribution of the 8-cell structure for t=0.5us, 0.6us and 0.7us when V_G=15V. Current filament appears in spite of homogeneous channel current and anode structure.

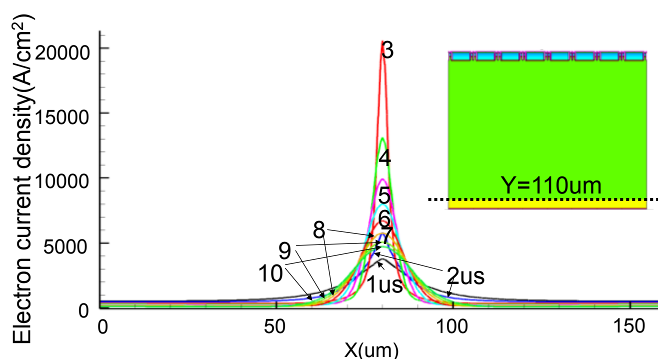

Fig.5. Electron current distributions for cross section of Y=110um, close to the N-base N-buffer junction. Numbers show time steps in unit of us. Once maximum current density reaches 20,000A/cm^2, then the filament is weakened by increased anode injection.

Another new phenomenon we have found is that the highest electric field created in the N-base N-buffer junction is not maintained anymore after sufficient lattice temperature increase. It is clearly seen in Fig. 6 that after 3us, the high electric field in the N-base N-buffer junction disappears and that a high electric field appears in the cathode-side of the N-base after 7us. The high lattice temperature region in the N-base moves from the anode-side to the cathode-side as shown in Fig. 7. In this period, the high lattice temperature in the anode-side can melt the anode metal layers and may lead to device destruction.

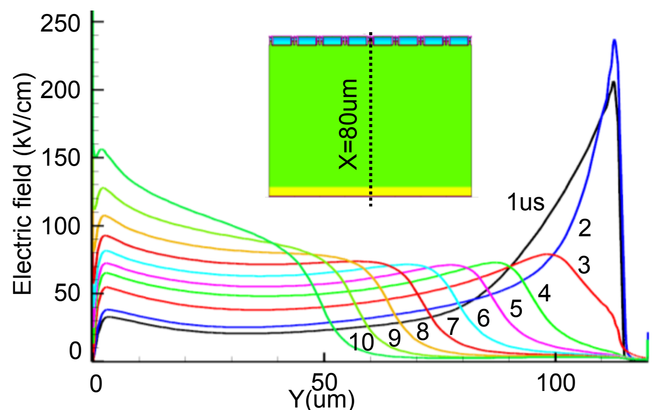

Fig.6. Electric field distribution for cross section of X=80um, center of the 8-cell structure. Numbers show time steps in unit of us. In the beginning of short-circuit operation, high electric field region is placed at the anode side. Then it moves to the cathode side.

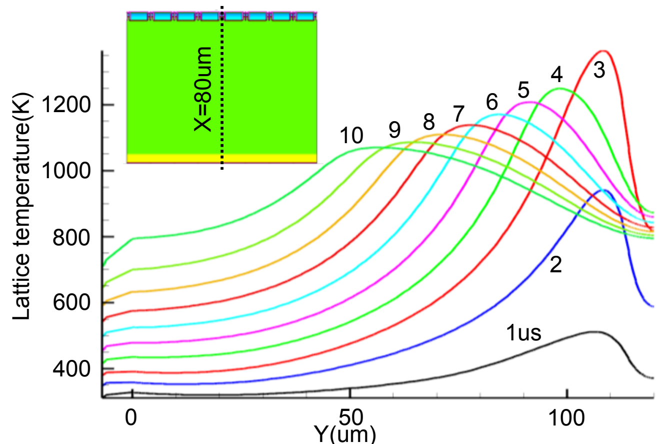

Fig.7. Lattice temperature distributions for cross section of X=80um, center of 8-cell structure. Numbers show time steps in unit of us. High temperature region moves from the anode side to the cathode side. It causes latch up.

The phenomenon mentioned above can be explained by relationship between γ_{MOS} and γ, which are defined at Y=110um. Fig. 8 shows the locus curves of γ_{MOS} and γ against lattice temperature from 0us to the time when the high electric field at the anode side disappears. Analytically calculated γ_{MOS} vs. temperature curves are also shown. As the lattice temperature increases, γ_{MOS} value initially increases to reach a local maximum value and then decreases. For the half cell case, γ value steadily increases as the lattice temperature increases. γ and γ_{MOS} finally meet at T=800K. This means net space charge become positive according to Eq. (1). Then the high electric field in the N-base N-buffer junction disappears as shown in Fig. 9(a).

For the 8-cell case, γ_{MOS} initially increases as the lattice temperature increases, then gradually decreases. Finally γ and γ_{MOS} meet at T=1,350K and the highest electric field disappears as shown in Fig. 9(b).

The 8-cell structure needs higher lattice temperature rising to eliminate the high electric field at the anode side, compared to the half cell case. This can be explained by the temperature dependence of analytical γ_{MOS}. When the electric field is higher, γ_{MOS} takes a local maximum at a higher temperature, as seen in Fig. 8. This means that the value of γ_{MOS} begins to decrease at a higher lattice temperature, when the electric field is higher. The 8-cell structure creates a current filament, where the very high electric field of 250kV/cm is observed as shown in Fig. 9. As a result, the high electric field at the anode-side is not removed until the lattice temperature reaches 1,350K.

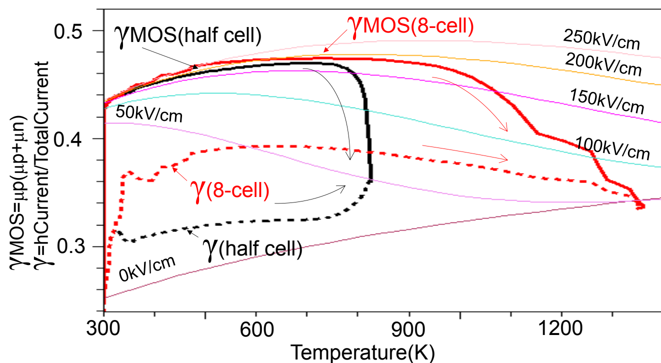

Fig.8. The locus curves of γ_{MOS} and γ are plotted against lattice temperature from 0us to the time when the high electric field at the anode side disappears (thick solid and broken lines). γ_{MOS} and γ show the values at the center of the current filament and Y=110um. The thin solid lines show analytically calculated γ_{MOS} vs. temperature curves with electric field as a parameter.

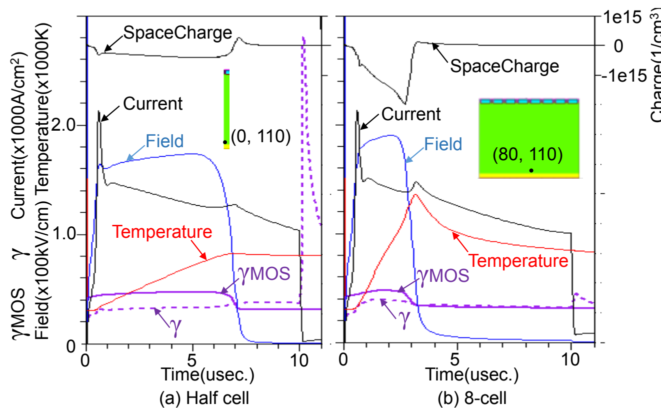

Fig.9. γ_{MOS}, γ, Space charge, Electric field, Collector current and Temperature are plotted as a function of time during short-circuit operation. All values are taken at the center of the current filament and Y=110um. A higher electric filed is observed for the 8-cell structure than for the half cell because of the current filamentation. The magnitude of electric field decreases as the value of γ_{MOS} decreases and approaches the value of γ.

High lattice temperature in the cathode-side finally causes latch-up of IGBT because the P-base region becomes intrinsic. In Fig. 10, it is found that in the 8-cell IGBT structure with anode efficiency of 0.3, the current filaments appear for V_G>14V and does not appear in the case of V_G=13V. This result implies that the device is safe when the current density is less than 1,000A/cm^2. This result approximately coincides with the measured results shown in Fig. 2.

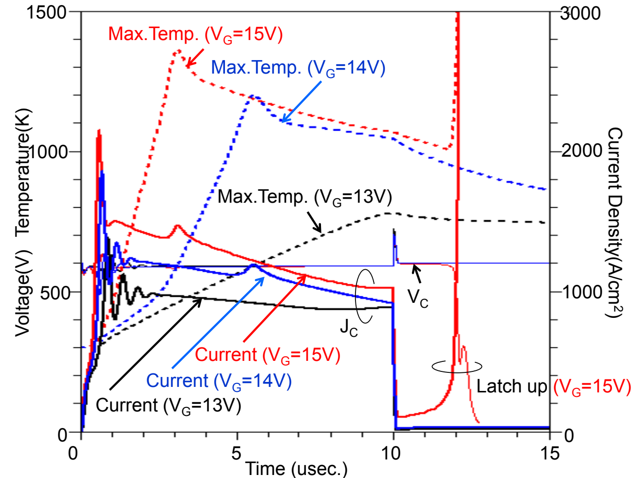

Fig.10. Comparison of the short-circuit waveforms of the 8-cell structure between V_G=13, 14 and 15V. The current filaments appear when V_G=14 or 15V. The filament does not appear in the case of V_G=13V. This implies that the device is safe when the current density is less than 1000A/cm^2. This result approximately coincides with the measured results shown in Fig.2.

It is also found that current filaments appear approximately every 160um distance. Another 8-cell structure with linearly graded wafer thickness was simulated. The N-base thickness is 118um at X=0um(the left side) and 122um at X=160um(the right side). More significant current filamentation occurs and increases the peak collector current, as seen in Fig. 11. It is shown in Fig. 12 that a large current filament appears at X=0um and the highest temperature reaches almost 1,500K. It is surprising that another current filament appears even in the thickest wafer portion at X=160um. This suggests that current filaments are forced to be created approximately every 160um distance to increase collector current by impact ionization in the N-base N-buffer junction. Fig. 13 proves it by 16-cell structure simulation.

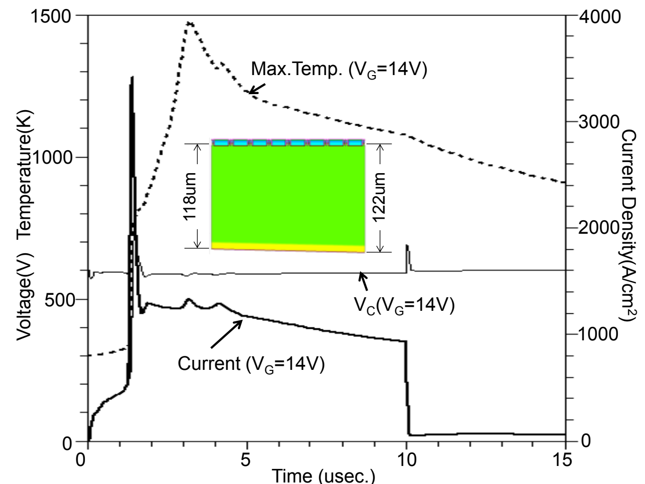

Fig.11. Calculated short-circuit waveforms for the 8-cell structure with linearly graded wafer thickness. The N-base thickness at X=0 is 118um and 122um at X=160um. The peak current exceeds 3,000A/cm^2, and the maximum temperaure reaches almost 1,500K, although V_G=14V, which is lower than V_G=15V of Fig.4.

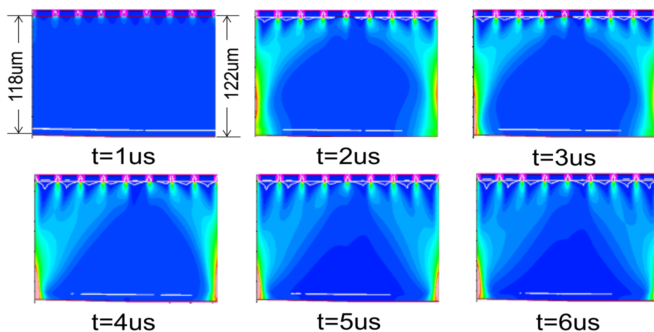

Fig.12. Electron current density distribution for the time step of 1, 2, 3, 4, 5, and 6us for the structure with linealy graded wafer thickness. A large current filament appear at the left hand side, the thinnest N-base portion of X=0. It is surprising that another current filament appears even at the right hand side, the thickest N-base portion of X=160um. This suggests that the current filaments are forced to be created approximately every 160um distance to increase collector current by impact ionization in the N-base N-buffer junction.

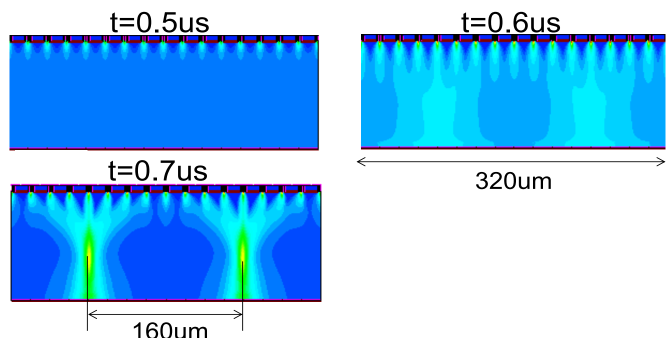

Fig.13. Electron current density distribution of the 16-cell structure for t=0.5us, 0.6us and 0.7us. Current filament appears every 160um distance.

B. 3D Simulation Results

It is shown in Fig. 14 that the three-dimensional 8-cell structure shows quicker lattice temperature increase during the short-circuit operation than 2D structures. The maximum lattice temperature reaches 1,600K, close to the melting point of Silicon. This is caused by denser current filamentation not only for lateral direction but also for depth direction in spite of homogeneous structure, as shown in Fig. 15. Current filament appears in the two diagonal corners of the XZ-plane as shown in Fig. 16.

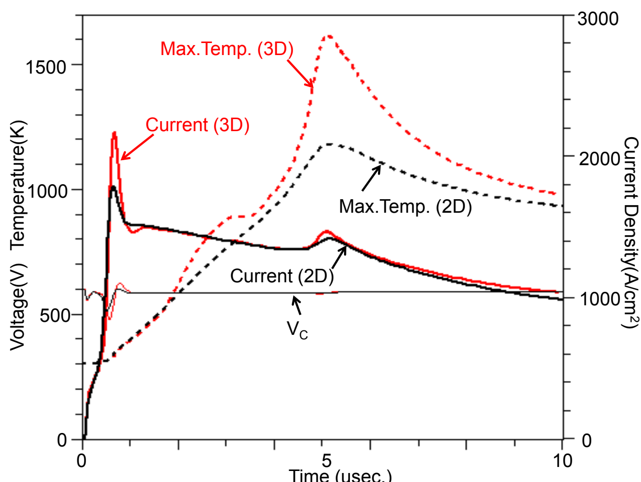

Fig.14. Comparison of the short-circuit waveforms of the 8-cell structure between 2D and 3D simulations. In the 3D simulation, the maximum lattice temperature more rapidly increased than the 2D case. In this calculation, the number of the mesh of the 2D structure is decreased from previous 2D calculations to keep compatibilty with the 3D structure.

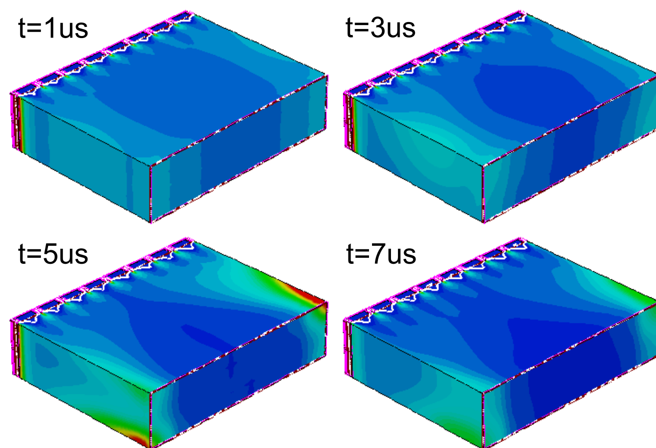

Fig.15. Electron current density distribution of the three-dimensional 8-cell structure for the time step of 1, 3, 5, and 7us for Fig.14. Current filament appears not only in lateral direction but also in depth direction.

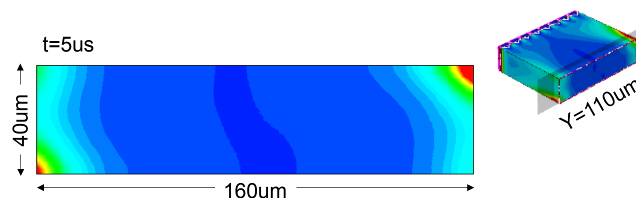

Fig.16. Electron current density distribution for the plane of Y=110um of the three-dimensional 8-cell structure for t=5us. Current filament appears in the two diagonal corners.

IV. Conclusion

New destruction mechanism for short-circuit operation of MOSFET-Mode IGBT is proposed. We identify three destruction modes; (a) Local melting metal layers in the anode contact. (b) Local melting Silicon substrate at the N-buffer N-base junction. (c) Latch up at the cathode cell. All modes are caused by current filamentation. The current filaments are observed during the short-circuit operation in spite of homogeneous electron channel current flow and completely symmetric cell structure. The calculated results agree well with previously reported experimental results.

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