1200V Bidirectional FS-IGBT (BFS-IGBT) with Superior Turn-Off Capability

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***Abstract*—In this paper, we propose Bidirectional Field-Stop IGBT (BFS-IGBT) and demonstrate its very fast turn-off capability. BFS-IGBT is characterized by the same thin N-base thickness as that of FS-IGBTs, and thus, superior to conventional bidirectional IGBTs. The device characteristics can be widely tuned by controlling the Anode side gate bias. By applying special sequence to the Anode side gate, 75% reduction of turn-off loss is realized compared with conventional FS-IGBTs. We also propose a new edge termination structure, which enables double sided blocking capability in spite of the thin N-base thickness.**

Keywords—IGBT, bidirectional, edge termination.

I. INTRODUCTION

Bidirectional FS-IGBT (BFS-IGBT[1]) has conduction and blocking capabilities for both polarities. It realizes AC-AC matrix converters, which achieve much smaller size than DC-linked type converters. For the matrix converter applications, MBS[2] structures and IGBT structures with reverse blocking capability[3] were proposed. However, in order to adapt the devices to the realistic applications, further loss reduction[4,5] and ruggedness such as short-circuit withstand capability should be required.

In this paper, we propose new BFS-IGBT by using 3D TCAD simulations[6]. The proposed device utilizes CS/N-buffer layers in order to introduce thin N-base and realize ideal carrier distribution profiles in the N-base. It improves the trade-off relationship between on-state voltage drop and turn-off loss. We show that further turn-off loss reduction can be achieved by extracting stored carriers through a N-channel, formed in the Anode side, and reducing the stored carriers prior to the turn-off[7-9]. The BFS-IGBT also realizes 10us short-circuit withstand capability.

Furthermore, we propose a new edge termination structure for the BFS-IGBT. A partially formed FS layer effectively stops the depletion layer in the termination region.

II. BFS-IGBT

A. BFS-IGBT structure and operations

The proposed device structures are designed for 1200V class. The wafer thickness and the N-base doping concentration are set to 120um and 8.0e13cm^{-3}, respectively. The proposed cell structure is illustrated in Fig. 1. In order to realize bidirectional operation, trench MOSFET cells are symmetrically formed on the front and rear side of the semiconductor wafer.

The structural parameters are summarized in Table 1. A large low concentration P-base surface, a CS/N-buffer and narrow segmented N$^+$/P$^+$ layers are formed in the surface between the two trench gates. The low concentration P-base surface realizes low hole injection efficiency when it is in the Anode side. A CS/N-buffer layer works as CS (Carrier Stored) layer and achieves high electron injection efficiency from the MOS gate[10] when it is in the Cathode side. It also works as FS (Field Stop) layer and realizes a high blocking capability. Thus, the CS/N-buffer layer improves trade-off relationship between on-state voltage drop and turn-off loss. The N$^+$ emitter width is set to 0.1um in order to reduce the saturation current, which affects short-circuit withstand capability. The operating gate voltage is 5V.

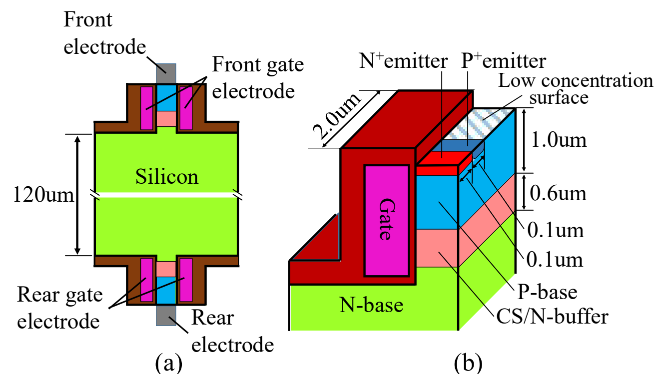

Fig. 1. Proposed BFS-IGBT structure. (a) Cross sectional view of the whole structure. (b) Schematic view of the cell design. CS/N-buffer layer is located between P-base and N-base.

Table 1. Device structural parameters.

N-base thickness	120um	Unit half cell pitch for horizontal direction	4.0um
P-base depth	1.0um	Mesa width	2.0um
Trench depth	2.0um	Gate oxide thickness	33nm

The main current is controlled by the Cathode side gate bias (V_{G1}). The hole injection efficiency from the Anode side can be increased by applying a negative Anode side gate bias (V_{G2}). When a positive V_{G2} is applied, the hole injection can be stopped by creating an N-channel in the Anode side gate. The N-channel can be used to extract the stored electrons in the turn-off operation.

In order to reduce the turn-off loss, four kinds of operations of the V_{G2} driving were analyzed, as shown in Fig. 2. The V_{G2} was always set to -5V in the on-state. The four operations, A-D, are explained as follows: Operation A: V_{G2} continues to keep -5V during the turn-off. Operation B: V_{G2} changes from -5V to +5V at the turn-off. The positive V_{G2} forms the N-channel. Operation C: V_{G2} changes from -5V to zero prior to the turn-off in order to reduce the hole injection from the Anode side, and changes from zero to +5V at the turn-off. Operation D: V_{G2} changes from zero to +5V prior to the turn-off in addition to the operation C. The positive V_{G2} switches the device operation mode from bipolar to unipolar. The intervals of the signal, Δt1 and Δt2 as defined in Fig. 2, were varied.

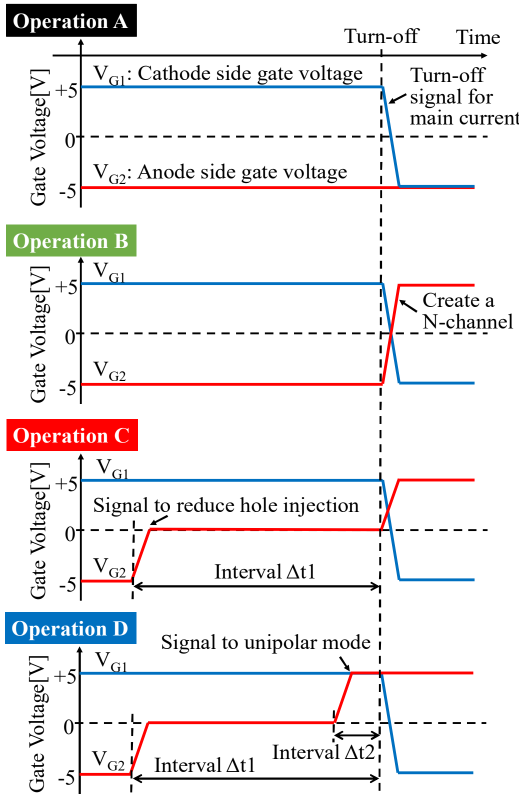

Fig. 2. Gate operations in this study.
Operation A: V_{G2} continues to keep -5V.
Operation B: V_{G2} changes from -5V to +5V simultaneously when V_{G1} does from +5V to -5V.
Operation C: V_{G2} changes from -5V to zero prior to the turn-off. Then V_{G2} changes from zero to +5V simultaneously when V_{G1} does from +5V to -5V. The first signal of V_{G2} reduces the hole injection from the Anode side. Δt1 is defined as the time interval between the first signal of V_{G2} and main gate signal of V_{G1}.
Operation D: V_{G2} changes from zero to +5V prior to the turn-off in addition to the C. The second signal of V_{G2} changes the device to unipolar mode. Δt2 is defined as the time interval between the second signal of V_{G2} and main gate signal of V_{G1}.

B. *BFS-IGBT simulation results and discussion*

It is shown in Fig. 3 that the on-state voltage drop, Vce, is as low as 1.31V at 200A/cm^2, when -5V is applied to V_{G2}. When V_{G2}=+5V, the simulated I-V curve is almost MOSFET because the hole injection from the Anode is insufficient. It is shown in Fig. 4 that the negative V_{G2} increases hole injection efficiency and raises carrier density in the Anode side. We also confirmed in Fig. 5 that the device has 10us short-circuit withstand capability.

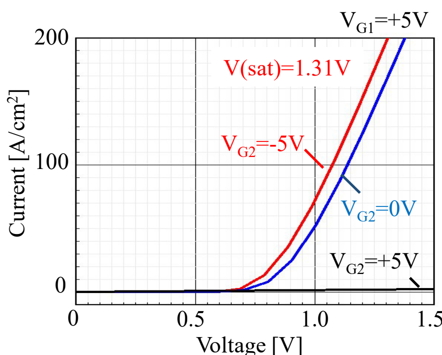

Fig. 3. Forward I-V characteristics of the BFS-IGBT. The on-state voltage drop can be reduced by applying a negative gate bias to the Anode side. The device becomes unipolar mode when a positive gate bias is applied to the Anode side.

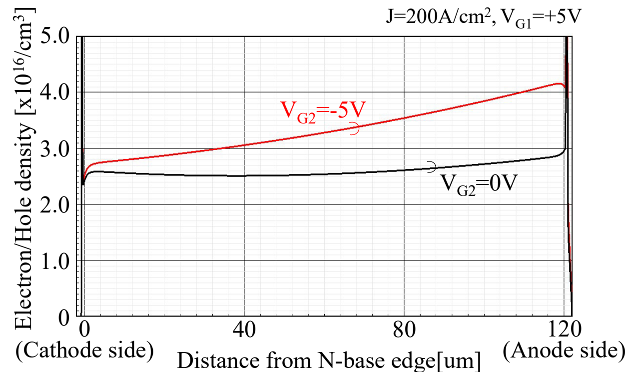

Fig. 4. On-state carrier distributions. The carrier density becomes higher when applying a negative gate bias to the Anode side gate, V_{G2}.

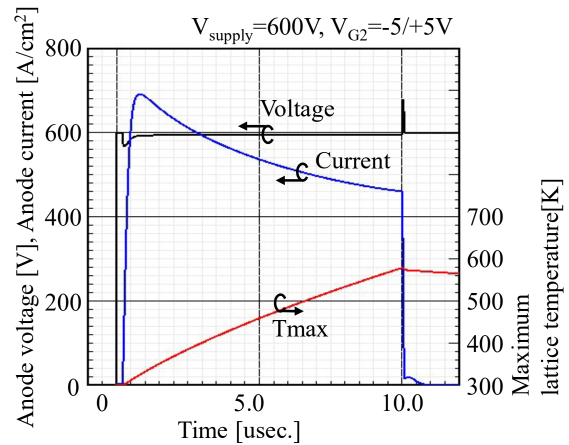

Fig. 5. Short-circuit waveforms, including self-heating. BFS-IGBTs withstand 10us short-circuit.

The turn-off waveforms of the four operation modes are shown in Fig. 6. The operation A is the same switching behavior of conventional FS-IGBT. The operation B is faster than the operation A because the excess electrons are swept out from the Anode side N-channel, formed by the positive V_{G2}. It is shown in Fig. 7 that the hole current rapidly decreases after V_{G2} exceeds Vth, and all the current flows by electron current during the fall time. Even, the hole current becomes negative. It indicates that a part of the stored hole flows toward the Anode electrode[11].

The operation C is faster than the operation B, because the excess carriers are decreased prior to the turn-off as shown in Fig. 8. There is an optimum value of Δt1, which is defined in Fig. 2. It is shown in Fig. 9 that the optimum Δt1 is 5us. If Δt1 is longer than the value, the slightly larger on-state loss results in the increased total turn-off loss. If Δt1 is shortened, the turn-off loss even becomes larger due to the higher excess carrier density as shown in Fig. 8 and approaches to the operation B.

The operation D is fastest of all because the device becomes unipolar mode prior to the turn-off. There is also an optimum value of Δt2, which is defined in Fig. 2. It is shown in Fig. 10 that the optimum Δt2 is 200ns. If Δt2 is longer than the value, the very large on-state loss results in increased total turn-off loss. If Δt2 is shortened, the turn-off loss becomes larger due to the increased residual of the excess carriers, and eventually becomes the same as the operation C when Δt2=0.

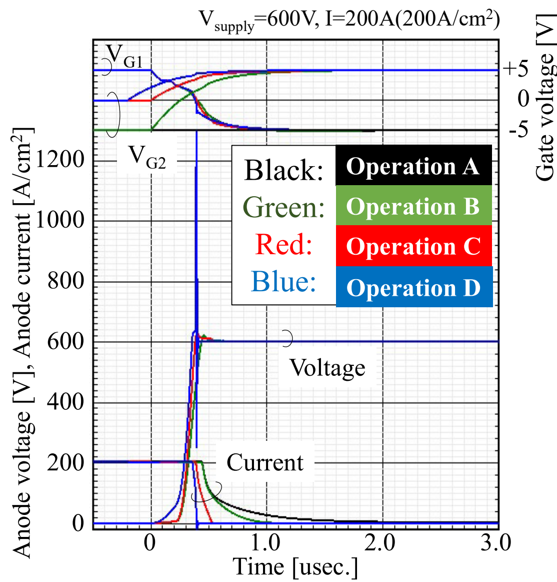

Fig. 6. Turn-off waveforms of four types of the operations. Operation D shows fastest turn-off of all.

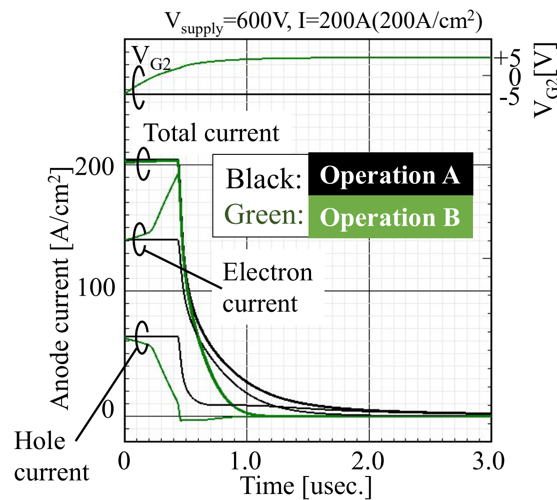

Fig. 7. Comparison of the turn-off waveforms of operation A and B. In the operation B, a large part of the stored electrons are extracted via Anode side N-channel.

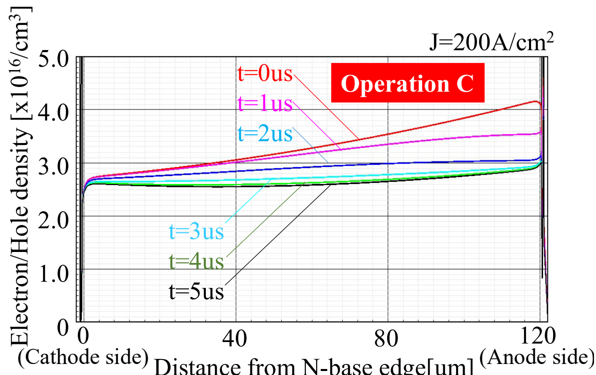

Fig. 8. Transient carrier density distributions are plotted as a function of time after V_{G2} changes from -5V to 0V in operation C. They approaches to the steady state distribution of V_{G2}=0V after 5us, which is shown in Fig. 4.

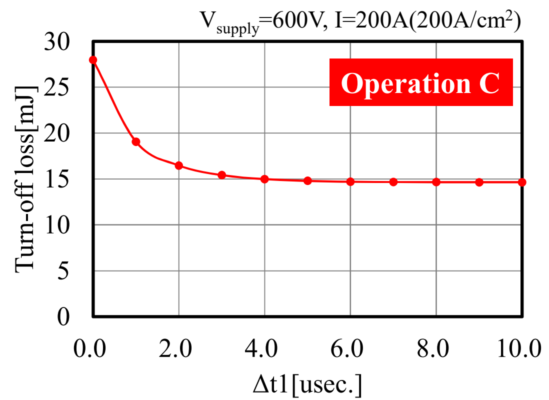

Fig. 9. Turn-off loss as a function of interval Δt1 for operation C. When V_{G2} changes from -5V to zero, 5us before turn-off, the turn-off loss becomes minimum.

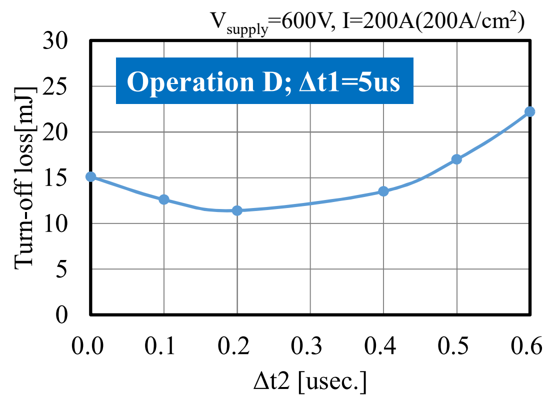

Fig. 10. Turn-off loss as a function of interval Δt2 for operation D. When V_{G2} changes from zero to +5V, 200ns before turn-off, the turn-off loss becomes minimum.

It is shown in Fig. 11 that the proposed BFS-IGBT drastically improves the trade-off relationship between on-state voltage drop and turn-off loss. 75% reduction of turn-off loss is realized for the same on-state voltage of 1.3V by adopting operation D and Δt2=200ns, compared with conventional FS-IGBTs.

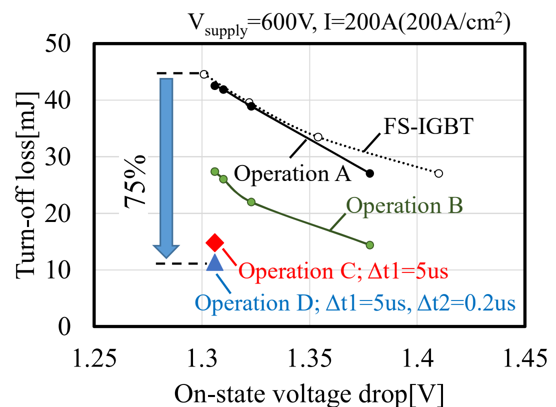

Fig. 11. Trade-off relationship between on-state voltage drop and turn-off loss. Proposed BFS-IGBT reduces 75% of turn-off loss, keeping the same on-state voltage drop, Vce.

III. Edge Termination

A. Edge termination structure

The proposed edge termination structure is illustrated in Fig. 12. In the fashion similar to the cell regions, it is symmetrically formed on the front and rear sides of the

semiconductor wafer and has many shallow and lightly doped P layers of Field Limiting Rings (FLR)[12-13]. It consists of the inner side and the outer side regions, as shown in Fig. 12. A lightly doped CS/N-buffer layer is placed underneath the inner side region in order to stop the depletion layer, when the termination region is placed in the rear side of the wafer. The distance of the two FLRs is determined by two different linear functions. The distance is set to be small in the inner region and large in the outer region.

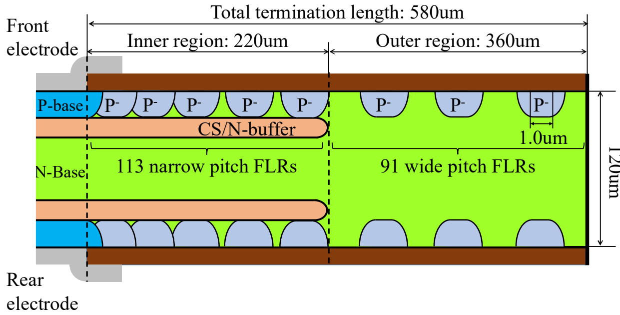

Fig. 12. Proposed edge termination structure. It is symmetrically formed on the front and rear side of the wafer. It consists of the inner and the outer regions. The CS/N-buffer layer is placed only in the inner region.

B. Edge termination simulation results and discussion

The proposed structure achieves 1310V breakdown voltage. The potential distribution of the blocking status is shown in Fig. 13. It is shown in Fig. 14 that the CS/N-buffer layer effectively stops vertical expansion of the depletion layer in the rear FLR region. There is an optimum width of the inner region to maximize the breakdown voltage. When the width is shorter than the optimum value, the breakdown voltage decreases drastically because the depletion layer reaches the FLRs in the rear side, where no CS/N-buffer exists.

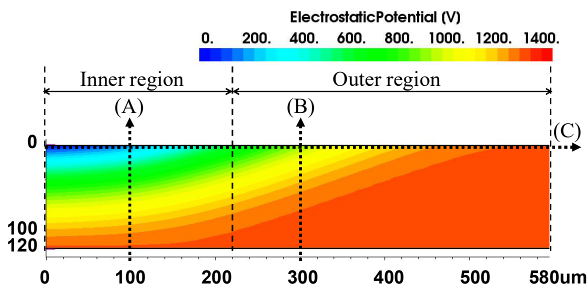

Fig. 13 Electrostatic potential distribution when breakdown occurs. The cut-lines (A), (B) and (C) in the figure are used in Figs. 14 and 15.

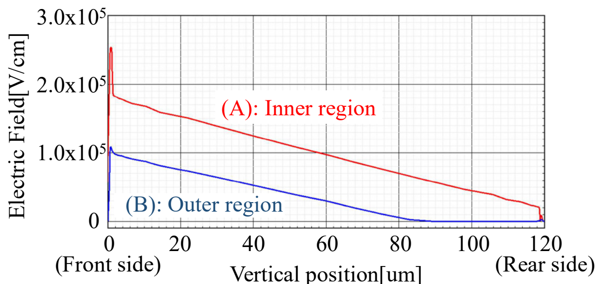

Fig. 14. Electric field distributions along the cut-lines (A) and (B) defined in Fig. 13. The line (A) indicates that the CS/N-buffer layer stops the depletion layer expansion in the inner region of the rear side. The line (B) shows that the depletion layer does not reach to the opposite side of the chip in the outer region.

It is shown in Fig. 15 that the electric field is distributed smoothly for lateral direction and no significant peak is observed, thanks to the combination of the two linear functions. When a single linear function is applied for both regions, the electric field in the outer region becomes too low. It requires wider termination region.

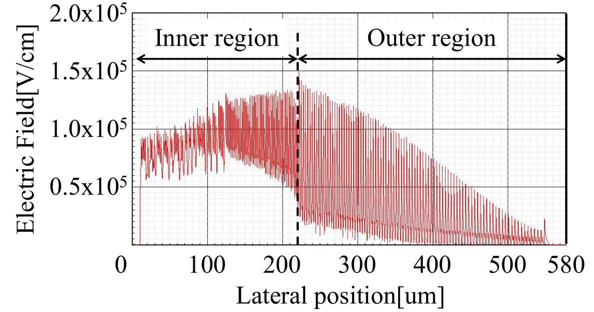

Fig. 15. Electric field distribution along the cut-line (C), defined in the Fig. 13. The electric field is distributed smoothly from the inner to the outer regions.

IV. Conclusion

New Bidirectional Field-Stop IGBT (BFS-IGBT) and new edge termination structure were proposed. Proposed BFS-IGBT achieved 75% reduction of turn-off loss compared with conventional FS-IGBTs.

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