Proceedings of the 30th International Symposium on Power Semiconductor Devices & ICs
May 13-17, 2018, Chicago, USA

Novel 3D narrow mesa IGBT suppressing CIBL

Masahiro Tanaka
Nihon Synopsys G.K.
2-21-1 Tamagawa, Setagaya-ku Tokyo, 158-0094, JAPAN.
E-mail: mtanaka@mem.iee.or.jp

Akio Nakagawa
Nakagawa Consulting Office, LLC.
3-8-74 Hamatake, Chigasaki-city, Kanagawa, 253-0021, JAPAN.
E-mail: akio.nakagawa.dr@ieee.org

***Abstract*—It was reported that the experimentally fabricated very narrow mesa IGBT has poor short-circuit withstand capability because of CIBL. We propose a novel narrow mesa IGBT, which suppresses CIBL. Additional deep P^+ diffusion layer inside the P-base improves CIBL by reducing the enhanced conductivity modulation in the channel inversion layer. The structure achieves good short-circuit withstand capability and superior trade-off relationship between on-state voltage drop and turn-off loss.**

Keywords—Narrow mesa IGBT, CIBL, Short-Circuit, Conductivity Modulation

I. INTRODUCTION

IGBTs are widely used in the middle to high power electronics field, and the market is expanding to Zero Emission Vehicles and renewable energy sources. It was predicted that the IGBTs with extremely narrow mesa realize theoretical silicon limit performance[1]. However, it was reported recently that the actually fabricated very narrow mesa IGBTs[4-8] have poor short-circuit withstand capability because of CIBL (Collector bias Induced Barrier Lowering) related current filamentation[2]. In ISPSD 2017, we showed that the cause of CIBL in the very narrow mesa IGBT is that the enhanced conductivity modulation occurs in the channel inversion layer, which includes the whole mesa region[3]. We discussed that the combination of the CIBL and high transconductance is the cause of short-circuit failure because the electric potential increase in the P-base induces the gate voltage overshoot. We also mentioned that the mesa width should be set above 200nm to prevent the conductivity modulation in the channel inversion layer of the whole mesa and achieve sufficient short-circuit withstand capability.

In this paper, we, for the first time, propose a novel narrow mesa structure with additional deep P^+ layers, which suppress CIBL even in 40nm mesa IGBTs. The potential in the deep P^+ layer becomes stable even when large current flows in the mesa region. It successfully prevents CIBL and achieves good short-circuit withstand capability. The structure even improves on-state voltage drop.

II. TCAD SIMULATION SETUP

Two types of 40nm narrow mesa 1200V IGBTs have been analyzed by TCAD 3D simulations. First one is conventional narrow mesa structure, which has 0.1um wide N^+ source and 0.4um wide P^+ contact layers (see Fig.1 and 2.) The other is the proposed structure, which has an additional deep P^+ diffusion under the P^+ contact layer. The mesa width is varied from 40nm to 100nm. The half unit cell pitch for the width direction is kept at 0.5um, and the pitch for the depth direction is 0.5um. The trench gate depth is 1.0um. The gate oxide thickness and the rated gate voltage are set to be 33nm and 5V, respectively. The N-base thickness is 100um. 8-cell IGBT structure was also used in short-circuit simulation to confirm whether current filament appears. The points: (A), (B), (C), and (D), shown in Fig. 1, are used to probe the values of potential and current density, etc. in the short-circuit simulations in the next Section. The cut-lines: (E), (F), (G) and (H) in Fig. 2 are used to plot the carrier profiles in the next section.

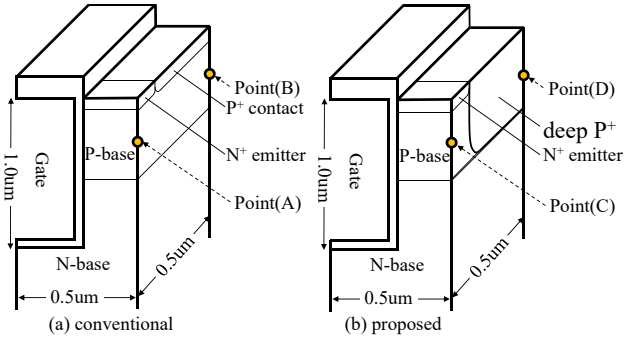

Fig. 1. Schematic view of the simulated structures. The mesa width is varied from 40nm to 100nm. Proposed structure has additional deep P^+ diffusion layer. The points: (A), (B), (C), and (D) in the figure are used to plot the values of potential and current density, etc. in Figs. 7.

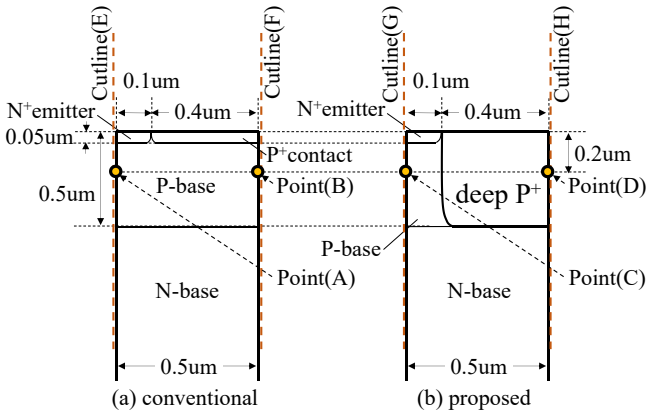

Fig. 2. Cross sectional view in the depth direction of the simulated structures. The cut-lines: (E), (F), (G) and (H) in the figure are used to plot the carrier profiles in Figs. 3, 8 and 10.

III. Results and Discussion

A. CIBL Suppression

We show that CIBL of the conventional narrow mesa IGBT can be successfully suppressed by the proposed structure. The proposed deep P^+ layer even prevents the potential increase inside the N^+ emitter. Fig. 3 shows the potential diagrams of the conduction band edge. In the conventional narrow mesa IGBT, the potential inside the N^+ emitter rises as the applied collector voltage increases. This is because the conductivity modulation occurs in the whole mesa region and the collector voltage directly affects the potential in the P-base and the N^+ emitter. In contrast, in the proposed structure, the potential is stable even when the collector voltage is high. The conductivity modulation in the channel inversion layer is weakened because a large portion of the hole current flows in the deep P^+ layer. In result, the proposed structure improves I_C-V_C saturation characteristics as shown in Fig. 4. And the proposed structure has lower transconductance than the conventional narrow mesa structure as shown in Fig. 5. It stabilizes the current level during the short-circuit operation.

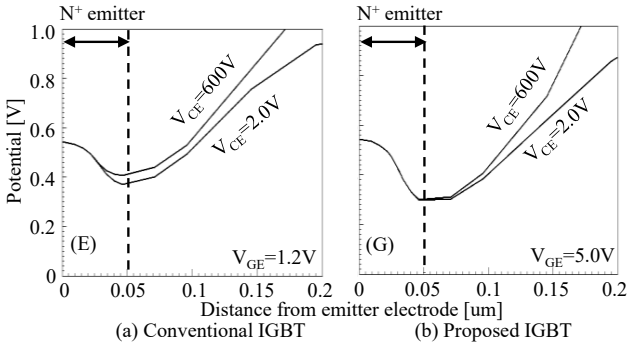

Fig. 3. Potential diagrams in the cutline (E) and (G) of calculated 40nm mesa IGBTs. Proposed structure prevents potential increase inside N^+ emitter and improves CIBL.

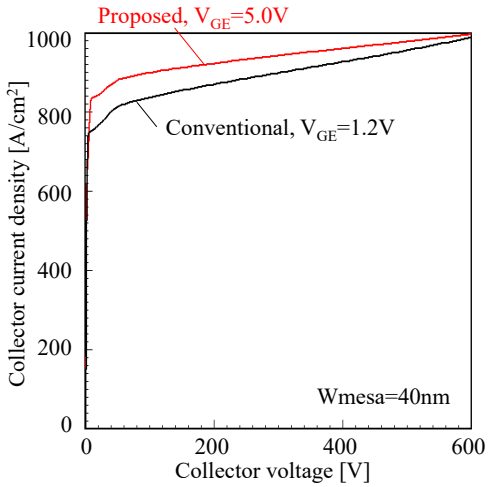

Fig. 4. Current saturation characteristics of two calculated IGBTs. The gate voltage is adjusted so that the saturation current reaches 1000A/cm^2 at V_{CE}=600V. Proposed structure shows good current saturation characteristics.

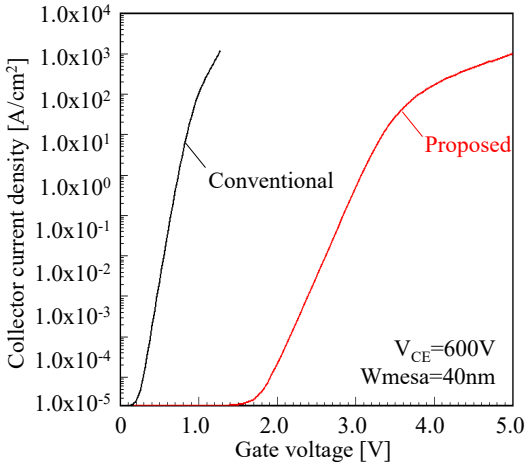

Fig. 5. I_C-V_G characteristics of calculated 40nm mesa IGBTs. Proposed structure reduces the transconductance. It stabilizes the short-circuit current.

B. Short-Circuit Withstand Capability

The proposed 40nm IGBT successfully exhibits a good short-circuit withstand capability, as seen in Fig. 6(b), although conventional 40nm mesa IGBT fails, as seen in Fig. 6(a). It should be noted that in the 40nm mesa IGBT, the whole mesa becomes channel inversion layer when a positive gate voltage is applied.

Conventional narrow mesa IGBT has poor short-circuit withstand capability because of the gate voltage overshoot during the operation. When large hole current flows in the mesa region, the potential at point (A) under the N^+ emitter becomes lower than that of point (B) under the P^+ contact layer as shown in Fig. 7(a). It follows that the hole current in the P-base flows toward the N^+ emitter and enhances the conductivity modulation in the channel inversion layer as shown in Fig. 8(a). It induces the gate voltage overshoot, resulting in the collector current increase far beyond the saturation current because of high transconductance.

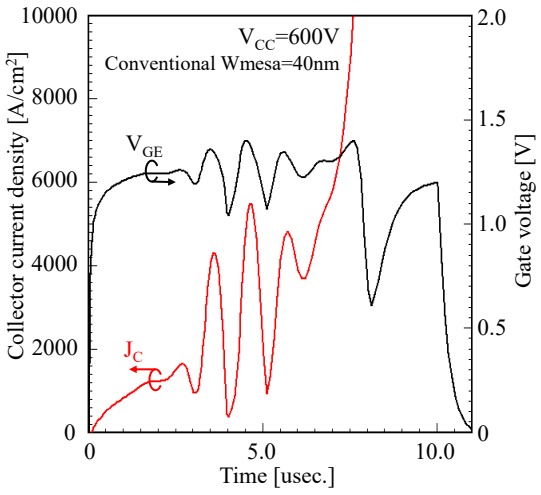

Fig. 6(a). Short-circuit waveforms of conventional 40nm IGBT. Gate voltage overshoot occurs and it increases collector current beyond the saturation current because of the high transconductance.

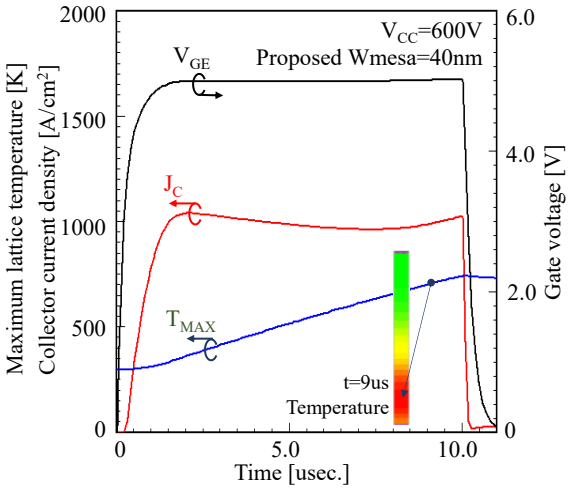

Fig. 6(b). Short-circuit waveforms of proposed 40nm IGBT. The simulated structure is 8-cell. Gate voltage overshoot does not occur. The collector current is saturated. The maximum lattice temperature was observed in the high electric field region in the N-base as discussed in[3]. No current filament was observed.

In contrast, in the proposed structure, the potential in the deep P^+ layer is stably lower than that of point (C) under the N^+ emitter during short-circuit operation, as shown in Fig. 7(b). Fig. 7(b) also shows that a large portion of the hole current flows inside the deep P^+ layer. The hole density under the N^+ emitter is greatly reduced, as shown in Fig. 8(b). The conductivity modulation in the channel inversion layer is weakened and the gate voltage overshoot is suppressed in the proposed structure. Also, the transconductance of the proposed structure is lower than conventional narrow mesa IGBT as shown in Fig. 5. In result, the proposed structure achieved stable short-circuit operation.

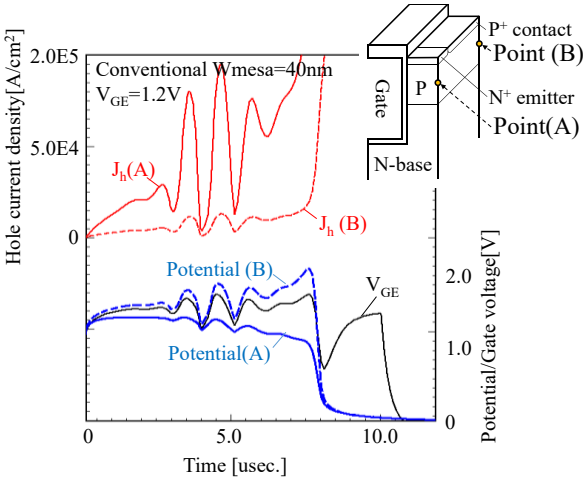

Fig. 7(a). Hole current densities, electric potentials and gate voltage are plotted as a function of time for points (A) and (B) for conventional narrow mesa IGBT during the short-circuit operation. The potential of point (A) under the N^+ emitter becomes lower than that of point (B) under the P^+ contact layer. It follows that the hole current in the P-base flows toward the N^+ emitter and enhances the conductivity modulation. It induces the gate voltage overshoot and rapidly increases the collector current, resulting in the short-circuit failure.

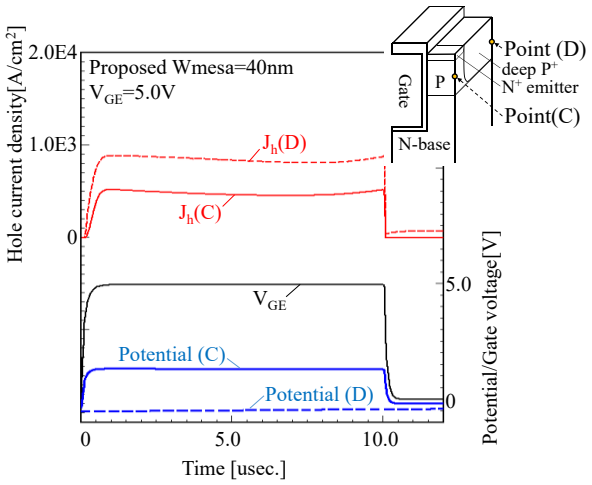

Fig. 7(b). Hole current densities, electric potentials and gate voltage are plotted as a function of time for points (C) and (D) for proposed IGBT during the short-circuit operation. The potential of point (D) in the deep P^+ layer is lower than that of point (C) under the N^+ emitter. A large portion of the hole current flows inside the deep P^+ layer. The conductivity modulation and gate voltage overshoot are suppressed.

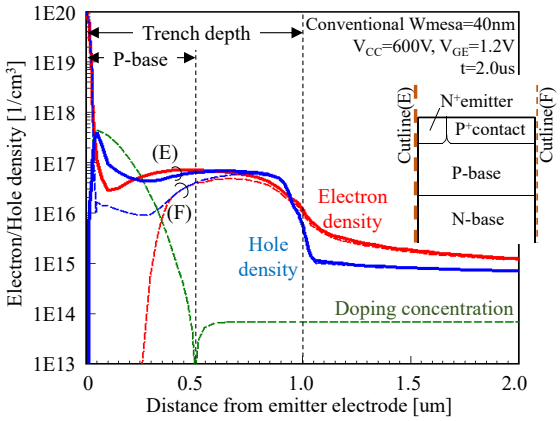

Fig. 8(a). Carrier distributions along the cut-lines (E) and (F) at t=2us are plotted for conventional narrow mesa IGBT. The hole density inside the P-base under the N^+ emitter along the cut-line (E) is high

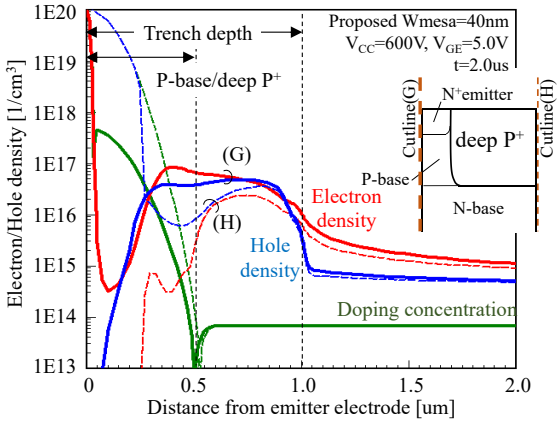

Fig. 8(b). Carrier distributions along the cut-lines (G) and (H) at t=2us are plotted for proposed IGBT. The hole density inside the P-base under the N^+ emitter along cut-line (G) is greatly reduced.

C. $V_{CE}(sat)$-E_{OFF} Trade-off

It is found that the proposed 40nm IGBT achieves very low on-state voltage drop below 1.1V as shown in Fig. 9, even if the saturation current is set to be 1000A/cm^2 at V_{CE}=600V. The rated gate voltage of 5V can be applied to the proposed IGBT because it has lower transconductance than conventional narrow mesa IGBT. Because of the higher 5V gate voltage, the higher electron density is induced in the mesa region as shown in Fig. 10, resulting in lower on-state voltage drop. Fig. 11 shows the trade-off relationship between on-state voltage drop and turn-off loss. The 40nm mesa structure realizes extremely low on-state voltage drop, which is close to the Silicon limit characteristic. It is found that the 100nm mesa IGBT with deep P$^+$ diffusion shows superior trade-off relationship of V_{CE}(sat)=1.28V at 200A/cm^2 and E_{OFF}=10mJ at 200A.

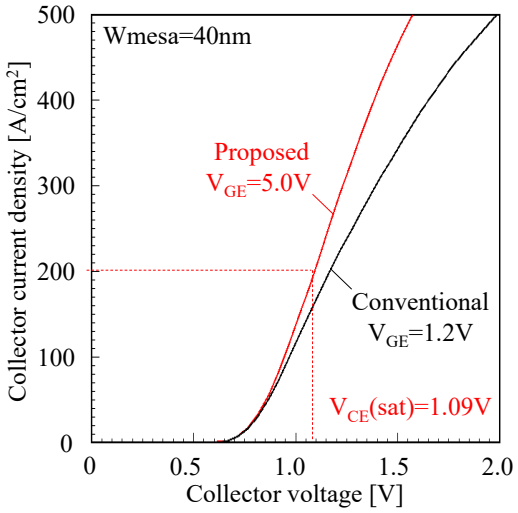

Fig. 9. I_C-V_C characteristics of calculated IGBTs. The gate voltage is adjusted as shown in Fig. 4. Proposed structure improves on-state voltage drop.

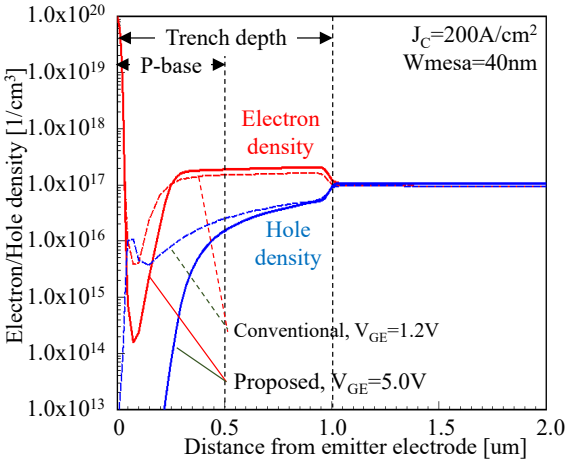

Fig. 10. Comparison of the on-state carrier distribution between the cutline (E) and (G) of calculated 40nm mesa IGBTs. The conductivity modulation in the mesa region is weakened in the proposed IGBT(solid lines). It has higher electron density in most of the mesa region than conventional one because higher gate voltage can be applied. It leads lower on-state voltage drop.

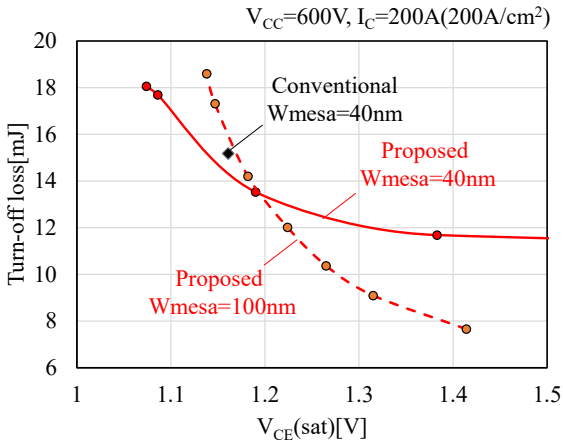

Fig. 11. Trade-off between on-state voltage drop and turn-off loss of calculated IGBTs. The stray inductance between bridge arms was set to 10nH. The gate resistance was set to 1ohm.

IV. Conclusion

A novel narrow mesa IGBT structure is proposed. Additional deep P$^+$ layer in the P-base improves CIBL by suppressing the conductivity modulation in the channel inversion layer in the narrow mesa IGBTs of 40nm and 100nm mesa width. The structure achieves sufficient short-circuit withstand capability and superior trade-off relationship between on-state voltage drop and turn-off loss.

References

[1] A. Nakagawa, "Theoretical Investigation of Silicon Limit Characteristics of IGBT", Proc. of ISPSD'06, pp. 5-8, 2006.

[2] K. Eikyu, A. Sakai, H. Matsuura, Y. Nakazawa, Y. Akiyama, Y. Yamaguchi and M. Inuishi, "On the Scaling Limit of the Si-IGBTs with Very Narrow Mesa Structure", Proc. of ISPSD'16, pp. 211-214, 2016.

[3] M. Tanaka and A. Nakagawa, "Conductivity modulation in the channel inversion layer of very narrow mesa IGBT", Proc. of ISPSD'17, pp.61-64, 2017.

[4] M. Sumitomo, J. Asai, H. Sakane, K. Arakawa, Y. Higuchi, and M. Matsui, "Low loss IGBT with Partially Narrow Mesa Structure (PNM-IGBT)", Proc. of ISPSD'12, pp.17-20, 2012.

[5] M. Antoniou, N. Lophitis, F. Udrea, F. Bauer, I. Nistor, M. Bellini and M. Rahimo, "Experimental demonstration of the p-ring FS+ Trench IGBT concept: A new design for minimizing the conduction losses", Proc. of ISPSD'15, pp. 21-24, 2015.

[6] K. Kakushima, T. Hoshii, K. Tsutsui, A. Nakajima, S. Nishizawa, H. Wakabayashi, I. Muneta, K. Sato, T. Matsudai, W. Saito, T. Saraya, K. Itou, M. Fukui, S. Suzuki, M. Kobayashi, T. Takakura, T. Hiramoto, A. Ogura, Y. Numasawa, I. Omura, H. Ohashi, and H. Iwai, "Experimental Verification of a 3D Scaling Principle for Low Vce(sat) IGBT", IEDM 2016 Technical Digest, pp. 10. 6. 1-4, 2016.

[7] H. Feng, W. Yang, Y. Onozawa, T. Yoshimura, A. Tamenori and J. K. O. Sin, "A 1200V-class Fin P-body IGBT with Ultra-narrow-mesas for Low Conduction Loss", Proc. of ISPSD'16, pp. 203-206, 2016.

[8] M. Shiraishi, T. Furukawa, S. Watanabe, T. Arai and M. Mori, "Side Gate HiGT with Low dv/dt Noise and Low Loss", Proc. of ISPSD'16, pp. 199-202, 2016.