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Conductivity modulation in the channel inversion layer of very narrow mesa IGBT

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***Abstract*—It was experimentally found that the short-circuit withstand capability of very narrow mesa IGBTs is degraded because of CIBL. In this paper, we report, for the first time, that conductivity modulation in the channel inversion layer of narrow mesa IGBT is the cause of CIBL. It is shown that the combination of the conductivity modulation and avalanche generation due to MOSFET-Mode operation causes short-circuit failure. We also propose a new cell design principle of narrow mesa IGBTs for low on-state voltage drop and good short-circuit withstand capability.**

Keywords—Narrow mesa IGBT; Short circuit; Current filament.

I. Introduction

IGBT is still widely used in the middle to high power electronics field although the wide bandgap devices were commercialized, recently. It was predicted that the IGBTs with extremely narrow mesa realize theoretical silicon limit performance[1]. However, it was reported recently that the actually fabricated very narrow mesa IGBTs[5-9] have poor short-circuit withstand capability because of CIBL (Collector bias Induced Barrier Lowering) related current filamentation[2]. The failure mechanism has not been clarified yet.

In this paper, first, we closely analyze the mechanism of CIBL and its related current filamentation by TCAD simulations. We report, for the first time, that conductivity modulation occurs in the channel inversion layer of very narrow mesa IGBTs. This increases the conductivity in the channel and increases the collector current of narrow mesa IGBT. This is the cause of collector current increase by so-called "CIBL". Second, we report that there are two reasons for the CIBL related current filamentation during the short-circuit operation. Third, we propose a new device design of the narrow mesa IGBT. The structure is characterized by an optimized mesa width and a cell pitch, uniformly doped P-base layer and a thinner gate oxide for 5V gate drive. The proposed structure realizes a lower on-state voltage drop and a practical saturation current by effectively suppressing CIBL. The device is expected to have good short-circuit withstand capability.

II. TCAD Simulation Setup

The simulated IGBTs were 1.2kV rated and had the N-base thickness of 120um. The simulations included the IAL (Inversion and Accumulation Layer) mobility model to accurately reproduce the carrier distributions in the narrow mesa, as well as conventionally used mobility models and generation-recombination models. TCAD Sentaurus Device was used for all the simulations.

In order to analyze the mechanism of CIBL, the mesa width was varied from 20nm to 1.0um. The trench depth and the P-base depth were fixed at 2.0um and 1.0um respectively. The gate oxide thickness is 100nm. The half cell pitch W was fixed at 10um, if not specified.

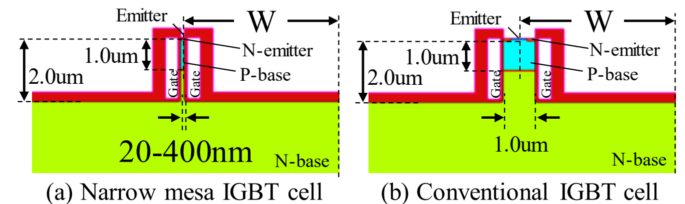


Fig. 1. Cross sectional view of simulated structures.

III. Results and Discussion

A. CIBL mechanism

Fig. 2 shows the on-state carrier distributions in the center of the mesa region. If the mesa width is extremely narrow, the whole mesa becomes an inversion/accumulation layer. We found that conductivity modulation occurs in the inversion layers of the P-base in 20nm and 100nm mesa IGBTs, and both electron and hole densities become greater than the impurity density of the P-base. This is because the hole current flows into the inversion layer of the P-base. This effect does not occur in conventional IGBTs because the hole current flows into the neutral P-base and does not flow inside the channel.

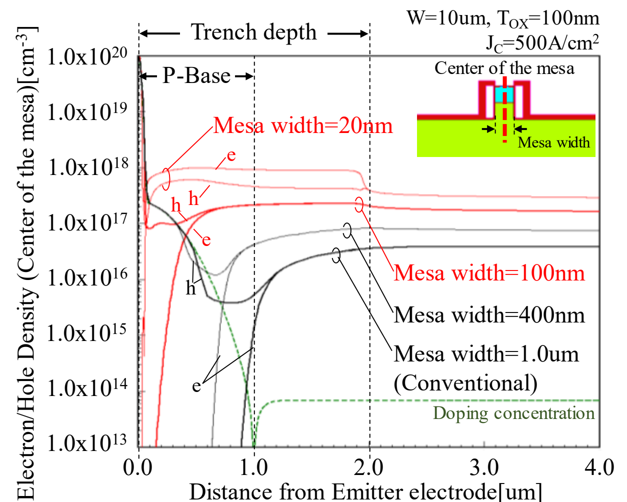


Fig. 2. Carrier distributions in the center of the mesa region. Very high conductivity modulation occurs in the channel inversion layer of 20nm & 100 nm mesa IGBTs. Both the electron and hole densities far exceed the P-base impurity doping density in 20nm mesa IGBT.

Fig. 3 shows I_C-V_G curves of the narrow mesa IGBTs. If the mesa width is extremely narrow, less than 100nm, the threshold

voltage becomes lower and the transconductance becomes higher because the conductivity modulation occurs in the inversion layer of the P-base. The combination of the CIBL and high transconductance may cause short-circuit failure because slight gate voltage instability may cause large variation of the collector current.

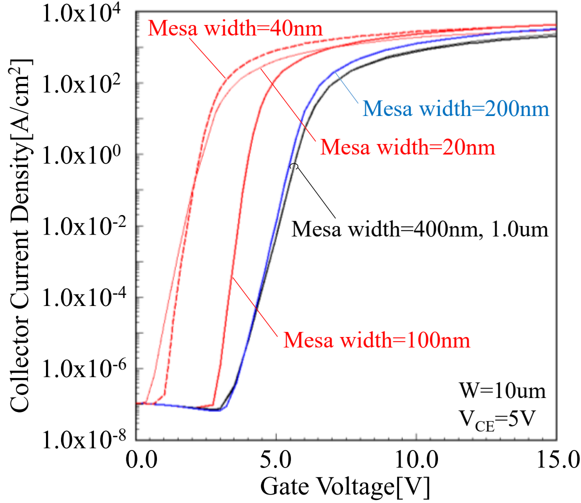


Fig. 3. I_C-V_G characteristics of the narrow mesa IGBTs. As a consequence of the conductivity modulation, the threshold voltage becomes lower and the transconductance becomes higher in case that the mesa width is less than 100nm.

B. CIBL related short-circuit failure mechanism

We found two causes for CIBL related short-circuit failure. Both are induced by the MOSFET-Mode operation[3]. MOSFET-Mode is defined in such a way that the anode efficiency $\gamma(=J_p/J)$ is less than γ_{MOS}, which represents $\mu_p/(\mu_p+\mu_n)$. γ and γ_{MOS} are defined at the N-base N-buffer junction.

The net charge ρ in the high field region can be calculated with the donor density N_D.

$$\rho = N_D + p - n = N_D + \left(\frac{\gamma}{v_h} + \frac{\gamma - 1}{v_e}\right)\frac{J}{q}$$
$$= N_D + \left(\frac{v_h + v_e}{v_h v_e}\right)(\gamma - \gamma_{MOS})\frac{J}{q} \qquad (1)$$
$$\gamma_{MOS} = \frac{\mu_p}{\mu_p + \mu_n} = \frac{v_h}{v_h + v_e} \qquad (2)$$

where v_e and v_h are saturation velocities. For the high electric field case, γ_{MOS} is given by Eq.(2). When the anode efficiency γ is less than γ_{MOS}, the second term in Eq.(1) is negative, and the net charge ρ becomes negative for sufficiently large current density J. Once the net charge becomes negative, a high electric field region appears in the anode side of the N-base.

(i) Current filament formation by anode side avalanche

Fig. 4 shows that the electron injection efficiency of very narrow mesa IGBTs exceeds 0.9. This means that very narrow mesa IGBTs operates in the deep MOSFET-Mode. Thus, when a large collector voltage is applied to narrow mesa IGBTs, a high electric field appears at the N-base N-buffer junction, and induces a large avalanche generation, as shown in Fig. 5. The generated holes flow into the narrow mesa and enhances the conductivity modulation of the mesa as shown in Fig. 6. Thus, the collector current of narrow mesa IGBTs significantly increases as the collector voltage increases, as shown in Fig. 5.

When the avalanche generation in the N-base N-buffer junction exceeds a critical value, current filaments appear even in the isothermal condition[4]. Because the hole current density is significantly large inside the filament, this enhances the conductivity modulation of the very narrow mesa and creates larger current density filaments, as shown in Fig. 7.

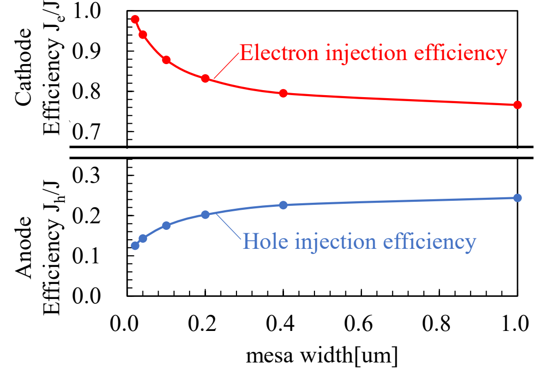


Fig. 4. Relationship between the injection efficiencies and the mesa width. The electron injection efficiency exceeds 0.9 in very narrow mesa IGBTs.

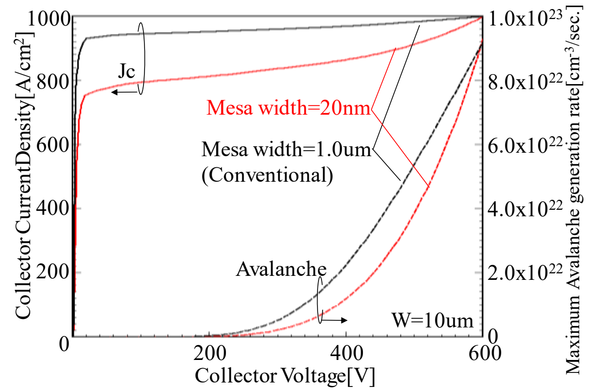


Fig. 5. Current saturation characteristics are shown for 20nm and 1um mesa IGBTs. The different gate voltage is applied for each device so that the saturation current reaches 1000A/cm² at V_{CE}=600V. The collector current of the 20nm mesa IGBT significantly increases as the collector voltage increases. For both IGBTs, large avalanche generation occurs at the N-base N-buffer junctions when $V_{CE} > 200$V.

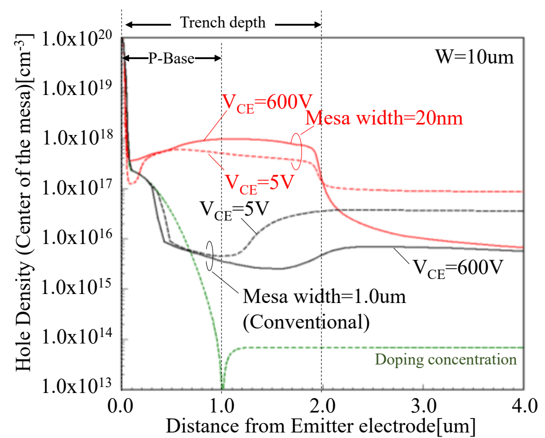


Fig. 6. Carrier distributions in the mesa region for V_{CE}=5V and 600V. The carrier densities in the mesa of the narrow mesa IGBT are increased by the avalanche induced holes.

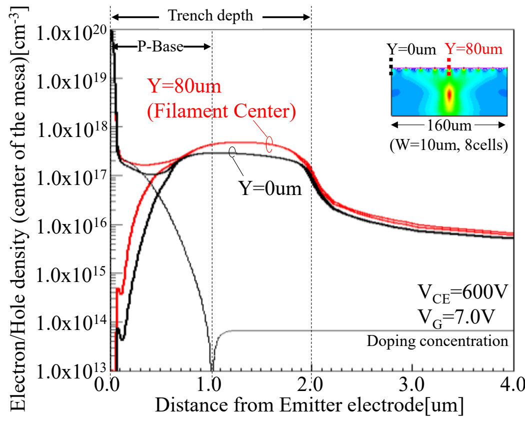


Fig. 7. Carrier distributions in the mesa region of the 20nm mesa IGBT are plotted along the line of Y=80um (center of the current filament) and Y=0um (outside the current filament). The conductivity modulation is enhanced inside the filament in spite of the isothermal simulation.

(ii) Temperature dependence of MOSFET-Mode operation

The saturation current of the narrow mesa IGBT increases as the lattice temperature rises as shown in Fig. 8. This phenomenon can be explained by the temperature dependence of the γ_{MOS} value. As shown in Fig. 9, the γ_{MOS} value dynamically changes as the electric field or the lattice temperature changes inside the device because the mobility μ_p and μ_n are functions of electric field and temperature.

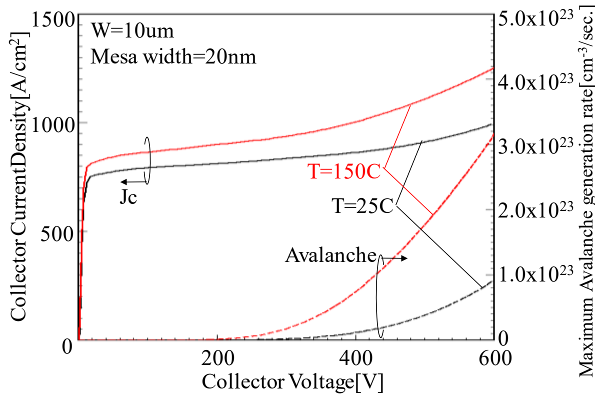


Fig. 8. Temperature dependence of the current saturation characteristics are shown for 20nm mesa IGBT. The gate voltage is adjusted so that the saturation current reaches 1000A/cm² at V_{CE}=600V and T=25C. The collector current significantly increases as V_{CE} increases at T=150C due to avalanche generation.

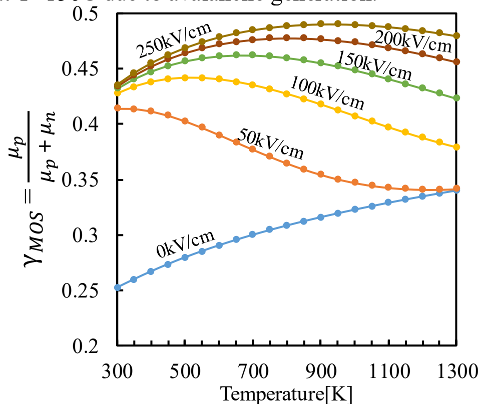


Fig. 9. Analytically calculated γ_{MOS} vs. lattice temperature with electric field as a parameter.

In the high field condition, the γ_{MOS} value increases as the lattice temperature rises over the room temperature. This further increases the electric field as well as the avalanche generation rate at the N-base N-buffer junction, resulting in more severe current filament formation because of the positive feedback between the increase in γ_{MOS} and the temperature rise.

C. Minimization of the on-state voltage drop

Conventional IGBTs have an optimum ratio of mesa width over the cell pitch for a minimum on-state voltage drop and maximized IE effect, as seen in Fig. 10, where on-state voltage drop is shown as a function of half unit cell pitch W. Regarding the very narrow mesa IGBTs, it is found that the on-state voltage drop simply reduces as the unit cell pitch becomes narrower. This tendency comes from the fact that the whole mesa becomes an inversion/accumulation layer and increases the electron density under the trench bottom, directly enhancing the electron injection efficiency. This mechanism is quite different from conventional IE effect.

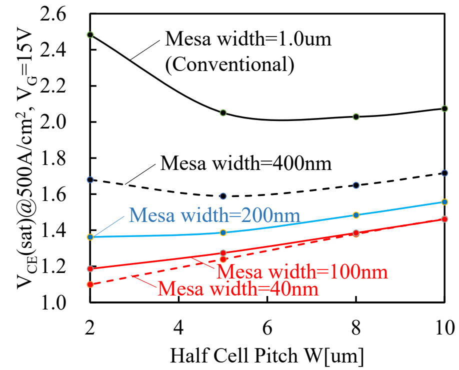


Fig. 10. On-state voltage drop as a function of half unit cell pitch W. In the conventional IE effect, V_{CE}(sat) takes a minimum depending on the ratio of mesa width over the cell pitch. In the narrow mesa IGBT, V_{CE}(sat) simply decreases as cell pitch reduces because the whole mesa becomes an inversion/accumulation layer.

IV. SHORT-CIRCUIT SIMULATION AND PROPOSED STRUCTURE

In order to realize good short-circuit withstand capability, the conductivity modulation inside the channel has to be prevented. We executed short-circuit simulations using the two IGBT structures of 100nm and 200nm mesas. The 200nm mesa probably is a minimum mesa width, which is sufficient to prevent the conductivity modulation in the channel inversion layer. The half cell pitch W is set as 4um to realize a low on-state voltage drop and the positive temperature dependence of the saturation current. If much narrower W is chosen for 200nm IGBTs, the device saturation current increases as temperature increases over the room temperature. This may degrade the short-circuit withstand capability.

We found that, according to the well-known "long channel MOSFET theory:"

$$I_{saturation} \propto \frac{(V_G - V_{TH})^2}{T_{OX}},$$

the IGBT saturation current $I_{saturation}$ can be successfully reduced without sacrificing the low on-state voltage drop by simultaneously reducing both the thickness T_{OX} of the gate oxide and the applied gate voltage V_G with keeping the same magnitude of the applied gate electric field. The gate oxide thickness is set at 33nm and the gate voltage is, thus, set at 5V in place of 15V. The P-base impurity profile is set as uniform and the concentration is $6\text{x}10^{17}/\text{cm}^3$ for 100nm IGBT and $4\text{x}10^{17}/\text{cm}^3$ for

200nm IGBT, respectively. The uniformly doped P-base is good to reduce the saturation current. A lightly doped N-buffer[10] is also applied to reduce the avalanche generation at the N-base N-buffer junction.

The on-state voltage drop of the 200nm mesa IGBT is 1.25V for 200A/cm^2. Fig. 11 shows the current saturation characteristics of the two IGBTs. The saturation current decreases as the lattice temperature becomes higher.

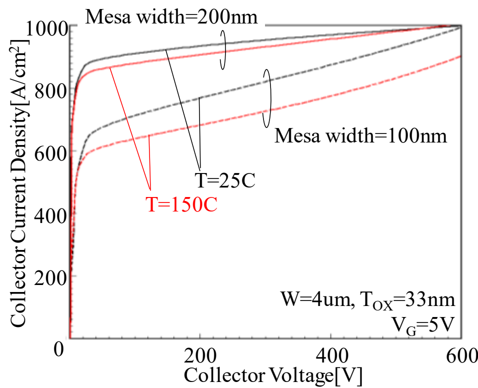


Fig. 11. Current saturation characteristics of proposed IGBT. The different P-base impurity concentration (4x10^{17}/cm^3 for 200nm and 6x10^{17}/cm^3 for 100nm mesa device) is applied for each device so that the saturation current reaches 1000A/cm^2 at V_{CE}=600V in T=25C. The saturation current has positive temperature dependence.

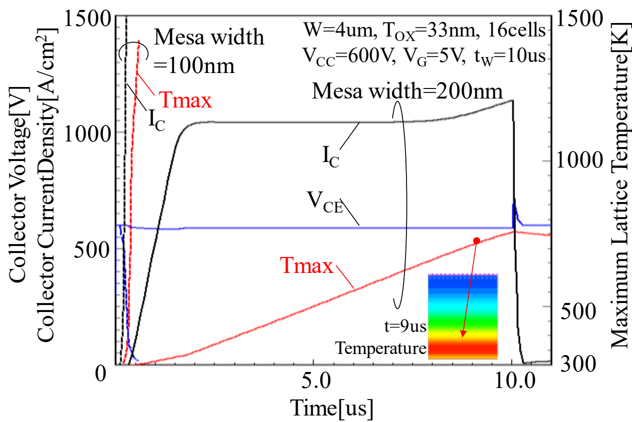
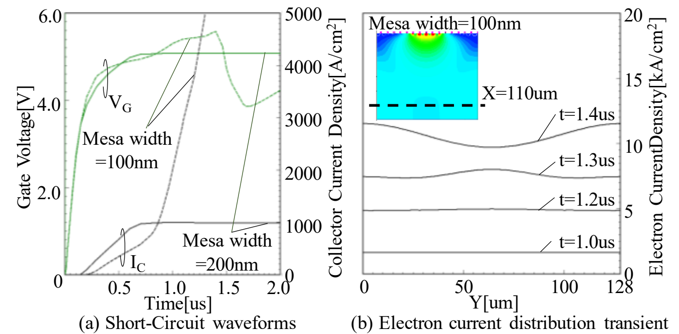


Fig. 12. Short-circuit waveforms for calculated IGBTs. The 200nm mesa width device was successfully turned-off after 10us. In contrast, the 100nm mesa width device failed immediately when the device turned on. The maximum lattice temperature of the 200nm mesa width device was observed in the high electric field region in the N-base.

Fig. 12 compares the short-circuit waveforms of the two IGBTs. In this simulation, completely symmetric 16 cells structure was used and a 0.3cm^{2}K/W of thermal resistance was added on the collector electrode. The 200nm mesa IGBTs successfully turned off after 10us whereas the 100nm IGBT failed immediately when the devices turned on. No current filamentations were observed in the 200nm IGBT during the short-circuit operation. The maximum lattice temperature was observed in the high electric field region in the N-base.

Fig. 13(a) compares the waveforms of the gate voltages and the collector currents of the two IGBTs from t=0us to t=2.0us. The gate voltage of the 100nm mesa IGBT shows an overshoot exceeding 5V, which significantly increases the collector current density throughout the device because of the high transconductance, as seen in Fig.13(b). The device finally latched-up after 1.3us. The large hole current density flowing in the mesa rapidly increases the potential in the P-base and creates the gate voltage overshoot. Fig. 14 shows the transient electron distributions of various time steps in the mesa of the 100nm IGBT. The high electron densities were observed inside the mesa in the center of the device. The simulation results prove that at least 200nm width is required for the mesa to prevent the conductivity modulation in the channel by reducing the neutral P-base resistance.



(a) Short-Circuit waveforms (b) Electron current distribution transient

Fig. 13. (a) Comparison of short-circuit waveforms of 100 and 200nm mesa IGBTs from t=0us to t=2.0us. The gate voltage of the 100nm mesa IGBT shows slight overshoot exceeding 5V. It significantly increases the collector current density of 100nm IGBT. (b) Transient electron current density distributions of the 100nm mesa IGBT at Y=110um. Current density is increased almost uniformly throughout the device before 1.3us. Current filamentation is not the main cause of the present device destruction.

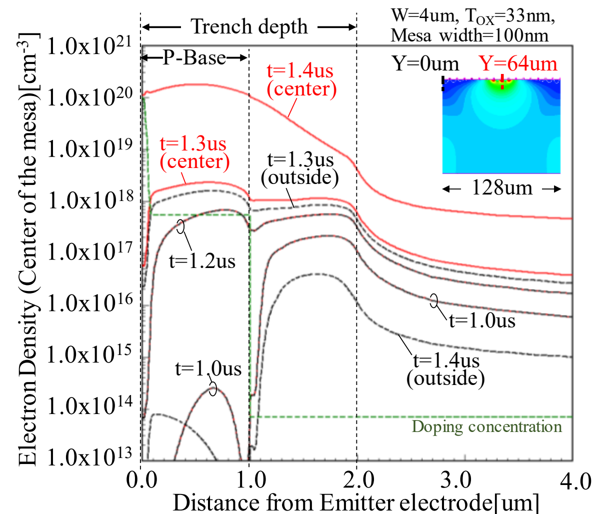


Fig. 14. Transient electron distributions in the mesa region of the 100nm mesa IGBT are plotted along the line of Y=64um (center of the current filament; red lines) and Y=0um (outside the current filament; black dashed lines).

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