

Study of the electrostatic potential of the floating-p region during the turn-on period of IGBT

Yoshihiro Ikura, Yuichi Onozawa

Device Development Department, Fuji Electric, Matsumoto,
Nagano, Japan, e-mail: ikura-yoshihiro@fujielectric.com

Akio Nakagawa

Nakagawa Consulting Office, Chigasaki, Kanagawa, Japan

Abstract— In this work, the influence of the initial electrostatic potential value of the floating-p region, V_{fp} , on the controllability over the turn-on dI_c/dt (Collector current increase rate) is studied using TCAD simulation. To investigate the influence of V_{fp} on the turn-on characteristics, a two-step calculation procedure is used. In the first step, the off state is calculated in which the floating-p region is connected to a fixed voltage source. In the second step, the turn-on characteristics are calculated in which a large resistance is connected between the floating-p region and the voltage source. In this manner, V_{fp} can be fixed at arbitrary value V_{fix} at the beginning of the turn-on period, and, then, becomes floating during the following period. The increase rate of the collector current becomes lower as V_{fix} increases because the high initial V_{fp} accumulates fewer holes in the floating-p region. And the mechanism that determines the initial V_{fp} is also analyzed. A hypothesis is set up that the off-state V_{fp} is equal to the threshold voltage of the P-channel MOSFET which consist of the floating-p, the n-drift, and the p-base region. To confirm the hypothesis, the relation between V_{fp} and major structural components such as the oxide permittivity, the oxide thickness, and the doping concentration are investigated. These results show a good agreement with the theoretical formula of threshold voltage of MOSFET.

Keywords— Insulated gate bipolar transistors, Floating P, Turn on, Controllability, Noise, Transient analysis

I. INTRODUCTION

It is well known that the IGBT with floating-p region has a poor controllability over the turn-on dI_c/dt (Collector current increase rate) [1-3]. Figure 1 is the schematic diagram of how this process occur. As the channel is formed, electrons flow toward the n-drift region. And holes are injected from the Collector to the n-drift region. Holes gather in the floating-p region whose potential is lower than the Collector. The accumulation of holes increases the potential of the floating-p region, V_{fp} . The rapid increase of V_{fp} causes a displacement current, I_{dis} , which flows into the gate electrode. Ideally the gate current, I_g , which would be limited by the gate resistance R_g , should govern the increase rate of the the gate potential. However, actually, the gate electrode facing the floating-p region is charged by I_{dis} which is not limited by R_g . Thus it leads a poor controllability on the turn-on dI_c/dt by R_g .

To overcome this drawback, some group proposed novel device structures which do not have the floating-p region [4, 5]. However, their fabrication process need additional immature processes.

Although this phenomenon is well known, the detail of the mechanism, such as the role of the potential of floating-p

region has not been analyzed yet. In this work, the influence of the initial potential value of V_{fp} on the controllability over the turn-on dI_c/dt is studied using TCAD simulation. And the mechanism that determines the initial V_{fp} is also analyzed.

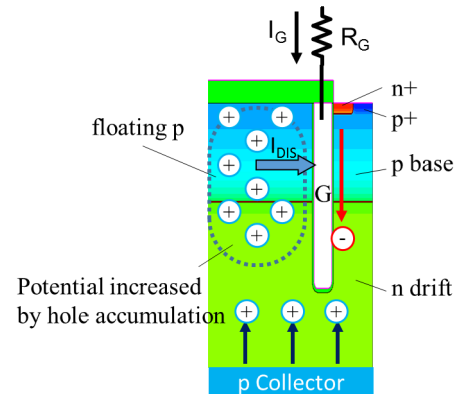


Fig. 1. Cross-section of IGBT with floating p region during turn-on period

II. SIMULATION PROCEDURE

To investigate the influence of V_{fp} on the turn-on characteristics, a two-step calculation procedure is used as shown in Fig. 2. In the first step, the quasi-stationary off-state characteristics are calculated in which the floating-p region is connected to the constant voltage source, V_{fix} . In the second step, the transient turn-on characteristics are calculated in which a large resistance is connected between the V_{fix} and the floating-p region in order to substantially disconnect the floating-p region from V_{fix} . In this manner, the potential of the floating-p region V_{fp} can be fixed at arbitrary value V_{fix} at the beginning of the turn-on period, and, then, becomes floating during the following period.

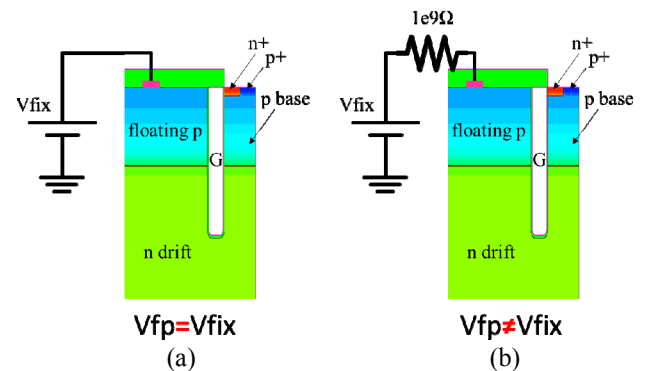


Fig. 2. Simulation procedure to fix the initial V_{fp} to V_{fix} and make it floating during the turn-on period

- a) 1st step; off state with floating p connected to V_{fix}
- b) 2nd step; turn on with floating p disconnected from V_{fix}

III. RESULTS AND DISCUSSIONS

A. Results

Figure 3 shows turn-on waveforms for various V_{fix} . The turn-on waveforms are drastically changed by V_{fix} value. The increase rate of V_{fp} , dV_{fp}/dt , and dI_c/dt becomes lower as V_{fix} value increases. Because the higher initial V_{fp} accumulates fewer holes in the floating-p region, V_{fp} increases less rapidly. The turn-on waveforms of the original IGBT with floating-p region (denoted as “floating” in Fig.3) are equivalent to that of $V_{fix} = 11V$. It is clear that this calculation procedure does not disturb the characteristics except the change of the initial V_{fp} value.

In Fig.4 the blue dotted line shows the relation between dI_c/dt and V_{fix} . And the red solid line shows the dI_c/dt for the IGBT with “non”floating-p region, where the p-region is connected to the Emitter potential. As V_{fp} increases, dI_c/dt decreases and gets close to the value for the IGBT with nonfloating-p region. For example, the dI_c/dt at $V_{fix}=9V$ is twice higher than that at $V_{fix}=11V$. These results indicates that V_{fix} , which is initial value of V_{fp} at the beginning of turun-on period, has a significant influence on the turn-on dI_c/dt .

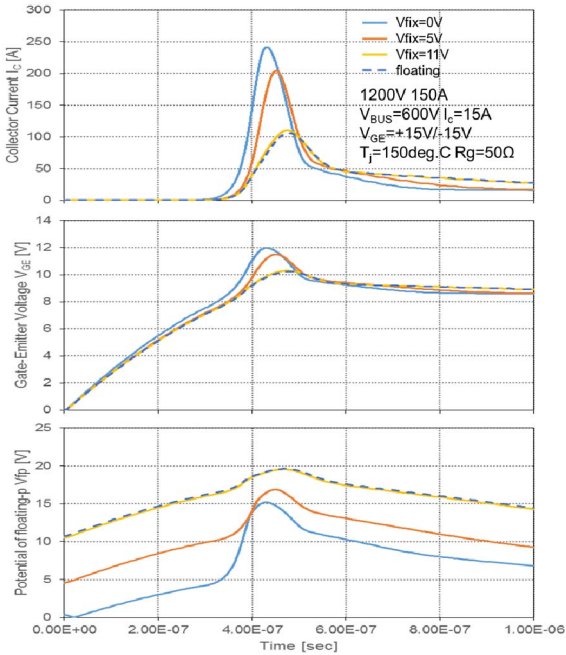


Fig. 3. Simulated turn-on waveforms for arbitrary initial potential of floating-p region, V_{fix}

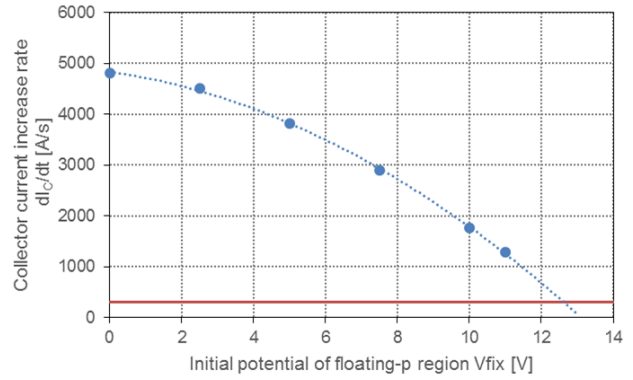


Fig. 4. Simulated dI_c/dt as a function of V_{fix}

B. Mechanism

It is important to reveal how the initial V_{fp} of the “real” floating-p region is determined during the off-state period in order to design IGBT with good turn-on controllability. A hypothesis is set up that the off-state V_{fp} is equal to the threshold voltage of the P-channel MOSFET which consists of the floating-p, the n-drift, and the p-base region (see Fig. 5). Even in the off-state condition, holes come from the Collector as the leakage current and pile up not only in the floating-p region but also in the n-drift region around the trench gate. As the piling-up holes raise the potential in this region, a P-channel layer forms around the trench gate. Since the excess holes flows to the p-base region via the P-channel, V_{fp} does not increase more. In this way V_{fp} takes a certain constant value.

To confirm this hypothesis, the relation between V_{fp} and major structural components such as the oxide permittivity, the oxide thickness, and the doping concentration are investigated.

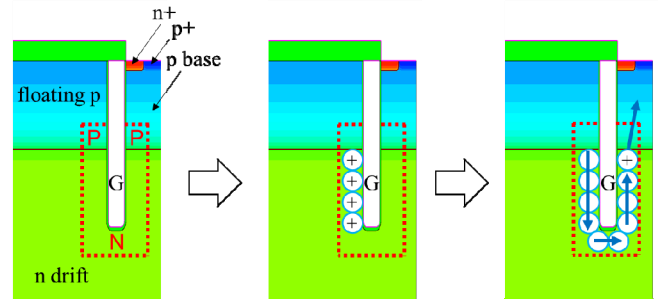


Fig. 5. Hypothetical mechanism which determine the initial potential of floating-p region. The potential rises until the P-channel layer forms around the trench gate.

C. Gate oxide permittivity

First, the initial V_{fp} for various dielectric constant, K , of the gate oxide is investigated. To keep the V_{th} , only K at the bottom of the trench is changed where the V_{th} is highest. As shown in Fig. 6, the initial V_{fp} is linearly dependent on the reciprocal of K . This relation agrees with the formula of the theoretical relation between V_{th} and ϵ_{ox} which can be expressed as

$$V_{th} = \frac{qN_D d \cdot t_{ox}}{K\epsilon_0} + 2\phi_n \quad (1)$$

where V_{th} is the threshold voltage, q is unit electron charge, N_D is donor concentration, d is depletion width, t_{ox} is oxide thickness, ϵ_0 is permittivity of vacuum, ϕ_n is Fermi potential in n-type semiconductor.

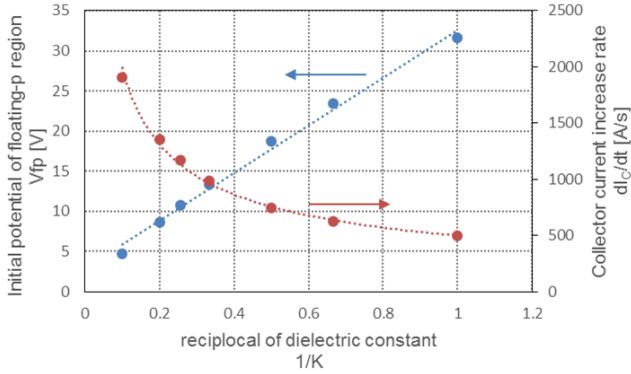


Fig. 6. Simulated Vfp and dIc/dt as a function of 1/K

D. Doping concentration

Second, the initial Vfp for various doping concentration of the n-drift region is investigated. Figure 7 shows the relation between initial Vfp and the doping concentration. The initial Vfp has a linear dependence on the doping concentration that also corresponds to the equation (1).

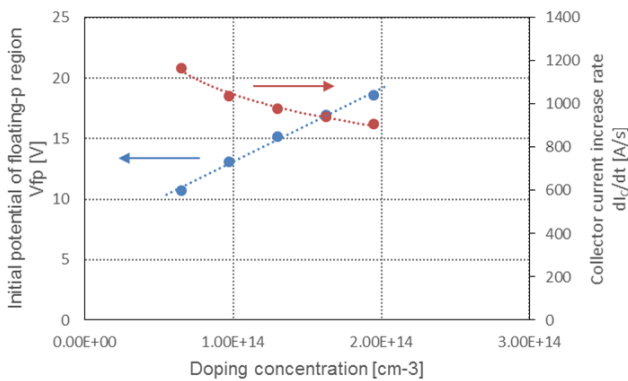


Fig. 7. Simulated Vfp and dIc/dt as a function of doping concentration

E. Gate oxide thickness at the bottom of the trench gate

Last, the initial Vfp for various gate oxide thickness at the bottom of the trench is investigated using the device structure shown in Fig. 8. To keep the V_{th} , only the bottom thickness is changed. The initial Vfp has a linear dependence on the gate oxide thickness that also corresponds to the equation (1) as shown in Fig. 9.

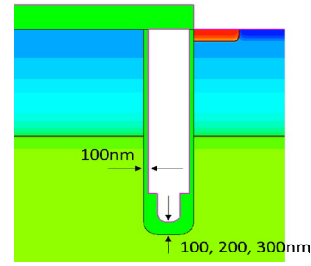


Fig. 8 Cross-section of IGBT with various thickness of bottom gate oxide

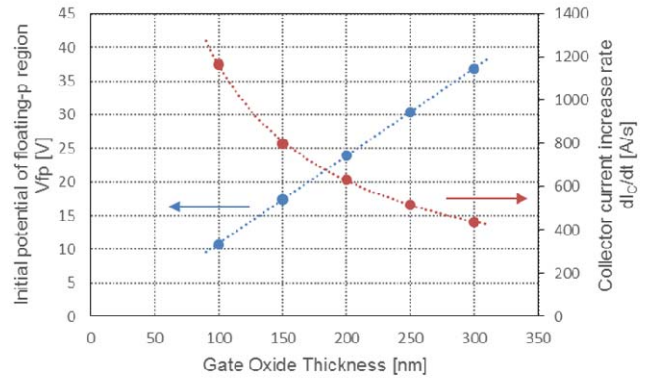


Fig. 9. Simulated Vfp and dIc/dt as a function of bottom gate oxide thickness

It is expected that the IGBT with thicker gate oxide at the bottom of the trench has a better controllability on the turn-on dIc/dt. Figure 10 shows the turn-on waveforms for 100 and 300nm of the gate oxide thickness at the bottom of the trench. The waveform for 100nm shows a rapid increase of the collector current I_c . This rapid increase occurs when the gate voltage suddenly changes the increase rate. As described earlier, this is because the displacement current charge the gate electrode rapidly.

Figure 11 shows the dIc/dt as a function of the gate resistance for different gate oxide thickness at the bottom of the trench. As expected, IGBT with 300nm trench bottom oxide shows a better controllability on the turn-on dIc/dt compared to that of 100nm one.

IV. CONCLUSIONS

In this work, it is shown that the initial potential value of the floating-p region has a significant influence on the controllability over the turn-on dI_c/dt . And the mechanism that determines the potential of the floating-p region, V_{fp} , is also analyzed. A hypothesis is set up that the off-state V_{fp} is equal to the threshold voltage of the P-channel MOSFET which consists of the floating-p, the n-drift, and the p-base region. To confirm the hypothesis, the relation between V_{fp} and major structural components such as the oxide permittivity, the oxide thickness, and the doping concentration are investigated. These results show a good agreement with the theoretical formula of threshold voltage of MOSFET.

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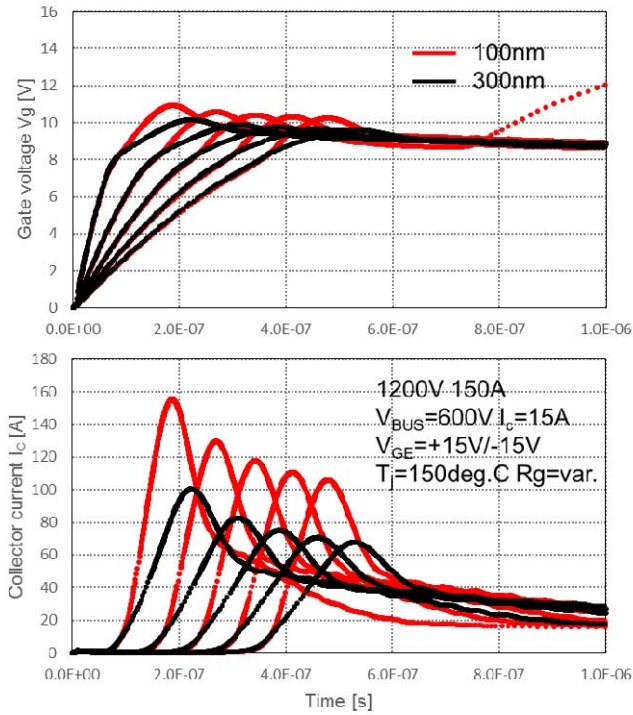


Fig. 10. Simulated turn-on waveforms for different bottom gate oxide thickness

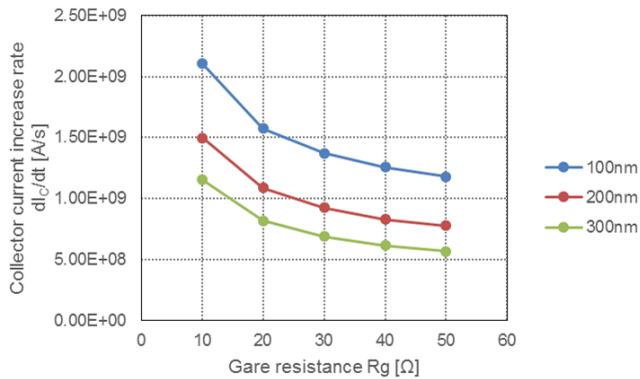


Fig. 11. Simulated dI_c/dt as a function of R_g with different bottom gate oxide thickness