Proceedings of the 2012 24th International Symposium on Power Semiconductor Devices and ICs
3-7 June 2012 - Bruges, Belgium

Carrier-Storage Effect and Extraction-Enhanced Lateral IGBT (E^2LIGBT): A Super-High Speed and Low On-state Voltage LIGBT Superior to LDMOSFET

Shigeki Takahashi[(1)], Akio Nakagawa[(2)], Youichi Ashida[(1)], Satoshi Shiraki[(1)], and Norihito Tokura [(1)]

[(1)]DENSO Co., Ltd
Kota-cho, Nukata-gun, Aichi 444-0193, Japan
SHIGEKI_TAKAHASHI@denso.co.jp

[(2)]Nakagawa Consulting Office
Chigasaki, Kanagawa 253-0021, Japan

***Abstract*— We have successfully developed novel extraction enhanced lateral insulated gate bipolar transistors (E^2LIGBTs), which exhibit super-high speed switching of 34 ns turn-off time and a low on-state voltage of 3.7 V at 84 A/cm^2 simultaneously with a high breakdown voltage of 738V. For the first time, E^2LIGBTs have exceeded the counterpart lateral DMOS both in switching speed and in on-resistance. The superior performance is achieved by the novel anode structure consisting of a narrow p^+-injector and a wide Schottky contact on a lightly doped p-layer over an n-buffer. The on-state voltage can be further reduced to 3.0V at 84 A/cm^2 by introducing Carrier Storage (CS) layer. The developed E^2LIGBTs achieved the best trade-off between on-resistance and switching speed among all the lateral MOS power devices, so far reported.**

I. INTRODUCTION

Lateral IGBTs (LIGBTs) are one of the key components for SOI single chip inverter ICs, because their characteristics strongly affect the inverter performance. 600V single chip inverter ICs are planned to be introduced in future HEV/EV vehicles to improve the system efficiency, replacing the existing 12V systems with high voltage systems[1].

Nakagawa et al. developed SOI-LIGBT with a lightly doped p-layer collector, resulting in fall-time t_F=300ns, on-state voltage V_{ON}=3.0V (120A/cm^2), and breakdown voltage BV_{CES}=500V [2, 3]. Kaneko et al. developed junction-isolated hybrid IGBT with employing anode short and electron irradiation, resulting in turn-off time t_{OFF}=110ns, V_{ON}=5.5V (68A/cm^2), and BV_{CES}=800V [4]. Sin et al. developed HSINFET, where the anode consists of p^+ emitter and Schottky contact on the n-drift, resulting in t_{OFF}=50ns, R_{ON}=7ohm, and BV_{CES}=130V [5]. However, all the devices, thus far reported, were still slower in switching speed than lateral DMOS(LDMOS), although their on-resistances were lower than that of LDMOS.

II. ANODE STRUCTURE FOR HIGH SPEED SWITCHING

We propose a novel anode structure, a combination of the p^+-injector and the wide Schottky contact on the lightly doped p-layer over the n-buffer, as shown in Fig. 1. Electrons and holes are injected from the channel and from the p^+-injector (S_I), resulting in conductivity modulation. The wide Schottky contact (S_E) extracts a large portion of electrons, flowing under the Schottky contact. It was found that the conductivity modulation, and thus, the turn-off time, t_{OFF}, can be controlled by the area ratio of the Schottky area over the p^+-injector area , S_E/S_I, as shown in Fig.2. Both a low V_{ON} and a short t_{OFF} can be achieved by designing an adequate area ratio, S_E/S_I. We found, for the first time, that the Schottky contact on the lightly doped p-layer is better than the Schottky contact directly on the n^--drift or the n-buffer. The Schottky contact directly on the n^--drift too much suppresses the hole injection from the p^+-injector, and forces a high forward voltage [6].

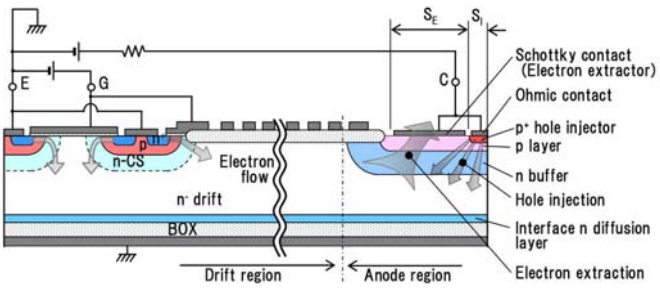


Figure 1. Schematic cross-section of E^2LIGBT with/without CS in SOI with interface n-diffusion-layer. Novel anode structure, a combination of p^+-injector and wide Schottky contact on lightly doped p-layer over n-buffer and CS layer is illustrated.

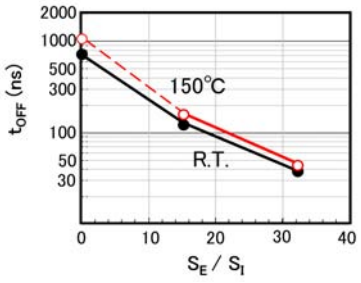


Figure 2. Measured turn-off time, t_{OFF}, of E^2LIGBT with CS as a function of S_E/S_I. t_{OFF} is determined by the area ratio, S_E/S_I.

An interface n-diffusion-layer(INL) with the dose of $1.05x10^{12}$/cm^2 was formed on the BOX, if not specified in the present paper, in order to increase the breakdown voltage [7]. The highest Breakdown voltage 780V was experimentally obtained for the INL dose of $1.7x10^{12}$/cm^2. If INL is not used, a thick BOX of 8μm is required to realize the same breakdown voltage, as shown in Fig.3.

Carrier storage layer(CS) was introduced under the emitter p-well region, as shown in Fig.1. CS layer not only increases the carrier density under the p-well but also enhances the channel current flowing from the inner channel, thus, reducing the forward voltage[8].

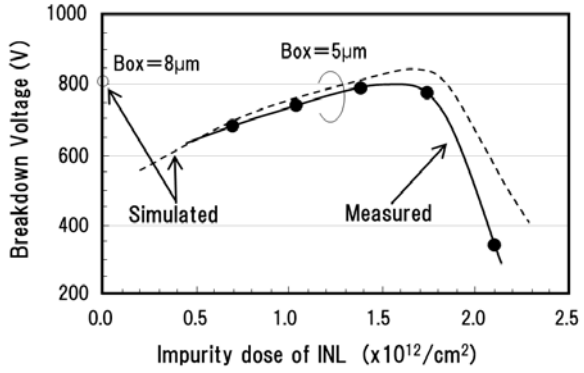


Figure 3. Breakdown voltage of SOI lateral device as a function of impurity dose of INL. The highest breakdown voltage 780V was experimentally obtained for INL dose of $1.7x10^{12}/cm^2$.

III. EXPERIMENTAL RESULTS

E^2LIGBTs with/without CS were fabricated in SOI wafer of 15μm thick silicon and 5μm BOX, using 0.6μm BiCD process. LDMOS were also fabricated in the same SOI wafer for comparison. Fig. 4 shows the photos of fabricated E^2LIGBT and LDMOS, respectively. The area of E^2LIGBT is $0.24mm^2$. LDMOS consists of 36 cells and the total device active area is $1.9mm^2$, which is 7.9 times larger than that of the E^2LIGBT.

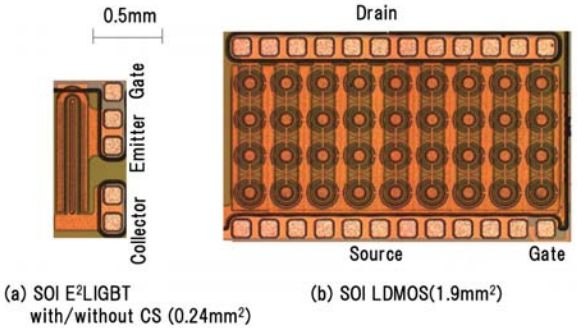


Figure 4. Micrographs of the fabricated devices. The area of E^2LIGBT with/without CS is $0.24mm^2$. LDMOS consists of 36 cells and the total device active area is $1.9mm^2$.

High blocking voltage of 738V for E^2LIGBT with/without CS and 731V for LDMOS were achieved as seen in Fig. 5(a). S_E/S_I ratio was set at 33. The measured V_{ON} of E^2LIGBT with CS dose of $1x10^{13}/cm^2$ was 3.0V at 200mA ($84A/cm^2$), whereas V_{ON} of E^2LIGBT without CS was 3.7V, as seen in Fig. 5(b). CS layer successfully reduced the V_{ON} by 0.7V.

Fig. 7 compares the measured turn-off waveforms for E^2LIGBTs with/without CS and LDMOS when S_E/S_I=33. The measured t_{OFF} are 34ns for E^2LIGBT without CS and 38ns for E^2LIGBT with CS, respectively. These are considerably shorter than 44ns of LDMOS. Fig. 8 compares the temperature dependence of E^2LIGBT with CS and LDMOS regarding (a) t_{OFF}, (b) turn-off energy loss, E_{OFF}, and (c) V_{ON}. The temperature dependence of E^2LIGBT without CS is reported in [6]. The turn-off energy loss, E_{OFF} of E^2LIGBT with/without CS hardly depends on temperature, and is remarkably smaller than that of LDMOS. The temperature dependence of V_{ON} of E^2LIGBT is far better than that of LDMOS.

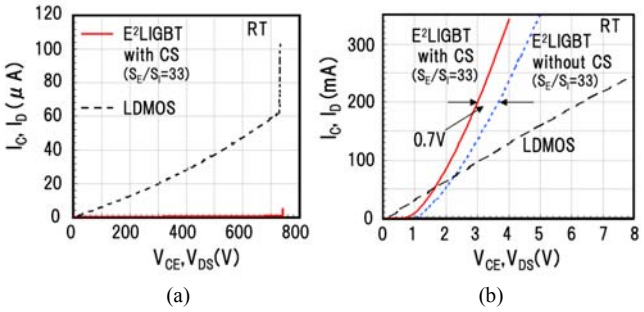


Figure 5. Measured (a)breakdown characteristics and (b)I-V characteristics.

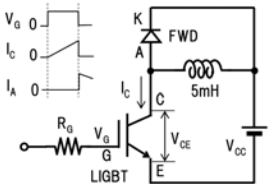


Figure 6. Measurement circuit for turn-off operation

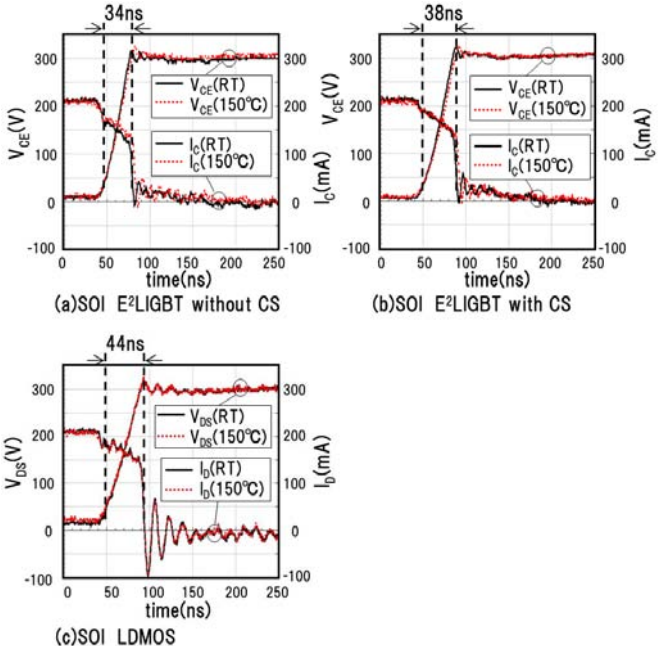
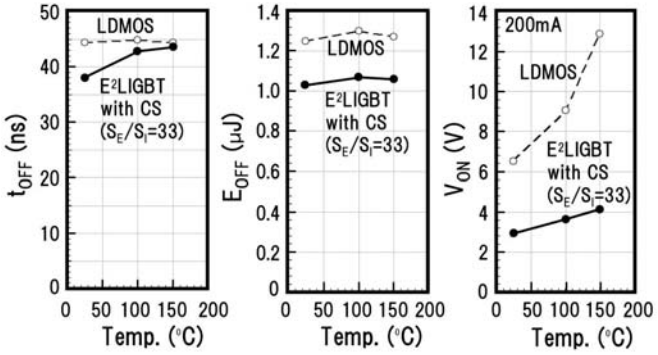


Figure 7. Measured turn-off waveforms under inductive load for E^2LIGBTs with/without CS and LDMOS.

Fig. 9 compares the trade-off relation between the current density for V_{ON}=3V and the turn-off time among the high voltage lateral MOS power devices in conventional SOI wafers, so far reported. It is clear that the trade-off of E^2LIGBT with CS is the best among all the devices, including lateral DMOS and E^2LIGBT without CS. CS layer increased the operation current density by 30%, compared with E^2LIGBTs without CS.



(a) t_{OFF} vs. temp (b) E_{OFF} vs. temp (c) V_{ON} vs. temp

Figure 8. Measured temperature dependence of turn-off time(t_{OFF}), turn-off energy loss(E_{OFF}) and on-state voltage(V_{ON}).

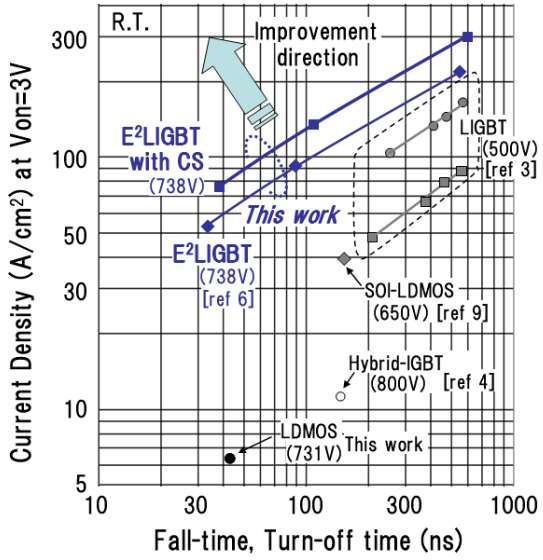


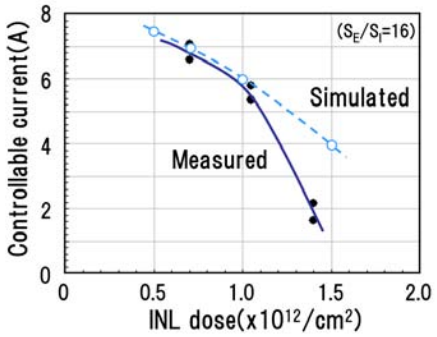
Figure 9. Trade-off relation between current density of V_{ON}=3V and turn-off time. Vertical axis shows the current density when V_{ON}=3V. E^2LIGBT with CS achieved the best trade-off among all the reported lateral MOS power devices in conventional SOI wafers.

IV. RBSOA OF LARGE AREA E^2LIGBTS

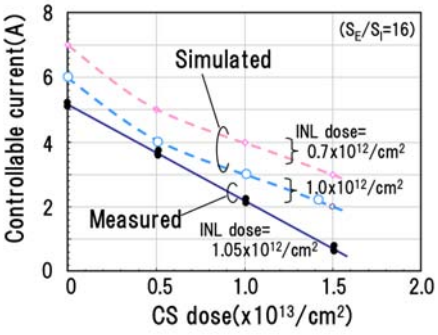
RBSOA of the large area E^2LIGBT (14 cells, area of 2.65mm^2) was investigated under an inductive load with 450V DC power supply. S_E/S_I ratio was set at 16 for the application of inverter ICs. The maximum controllable current, I_{CMAX}, of 7A was obtained at 150°C for E^2IGBT without CS. I_{CMAX} depended on INL dose as well as CS dose as shown in Fig. 10.

In order to clarify the mechanism of the device failure, device simulations were performed. Fig. 11 shows the simulated turn-off waveforms of E^2LIGBT with CS under an inductive load. The electron and hole current components at the emitter electrode are plotted together with the total current in Fig. 11. The electron current component decreased as the gate voltage decreased. It was found that the electron current decreasing rate was relaxed at the time step t_1. This was brought about because the so called "latch-up" phenomena started to occur. Fig. 12 shows the close-up view of the simulated impact ionization rate around the emitter region of E^2LIGBT with CS at the time t_1. The high impact ionization induced a large hole current flowing under the N^+ emitter, and created a voltage drop of more than 0.8V in the p-well, activating the parasitic bipolar action as seen in Fig. 13. This may result in localized latch-up in actual devices. It was found that the reduction in the total donor dose (CS or INL dose) under the p-well reduced the peak electric field and increased the controllable current. The simulation results revealed that the RBSOA locus is determined by the latch-up phenomena.

A good design optimization was found by simulations. In Fig.14, one of the optimized E^2LIGBT is shown as structure B where INL is formed only under the collector region. This structure effectively suppresses the electric field at the CS layer and shows high controllable current.



(a) Controllable current decreased as interface n-layer(INL) dose increased. Simulation results successfully reproduced the same tendency.



(b) Controllable current decreased as CS dose and INL dose increased. Simulation results agreed well with experiments.

Figure 10. Measured and simulated RBSOA of large area E^2LIGBTs with CS at 150°C as a function of INL and CS dose. S_E/S_I was set at 16.

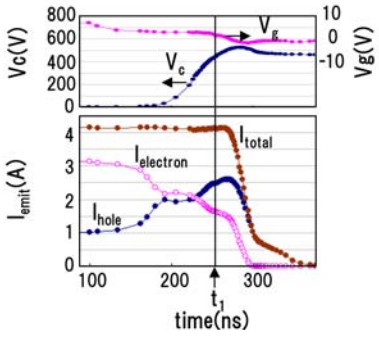


Figure 11. Simulated turn-off waveform of E^2LIGBT with CS under inductive load. Turn-off current was set at 4A. Electron current decrease rate is relaxed at time t_1.

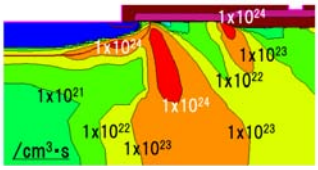


Figure 12. Close-up view of the simulated impact ionization rate contour of the emitter region for E^2LIGBT with CS at time t_1.

(a) Electrostatic potential (b) Electron current density

Figure 13. Close-up views of the simulated (a) electrostatic potential and (b) electron current density distributions for E^2LIGBT with CS at time t_1. Large hole current, created by impact ionization, flows under the N+ emitter and creates potential drop of more than 0.8V in the p-well under the N+ emitter layer, resulting in npn parasitic bipolar transistor action. In Fig.(b), electron current flows outside the channel, showing initiation of latch-up.

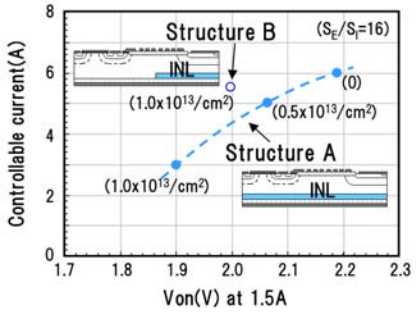


Figure 14. Simulated trade-off relation between on-state voltage at 1.5A and controllable current. Parenthesis shows CS dose. In structure B, INL is formed only under the collector layer. This structure shows improved controllable current, maintaining high breakdown voltage and low on-state voltage. INL dose was set at $1.0x10^{12}/cm^2$.

V. AUTOMOTIVE APPLICATION

Hybrid/Electric Vehicles are equipped with high voltage batteries ranging from 100V to 430V [10]. Automotive small power electronics such as blower fan motors are operated at 12V, so step down DC-DC converters are used. These conversion losses affect vehicle efficiency. To reduce these losses, it is effective to drive motors directly from high voltage battery.

600V single chip inverter ICs were developed with E^2LIGBT without CS for this purpose, as shown in Fig. 15. The IC drives 250W blower fan motors for air circulation and achieved 10% efficiency increase, compared to conventional 12V systems which utilizes 60V high current power MOSFETs.

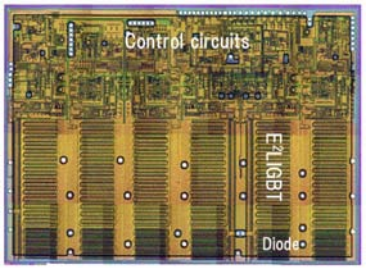


Figure 15. Photo of the fabricated 600V 4.5A SOI single chip inverter IC (6.2mm x 9.3mm).

ACKNOWLEDGMENT

The authors would like to thank Koji Senda and Takeshi Sakai for sample preparation, Shogo Ikeura for measurement, Hisato Kato and Shunsuke Harada for TCAD simulation. The authors also thank A. Yamada, Y. Tanaka, Y. Nakayama, and N. Iwamori, for their support throughout this study.

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