ESD protection structure with novel trigger technique for LDMOS based on BiCD process

Kazutoshi Nakamura, Toshiyuki Naka, Ken'ichi Matsushita, Tomoko Matsudai, Norio Yasuhara and Akio Nakagawa

Discrete Semiconductor Division, Toshiba Corporation Semiconductor Company
1,Komukai Toshiba-cho,Saiwai-ku,Kawasaki,212-8583,Japan
Phone:+81-44-549-2674,facsimile:+81-44-549-2877, E-mail:kazutoshi.nakamura@toshiba.co.jp

Abstract— This paper presents ESD protection structure with novel trigger technique for LDMOS based on BiCD process. The proposed ESD protection element includes the same structure as drain region in Nch-LDMOS, the vertical NPN transistor and the lateral NPN transistor. The trigger voltage is depended on the breakdown voltage in the drain region integrated in ESD protection device and the avalanche current acts as the base current of NPN transistor. The high ESD current spreads to the buried layer in the vertical NPN transistor without locally concentrating in the drain edge. The value of the second breakdown trigger current It2 in the proposed ESD protection element is nearly four times as large as that in the simple LDMOS.

I. INTRODUCTION

Lateral DMOS (LDMOS) power devices are widely used as output drivers in multiple applications in smart power IC designs. Relative to their sizes, LDMOS transistors are inherently weak with respect to ESD reliability and ESD ruggedness of LDMOS power devices has been a significant subject in smart power IC designs.

The LDMOS applied to the switching regulator has the drift layer with shallow junction depth due to the self-aligned process between the gate electrode and the drift layer. While the structure enables the high speed switching because of the small gate-drain capacitance, the drain current is likely to concentrate in the drain edge during an ESD event, resulting in a filamentation. ESD protection elements are required to withstand the surge current in parallel with the LDMOS. The some approaches based on Silicon Controlled Rectifier (SCR) have been proposed due to the high discharge capability derived by hole and electron injection conductivity modulation [1, 2]. There is a possibility that the SCR is triggered by unwanted serge voltage and latch-up stimuli may occur during normal operation. While the emitter-base shorted bipolar transistor as shown in figure.1 is effective, the trigger voltage and current is depended on the device parameter such as the length (L_{b-c}) between the base diffusion layer and collector layer [3].

The margin voltage between the snapback voltage Vt1 of the LDMOS and that of the ESD protection element has tended to widen considering the process fluctuation for the two devices because each breakdown voltage is determined by the different device parameters.

In this paper, we propose an ESD protection structure with novel trigger technique for LDMOS based on BiCD process.

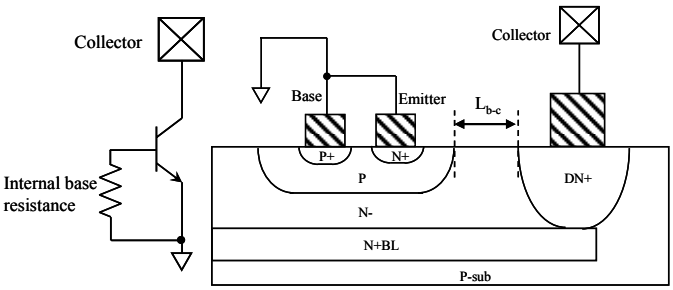


Figure.1 Electrical schematic and cross section of the emitter-base shorted bipolar transistor.

II. DEVICE STRUCTURES

A. Nch LDMOS

Figure 2 shows a cross-sectional view of Nch-LDMOS for switching regulator based on the low cost 0.6um BiCD process. The device is fabricated in the p-well so that the gate drain capacitance is minimized. The drift region is self-aligned to the gate electrode in order to reduce the parasitic gate-drain capacitance which affects the switching loss. The on-state breakdown voltage degrades as the drain current increases because the net effective positive charge is reduced by the existence of a large amount of negative electron charges in the Ndrift1 layer. The on-state breakdown tends to decrease as the junction depth of the drift layer is shallower. We have applied

978-1-4244-4673-5/09/$25.00 ©2009 IEEE.

2-step shallow n-implant structure (Adaptive Resurf) to the N-ch LDMOS. The breakdown voltage is 37V.

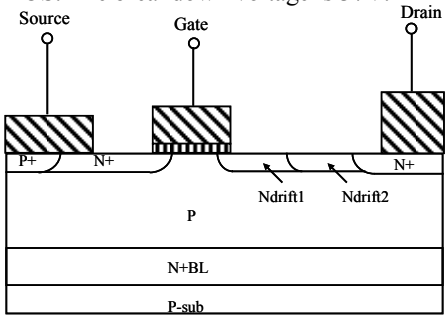


Figure.2 Cross-sectional view of Nch-LDMOS for switching regulator based on the low cost 0.6um BiCD process

Figure 3 shows the snapback TLP-IV characteristics of Nch-LDMOS. The LDMOS devices failed after the first snapback turn-on. Figure 4 (a)(b) shows the simulated current distribution and temperature distribution of LDMOS in injecting the high current into the drain electrode. The drain current concentrates in the drain edge and the kirk effect appearing in the high current bipolar mode pushes the avalanching region from the second drift layer Ndrift2 edge to the highly doped N+ diffusion region. High current and high electric field causes the physical destruction at the N+ region.

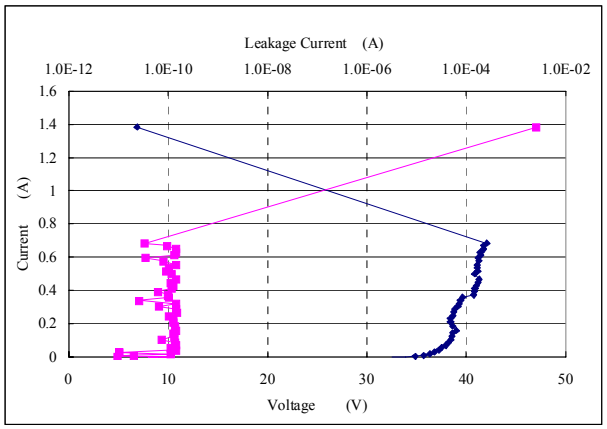
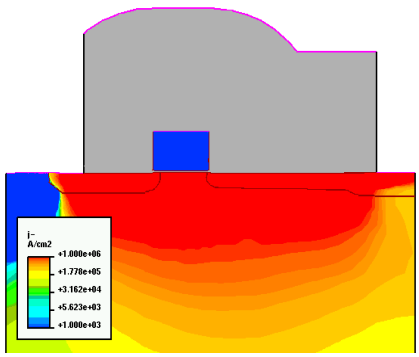
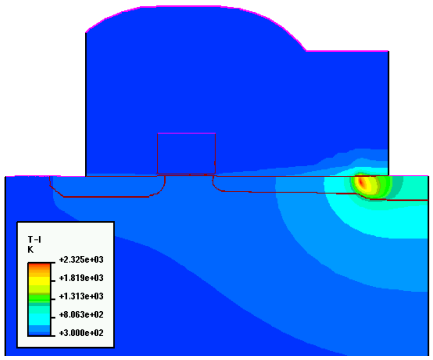


Figure.3 Snapback TLP-IV characteristics of Nch-LDMOS. The LDMOS devices failed after the first snapback turn-on.



(a) Current distribution



(b)Temperature distribution

Figure.4 Simulated current distribution and temperature distribution of LDMOS in injecting the high current into the drain electrode

B. Proposed ESD protection structure with novel trigger technique

Figure 5 shows the proposed ESD protection structure with novel trigger technique. The proposed ESD protection element includes the same structure as drain region in Nch-LDMOS, the vertical NPN Tr1 and the lateral NPN Tr2. The breakdown voltage is depended on the peak electric filed in first drift layer Ndrift1 between the gate and the highly doped N+ diffusion region and the avalanche current acts as the base current of the lateral NPN Tr2. The Vt1 trigger voltage of the protection device is controlled by the drift length and the margin voltage between the snapback voltage Vt1 of the LDMOS and that of the ESD protection element can be reduced. When the avalanche current creates a voltage drop of 0.7V over the parasitic resistance in the base layer, the lateral NPN Tr2 will be turned on. As the resistance R1 is connected to the collector of NPN Tr2 and the flowing current is limited, the vertical NPN Tr1 will be turned on in region of the higher ESD current. The high ESD current flows through the N+ buried layer N+BL. Then the ESD current spreads to the buried layer without locally concentrating in the drain edge. The high ESD ruggedness is achieved by the relaxation of the kirk effect and the current crowding effect.

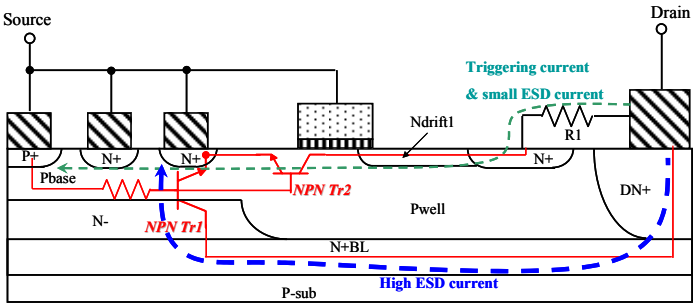
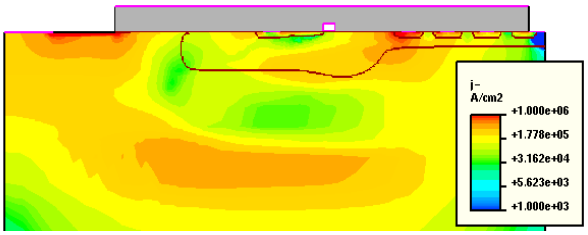
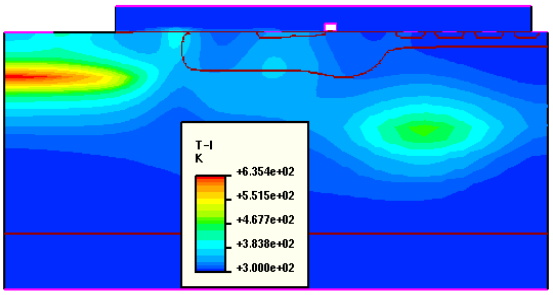


Figure.5 Proposed ESD protection structure with novel trigger technique. The proposed ESD protection element includes the same structure as drain region in Nch-LDMOS, the vertical NPN Tr1 and the lateral NPN Tr2.

Figure 6 shows simulated current distribution and temperature distribution of the proposed ESD protection element in injecting the high current into the drain electrode. The ESD current spreads to the buried layer without locally concentrating in the drain edge and the hot spot is widely distributed in the deep N+ layer DN+ connecting the drain electrode with the N+BL.



(a)current distribution



(b)temperature distribution

Figure.6 Simulated current distribution and temperature distribution of the proposed ESD element in injecting the high current into the drain electrode.

III. EXPERIMENTAL RESULTS

Figure 7 shows the snapback TLP-IV characteristics of the proposed ESD protection element. Both the breakdown voltage and the Vt1 trigger voltage is 33V. The lateral NPN Tr2 is turned on when the voltage between the drain and the source electrode is over the avalanche breakdown voltage. When the drain current is higher than 0.7A, the vertical NPN Tr1 is turned on and the on resistance is lower than that of the lateral NPN Tr2. The It2 value of the proposed ESD protection element is nearly four times as large as that of the simple LDMOS.

Figure 8 and 9 show the ESD protection structure with the adaptive resurf in the drain region of triggering LDMOS and the snapback TLP-IV characteristics, respectively. The breakdown voltage and the trigger voltage Vt1 in this device are 25V and 28V, respectively. The difference between the trigger voltage Vt1 and the onset voltage of the low resistive mode is larger compared with the ESD protection structure without the second drift layer Ndrift2 in the drain region of triggering LDMOS. This is why the adaptive resurf reduces the electric field in the region of high drain current and high drain voltage and suppresses the avalanche current for the trigger current of the NPN Tr1. In order to protect the LDMOS against the ESD surges, the breakdown voltage in LDMOS is higher than the trigger voltage Vt1 in the ESD protection element. The difference between the breakdown voltage in LDMOS and the Vt1 in the ESD protection element must be small. Because the rated voltage is determined by the Vt1 in ESD protection element and the on resistance is increased with increasing the breakdown voltage in LDMOS. If the trigger voltage Vt1 in the ESD protection structure with the adaptive resurf is brought close to the breakdown voltage in LDMOS, the onset voltage of the activated vertical NPN Tr1 is higher than the breakdown voltage in LDMOS and the vertical NPN transistor can't be turned on. Consequently, the capability to discharge the surge current in this ESD protection element isn't insufficient.

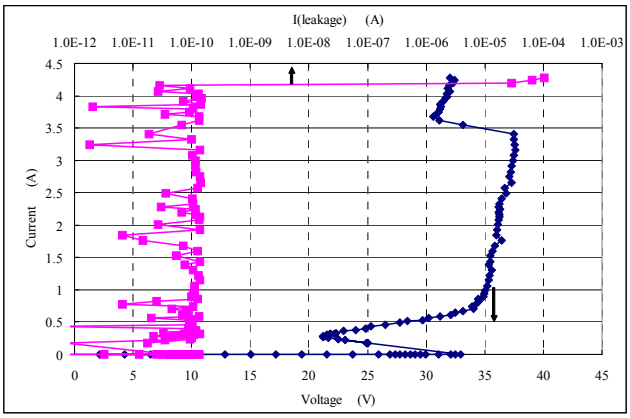


Figure.7 Snapback TLP-IV characteristics of the proposed ESD element. Both the breakdown voltage and the Vt1 trigger voltage is 33V.

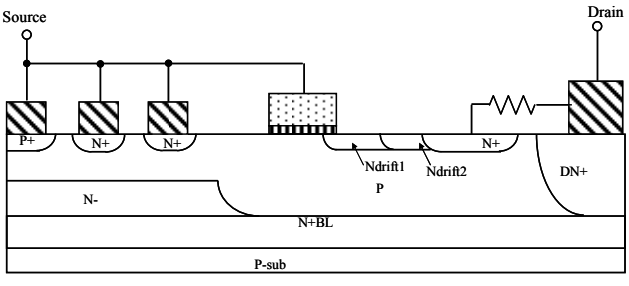


Figure.8 ESD protection structure with the adaptive resurf (Ndrift2 layer) in the drain region of triggering LDMOS

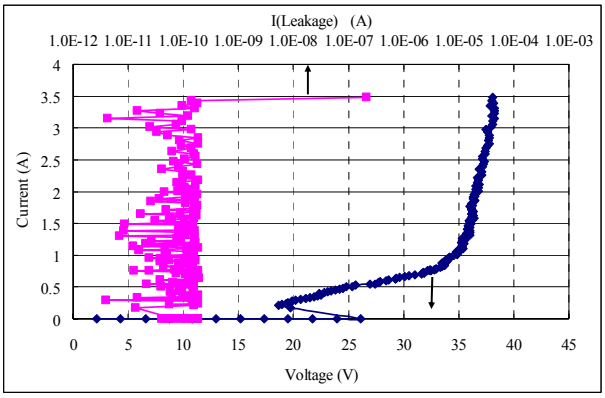


Figure.9 Snapback TLP-IV characteristics of ESD protection structure with the adaptive resurf (Ndrift2 layer) in the drain region of triggering LDMOS

Figure 10 shows the comparison of the snapback TLP-IV characteristics with small and large R1 resistance connected to the drain. The It2 value of the structure with large R1 is nearly twice as large as that with small R1. The structure with small R1 failed before the vertical NPN Tr1 turned on. The R1 resistance acts as the ballast resistance. Both the element device and the R1 need to be larger for the lateral NPN Tr2 to discharge the higher ESD current. From the viewpoint of the ESD protection element size, it is important to activate NPN Tr1 in region of high ESD current.

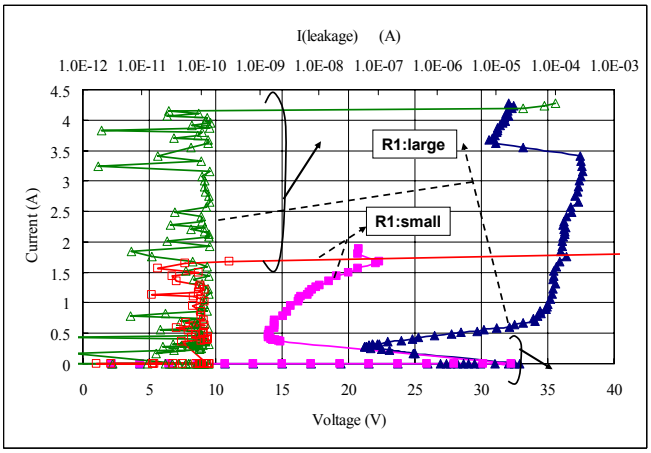


Figure.10 Comparison of the snapback TLP-IV characteristics with small and large R1 resistance connected to the drain.

IV. CONCLUSION

This paper presented ESD protection structure with novel trigger technique for LDMOS based on BiCD process. The proposed ESD protection element includes the same structure as drain region in Nch-LDMOS, the vertical NPN transistor and the lateral NPN transistor. The trigger voltage is depended on the breakdown voltage in the drain region integrated in ESD protection device and the avalanche current acts as the base current of NPN transistor. We demonstrated an ability to discharge the high ESD current in the proposed ESD protection structure. The It2 value of the proposed ESD protection element is nearly four times as large as that of the simple LDMOS.

ACKNOWLEDGMENT

The authors would like to thank Mr. K.Morizuka, Mr. Y.Aizawa, Mr.T.Tsurugai and Mr. M.Yamaguchi for providing the opportunity of this study and Mr. Y.Suzuki and Mr. K.Endo for assisting the experimental manufacture.

REFERENCES

[1] V.A. Vashchenko, D. Farrenkopf and P. Hopper, "ACTIVE CONTROL OF THE TRIGGERING CHARACTERISTICS OF NPN BJT, BSCR AND NLDMOS-SCR DEVICES," *ISPSD'07*, pp.41-44

[2] S.Pendharkar, R.Teggatz, J.Devore, J.Carpenter, T.Efland, C.Tsai "SCR-LDMOS-A NOVEL LDMOS DEVICE WITH ESD ROBUSTNESS," *ISPSD'00*, pp. 341-344

[3] G Bertrand, C.Delage, M.Bafleur, N.Nolhier, J.M.Dorkel, Q.Nguyen, N.Mauran, P.Perdu,"Analysis and Compact Modeling of a Vertical Grounded-Base NPN Bipolar Transistor used as an ESD Protection in a Smart Power Technology," *BCTM'00,*pp.28-31