Demonstration of high frequency and 10A operation in 12V 1 chip DC/DC converter IC using bump technology

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Abstract- **This paper presents 12V 10A 1chip DC/DC converter IC based on the low cost 0.6um BiCD process. The chip adopted low impedance metal bump technology and a high speed gate driving technique for large LDMOS, what we call "distributed driver circuit". The fabricated chip achieves that the on resistance of 20V output LDMOS is 9.7mΩ(@drain current=5A, gate voltage=5V) and the maximum efficiency is 88.9% at output current 5A when the input voltage, the output voltage and switching frequency is 12V, 1.3V and 780KHz, respectively.**

I. INTRODUCTION

With recent increase in clock speed of microprocessors, high efficiency, high power density, high current slew rate di/dt is strongly demanded for DC/DC converters. Precise voltage regulation under a large di/dt requires high switching frequency.

In order to improve the conversion efficiency at high switching frequency, not only the device structure of switching MOSFET but also the circuit parameters such as parasitic devices on board must be optimized. It has been pointed out that the parasitic inductance between the output MOSFET and the gate driver circuit decreases the conversion efficiency. Multi Chip Module or 1 chip solution are effective to reduce the parasitic wiring inductances [1,2]. It was also predicted that a low impedance gate drive can reduce the mirror period in the turn-off transient, realizing ideal switching and low turn-off power loss [3]. The achievable minimum turn-off power loss is just the main junction charge/discharge loss and is determined by the new FOM proposed in Ref.[3,5]. 1 chip solution is favorable for achieving the ideal switching because the parasitic inductances are small and sufficiently low impedance gate driver circuits are easily integrated with power MOSFETs.

Up to now, the output current of 1 chip converter has been limited to a few or several amperes because of the following two issues. (1)The interconnection resistance becomes larger and even exceeds the on-resistance of the device itself if the size of LDMOS increases. (2)It is difficult to uniformly turn-on and -off the large size LDMOS in short switching period.

In this paper, we demonstrate 10A operation and high speed switching in on-chip converter by applying a metal interconnection with bump technology and adopting distributed low impedance gate driver circuits.

II. DEVICE STRUCTURES

Figure 1 shows a cross-sectional view of 20V output LDMOS devices based on the low cost 0.6um BiCD process. The device is fabricated in the p-well so that gate drain capacitance is minimized. The buried N+ layer is electrically connected to the source electrode to reduce the coupling between the drain and the substrate. Three metal layers with a 3um thick top metal layer are utilized. The drift region is self-aligned to the gate electrode in order to reduce the parasitic gate-drain capacitance which affects the switching loss. Additionally, the source electrode extended over the gate poly-silicon is effective to reduce the parasitic gate-drain capacitance. In case of the optimized Nch LDMOS, the breakdown voltage, the threshold voltage and the specific on-resistance is 25.0V, 0.85V and 23.1mΩmm^2, respectively.

III. POWER IC USING BUMP TECHNOLOGY

The on resistance of lateral MOSFETs with wire bonding deteriorates considerably with increase in device size due to the parasitic resistance. Interconnection resistance not only increases overall device resistance but also causes debiasing effect in active cells [6]. In order to reduce the interconnection resistance, we have adopted wafer bumping technology [7].
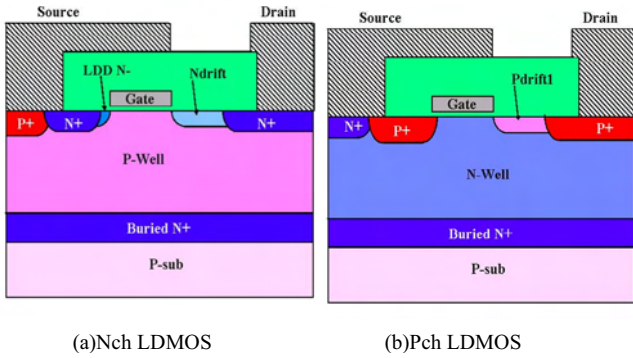
(a)Nch LDMOS   (b)Pch LDMOS

Figure.1 Cross-sectional view of 20V output power devices based on the low cost 0.6um BiCD process.

Figure 2 shows the assembled image, the layout of the top metal in IC and the Cu pattern on a printed circuit board (PCB). The chip is attached to the intermediate PCB through bump balls.

We have adopted Pch LDMOS for high side switching device in DC/DC converter. The source and drain metals are alternately formed and the drain metals of Pch LDMOS and Nch LDMOS are connected each other. The PCB connects drain and source bumps by parallel running thick Cu metals. The resistance that current laterally flows in the top metal is made as small as possible.
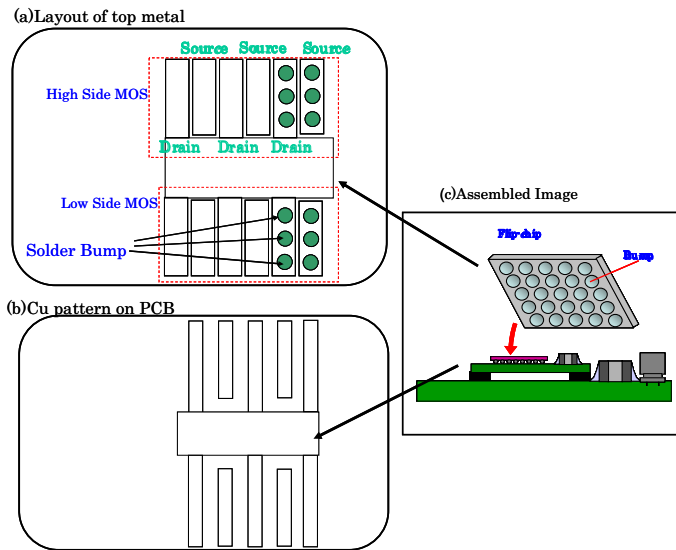

Figure.2 Assembled image, layout of top metal in IC and Cu pattern on printed circuit board (PCB). The drain and the source bumps are electrically connected by parallel running thick Cu metals in the PCB

IV. DISTRIBUTED DRIVER CIRCUIT LAYOUT

When the area of LDMOS is large, the gate current between driver circuit and LDMOS becomes increasingly large. The whole LDMOS device doesn't uniformly turn on or off because the gate drive delay may occur within the large LDMOS. In case of on-chip DC/DC converter, the parasitic resistance and capacitance of the gate interconnection affects gate signal delay. Especially in turn-off period, the gate delay may cause significant non-uniform switching because of the small threshold voltage (0.85V). Thus, we have proposed "distributed driver circuit layout."[4]

Figure 3 shows the comparison of the distributed driver circuit layout with the conventional concentrated driver circuit layout. In the concentrated driver circuit layout (a), the large gate charging or discharging current flows from one large driver circuit and the parasitic resistance of signal bus line causes non-uniform gate voltage distribution. In the distributed driver circuit layout (b), a number of driver circuits are formed along a long side of the LDMOS and the length that large gate charging or discharging current flow path is made as short as possible. The current magnitude of the signal bus line is small, and does not cause the gate signal delay.
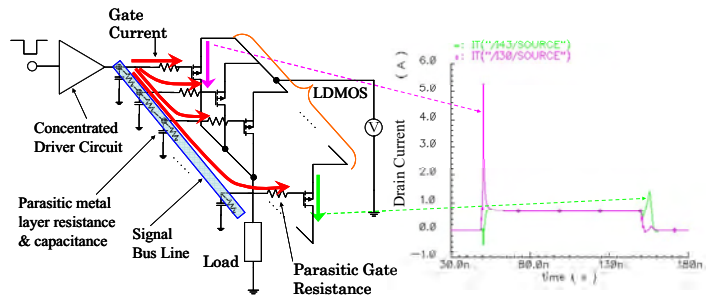
(a) Concentrated driver circuit layout
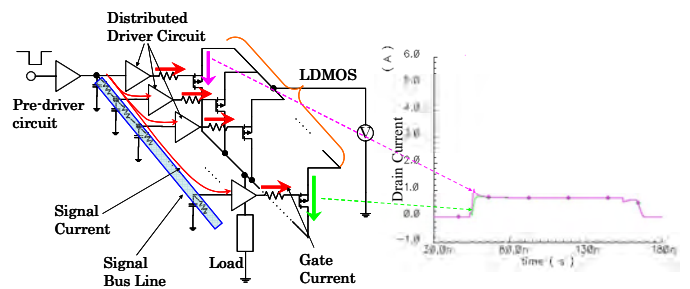
(b) Distributed driver circuit layout

Figure.3 Comparison of the distributed driver circuit layout with the conventional concentrated driver circuit layout and Simulated transient characteristics at condition of the resistive load.

We simulated the switching loss of distributed driver circuit and concentrated driver circuit in resistive switching when the input voltage, the resistance and switching frequency is 12V, 1.2ohm and 780KHz, respectively. The simulated condition is that the channel width of the gate driving MOSFET in the concentrated driver circuit is equal to the total channel width of the gate driving MOSFETs in the distributed driver circuit. Figure 3(a) shows the simulated transient characteristics of the drain current in the nearest segmented transistor to driver and in the farthest transistor from driver in case of concentrated driver circuit. The drain current is non-uniformly distributed during switching time. Figure 3(b) shows the simulated transient characteristics of the drain current in the nearest segmented transistor to the input port and in the farthest transistor from the input port in case of the distributed driver circuit. The whole LDMOS device can uniformly turn on or off.

Table I shows the simulated switching loss of the distributed driver circuit and the concentrated driver circuit under resistive switching when the input voltage, the load resistance and switching frequency is 12V, 1.2ohm and 780 kHz, respectively. As shown in table I, the turn off loss of distributed driver circuit is reduced to 54% of that of concentrated driver circuit.

Table I. Simulated Device characteristics

	Concentrated driver circuit layout	Distributed driver circuit layout
Turn-on loss (mW)	12.1	5.48
Turn-off loss (mW)	48.6	26.6

@Vin=12V, Resistance =1.2ohm, Switching frequency=780kHz

V. EXPERIMENTAL RESULTS

Figure 4 shows the micrograph of fabricated chip based on the low cost 0.6um process. The chip size is 20.3mm^2. A number of driver circuits are placed between N-ch and P-ch LDMOS.
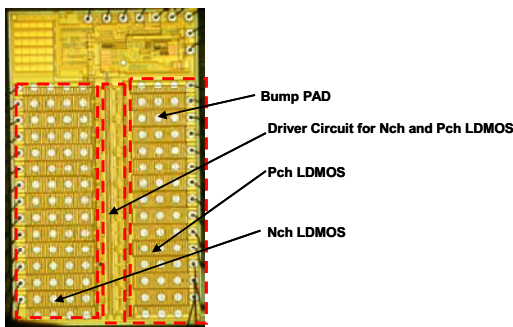

Figure.4 Micrograph of fabricated chip based on low cost 0.6um process. The chip size is 20.3mm^2

Figure 5 shows the measured output characteristics of a large area Nch LDMOS (the effective area 3.6mm^2). The on resistance is 9.7mΩ(@drain current=5A, gate voltage=5V). We have achieved that the value of on resistance is below 10mΩ in 20V LDMOS of Pw IC.
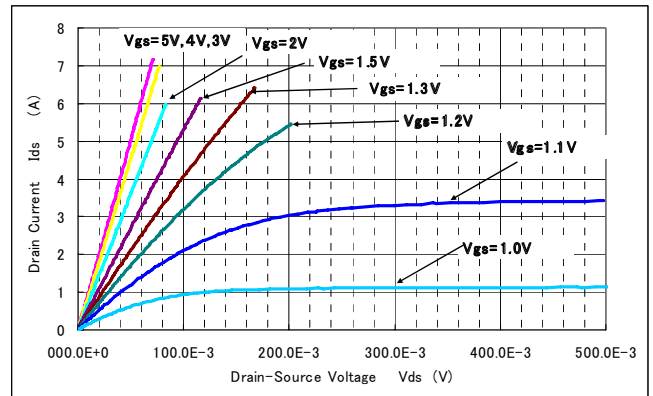

Figure.5 Output characteristics of a large area device (the effective area 3.6mm2).

Figure 6 shows the switching characteristics of the fabricated chip at the condition of an inductance of 2uH. Vi(HighSide), Vi(LowSide) and V(sw) indicate the input on/off signals for P-ch LDMOS and N-ch LDMOS and the intermediate voltage between the P-ch and the N-ch LDMOS devices, respectively. The rise time of V(sw) is 3ns. The fabricated device in the one-chip DC/DC converter exhibited high speed and high current switching capability of 10A.
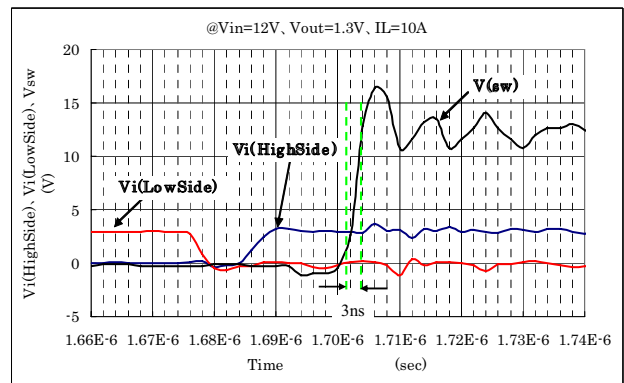

Figure.6 The switching characteristics of the fabricated chip at the condition of an inductance 2uH. The rise time of switching node is 3ns.

Figure 7 shows the measured efficiency comparison for low side LDMOS with N+ buried layer and with P+ buried layer when the input voltage, the output voltage and switching frequency is 12V, 1.3V and 780KHz, respectively. The N+ buried layer is more effective for suppressing the substrate current injection than the P+ buried layer. The difference of maximum efficiency between low side LDMOS with N+

buried layer and with P+ buried layer is 0.98%. The maximum efficiency is 88.9% at output current 5A in case of low side LDMOS with N+ buried layer. As shown in figure 7, the efficiency in the structure with source electrode extended over gate can be improved as compared with the structure with drain electrode extended over gate. The fabricated chip has accomplished the high efficiency.
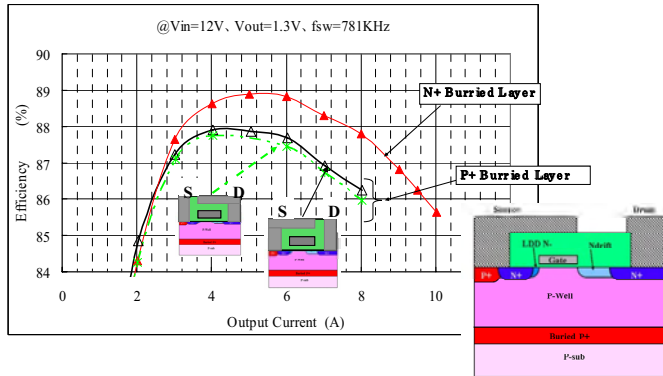

Figure.7 Measured efficiency comparison for low side LDMOS with N+ buried layer and with P+ buried layer. A higher efficiency can be achieved by the device structure with the source electrode extended over gate-poly(@input voltage=12V, output voltage=1.3V, switching frequency=781kHz).

Figure 8 shows the measured dependence of efficiency on the switching frequency when the input voltage, the output voltage is 12V, 1.3V, respectively. The difference of maximum efficiency is only 1.1% when the switching frequency is changed from 487KHz to 980KHz.
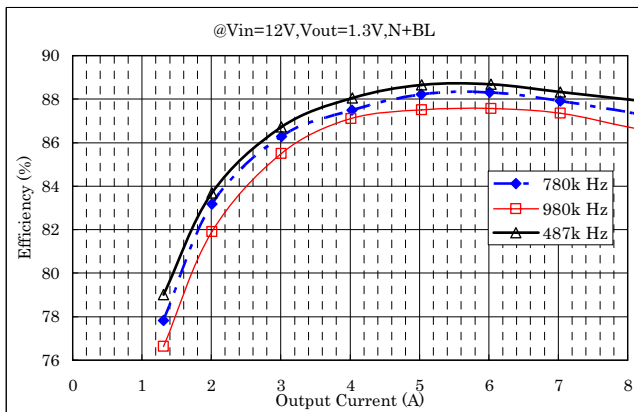

Figure.8 Measured dependence of efficiency on the switching frequency. (@input voltage=12V, output voltage=1.3V)

Figure 9 shows the measured dependence of efficiency on the dead-time. As shown in figure.9, the efficiency is improved as the dead-time is shorter. The maximum efficiency is increased by 1% when the dead-time is changed from 25.5ns to 8.5ns. It is more important to optimize the dead-time in the higher switching frequency.
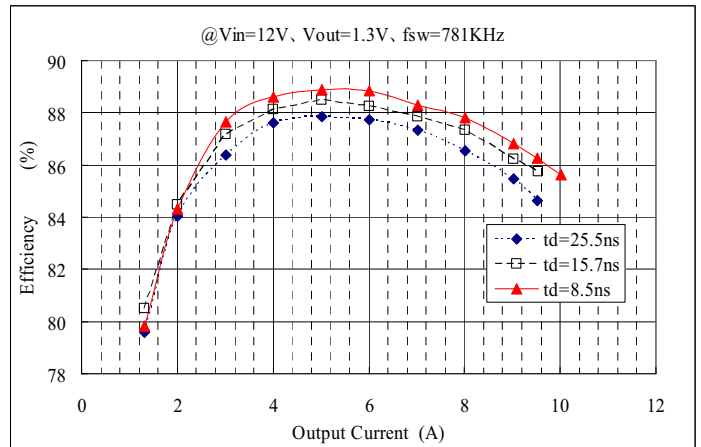

Figure.9 Measured dependence of efficiency on the dead-time. (@input voltage=12V, output voltage=1.3V, fsw=781KHz,N+BL)

VI. CONCLUSION

In this paper, we demonstrated high speed 10A DCDC converter by applying a metal interconnection with bump technology and adopting distributed driver circuit layout.

REFERENCES

[1] Y.Kawaguchi et al., "Multi Chip Module with Minimum Parasitic Inductance for New Generation Voltage Regulator," *ISPSD'05*, pp.371-374

[2]M.Shiraishi et al.,"Low Loss and Small SiP for DC-DC Converters," *ISPSD'05*, pp.175-178

[3]A. Nakagawa, "Evolution of Silicon Power Devices and Challenges to Material Limit," Proc. of MIEL 2006, pp.167-174

[4]K.Nakamura et al.," Demonstration of high frequency and 10A operation in 12V 1 chip DC/DC converter IC using bump technology," *BCTM'06*,pp.118-121

[5] Y.Kawaguchi et al, " Design for Efficiency Improvement and Future prediction in Multi Chip Module for DC-DC Converter," *PESC 2006*, PS 2-35

[6]T.Efland et al, " Lateral Thinking About Power Devices (LDMOS),"*IEDM'98*, pp.679-682

[7]Z.J.Shen et al, " Breaking the Scaling Barrier of Large Area Lateral Power Devices: An 1mΩ Flip-Chip Power MOSFET with Ultra Low Gate Charge," *ISPSD'04*, pp.387-390