Numerical analysis of SOI IGBT switching characteristics -- Switching speed enhancement by reducing the SOI thickness

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Abstract

Lateral IGBTs on thin SOIs are promising devices for use in trench isolated high voltage power ICs. This paper shows that the switching speed of SOI IGBTs is improved by reducing the SOI layer thickness without any special design. Furthermore, carrier recombination at the Si-SiO_2 interface affects carriers as if the bulk lifetime is reduced for a thin SOI, thus further improves the switching speed of IGBTs on thin SOIs such as 2 μm.

1. Introduction

Lateral IGBTs on SOIs are attractive devices for use in high voltage power ICs because of the low on resistance due to conductivity modulation. It was shown that a high breakdown voltage of over 500 V is possible for devices on thin SOI less than 15 μm by imposing a large part of applied voltage across the buried oxide. This makes it possible to realize complete high voltage device isolation by trenches[1].

Recent work has assumed that SOI device realizes high breakdown voltage under the RESURF principle([2]). This paper shows that the breakdown voltage is determined mostly by the 1-D MOS diode portion along the symmetry axis.

It was experimentally found that the turn-off waveforms for IGBTs on SOI were characterized by the unique tail current shape, what we call the terrace shaped tail current. Fig. 1 shows an experimentally obtained turn-off waveform for an IGBT on 10 μm SOI. The length of the terrace tail current period substantially determines the switching time. The mechanism for the terrace shaped current waveform will be analyzed.

Recently, it has been reported that IGBTs on SOI have an advantage in switching speed compared with conventional junction isolated IGBTs[3,4]. It has been found that the switching speed is further improved by reducing the SOI layer thickness. It has been also found that suface recombination cannot be ignored for the devices on thin SOI such as 2um.

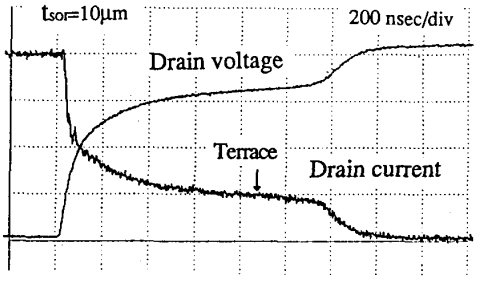

Fig. 1 Experimentally obtained turn-off waveform for an IGBT on 10μm SOI which has a unique shape characterized by a terrace shape current waveform.

2. Device design to realize a high voltage SOI device structure

Recent work has shown that an SOI device realizes high breakdown voltage under the RESURF principle([2]). The authors carried out breakdown voltage calculations for diodes on 10 μm thick SOI with various combinations of buried oxide thicknesses of 1 μm-3 μm and the impurity dose of the i-layer including p-type to reveal the breakdown voltage determination mechanism. The TONADDE II B program was used for the breakdown voltage simulations([5]).

The n+ buffer depth was assumed 4 μm. The ionization rates proposed by R. Van Overstraeten and H. DeMan([6]) were used for the ionization integral calculations. Fig. 2 shows the calculated breakdown voltages as functions of the impurity dose for various buried oxide thicknesses. The breakdown voltage abruptly decreased when the impurity dose exceeded the critical value because of the high electric field at the cathode side p-i junction. The critical impurity dose decreased with the increase in the oxide thickness.

The broken lines in Fig. 2 show the breakdown voltages of 1-D MOS diode structure [n-buffer/i-layer/oxide/substrate] along the symmetry axis. In the 1-D breakdown voltage calculation the junction between n+buffer and i-layer was treated as a step-wise impurity profile, for sim-

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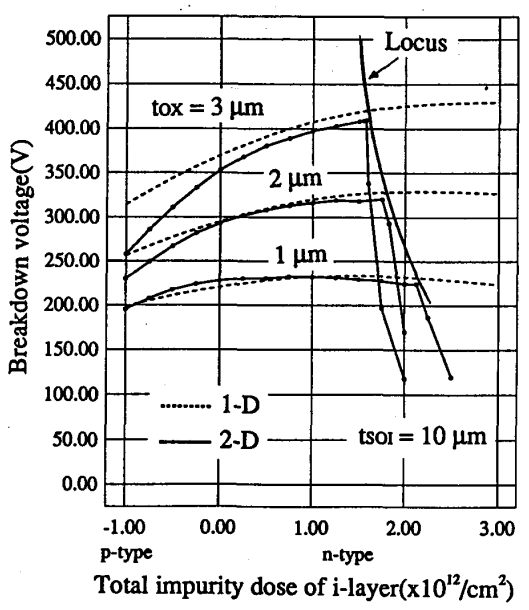

Fig. 2 Calculated breakdown voltage for 2-D structure(solid line) as well as that for 1-D MOS diode [n-buffer/i-layer/oxide/ substrate] structure along the symmetry axis of the 2-D structure(broken line) as a function of impurity dose of i-layer.

plicity. It has been found that the breakdown voltage is determined by the 1-D structure as far as the impurity dose is less than a critical value. Thus, the increase in the breakdown voltage with the impurity dose is mainly due to the breakdown voltage increase for the 1-D MOS structure, and 2 dimensional device design optimization has a minor effect if the drift region length is sufficiently large, because the optimum breakdown voltage is determined by the 1-D breakdown voltage.

3. Switching speed enhancement by the reduction of the SOI layer thickness

It has been reported that IGBTs on SOI operate at a high switching speed compared with conventional junction isolated lateral IGBTs. This is because carriers do not diffuse into the p-type substrate at the on-state and hence, the amount of stored carriers is reduced for IGBTs on SOI. In this section, it is shown that the switching speed is further improved by reducing the SOI layer thickness.

Simulation results

Simulations were carried out for IGBTs on 10 μm, 5 μm, and 2 μm SOIs. Fig. 3 shows the analyzed device structures. Based on the results of the previous section, each SOI layer was assumed to have the same total impu-

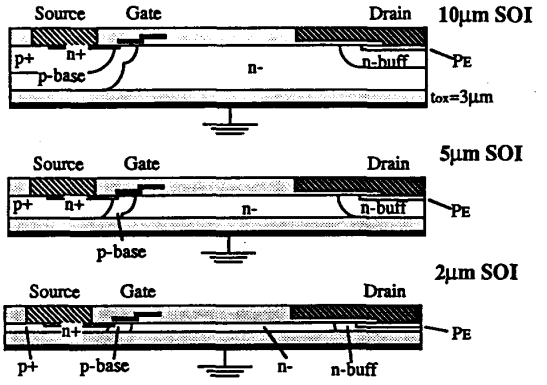

Fig. 3 Structures of simulated thin SOI IGBTs with SOI layer thicknesses of 10 μm, 5 μm, and 2 μm.

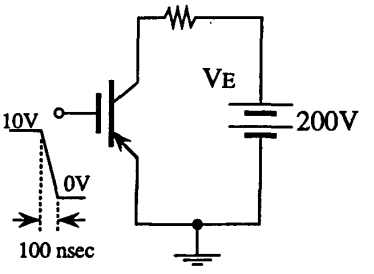

Fig. 4 Simulated circuit.

rity dose of 1.0×10^{12} /cm² and the buried oxide thickness was assumed to be 3 μm. The lifetime of both the electron and hole was 1 μsec for each device. The surface recombination was not taken into account for the present calculation. The effects of the surface recombination is discussed in the next section. The turn-off simulations were carried out under a resistive load, using the TONADDE II C program([7]). Fig.4 represents the simulated external circuit. The source voltage was 200 V and the initial drain current was 100 A/cm². Forward voltage drop for each device is 3.07 V, 3.25 V, and 3.38 V at 100 A/cm² current density, which is defined as the drain current divided by the device area.

Fig. 5 shows the calculated turn-off waveforms for IGBTs on 10 μm, 5 μm, and 2 μm SOIs with an applied voltage of 200 V. The obtained waveform for the IGBT on a 10 μm SOI agreed very well with the experimentally obtained waveform shown in Fig.1, and the terrace shaped tail current waveform was reproduced by the simulation. The fall time was found to be effectively shortened by reducing the SOI layer thickness without any special design

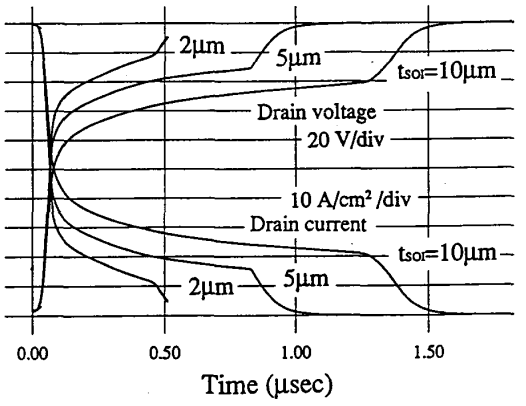

Fig. 5 Simulated turn-off waveforms.

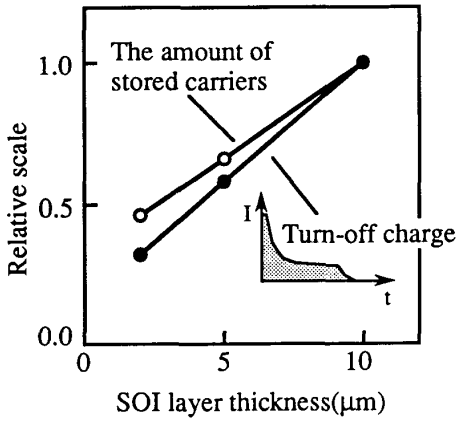

Fig. 6 The amount of stored carriers at the on-state and the integrated current charge at the turn-off as a function of the SOI layer thickness.

optimization. The calculated fall time for the 2 μm SOI IGBT was only 470 nsec, which is about 1/3 of that for the IGBT on a 10 μm SOI.

Switching speed enhancement mechanism

As shown in Fig. 5, the switching speed of 2 μm SOI IGBT was fast for the assumed carrier lifetime of 1 μsec. The fall time for the 2 μm SOI IGBT was 1/3 of that for the 10 μm SOI IGBT, while the forward voltage increase due to the reduction of the SOI layer thickness was as small as 0.3 V. As the surface recombination was not considered, this effect is purely due to the reduction of the SOI layer thickness.

Fig. 6 compares the amount of stored carriers at the

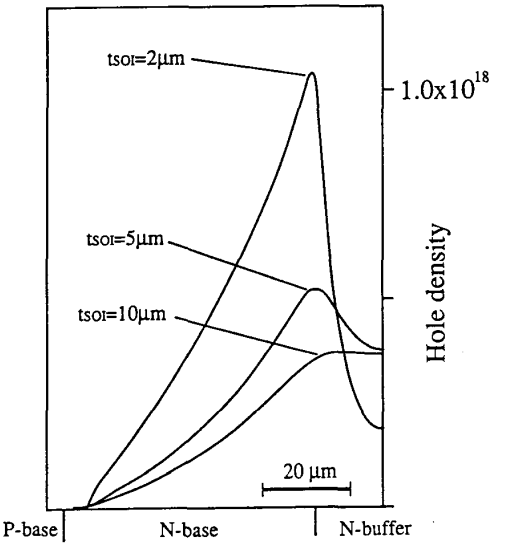

Fig. 7 Carrier density distributions in n-base at the on-state.

on-state and the integrated current charge at the turn-off transient. This figure shows that the turn-off time reduction comes from the reduced stored charge inside the device. The amount of stored carriers in the 2 μm SOI IGBT was reduced to less than a half of that for the 10 μm SOI. This is explained as follows. The actual density of current flowing laterally inside the SOI layer increases as the SOI layer thickness becomes thin, although the current density defined by the drain current divided by the device area is maintained to be 100 A/cm². For the 2 μm SOI IGBT, the actual current density was as high as 4750 A/cm$_2$, while 950 A/cm² for 10 μm SOI IGBT. Generally, at a high current density operation, the current tends to flow mostly by the drift current component because the injected carrier density level increases as shown in Fig. 7, and hence, the emitter efficiency is reduced. This results in that the value of the total stored charges divided by the total drain current decreased, resulting in a high switching speed.

It can also be seen from Fig. 6 that the integrated current charge at the turn-off transient reduced by 67 % with reducing the SOI layer thickness, while the actual stored charge was reduced only by 55 %. Hole current occupies only 35 % of the total current for the 2 μm SOI IGBT, while it is 44 % for the 10 μm SOI IGBT. Thus, less amount of holes was injected from the p-emitter during the turn-off for 2 μm SOI IGBT and, as a result, the stored carrier is efficiently swept out.

The MOS channel resistance keeps the same although the SOI layer thickness is reduced and the drift layer resistance increases somewhat. This is one of the rea-

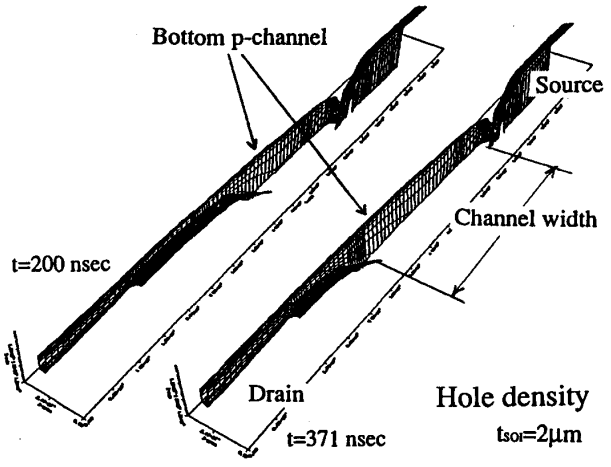

Fig. 8 Bird's eye views of hole density distribution for the 2 μm SOI IGBT during turn-off.

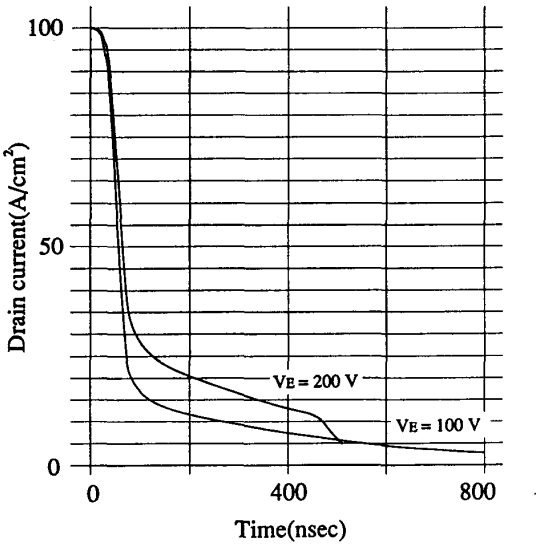

Fig. 10 Turn-off current waveforms for 2 μm SOI IGBT for two different source voltages, 100 V and 200 V.

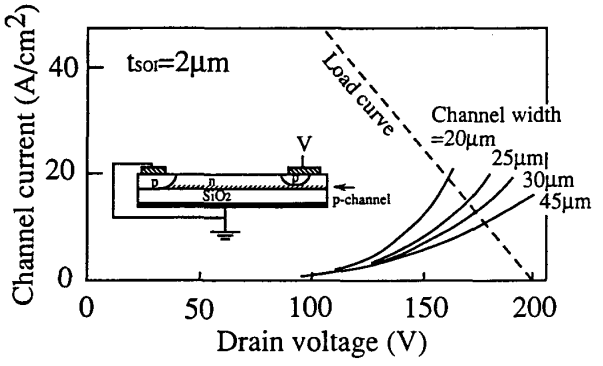

Fig. 9 Simulated V-I characteristic of the bottom p-channel as a function of applied voltage with the channel length as a parameter.

sons why the forward voltage increase due to the reduction of the SOI layer thickness was as small as 0.3 V.

4. Terrace shape current waveform mechanism

Switching waveforms for SOI IGBTs have unique shapes, characterized by a terrace tail current. The tail current abruptly decayed at the end of turn-off as shown in Fig. 1. It has been found from the simulation result that the abrupt decay started when the entire stored carrier was removed. This is because that the space charge region extended with time during turn-off and finally swept out the entire carriers stored in the n-base before the drain voltage reached 200 V. Only displacement current flowed after the stored carriers vanished, resulting in the rapid current decrease.

During the terrace period, the entire hole current flew through the induced p-channel on the bottom oxide in the depleted drift layer as seen in Fig. 8. Thus, the p-channel resistance determined the magnitude of the terrace current. Fig. 9 shows the simulated V-I characteristic of the bottom p-channel as a function of the applied voltage with the channel length as a parameter. The crossing point of the V-I characteristic and the load curve gives the magnitude of the terrace current.

The resistance of the bottom p-channel depends on the applied drain voltage, because the [i-layer/oxide/substrate] structure induces the p-channel and the channel length is the same as the length of the depleted drift layer. Thus, the turn-off waveform depends on the external source voltage. Fig. 10 compares the current waveforms for the 2 μm SOI IGBT for two different external source voltages, 100 V and 200 V. As the threshold voltage for the bottom p-channel is high, 100 V is not sufficient to induce the bottom p-channel. Thus, the terrace did not appear in the waveform for the source voltage of 100 V, and the waveform had a long tail current.

5. Influence of surface recombination on the device characteristics

In a thin SOI, the effects of surface carrier recombination is comparable to or more important than that of the

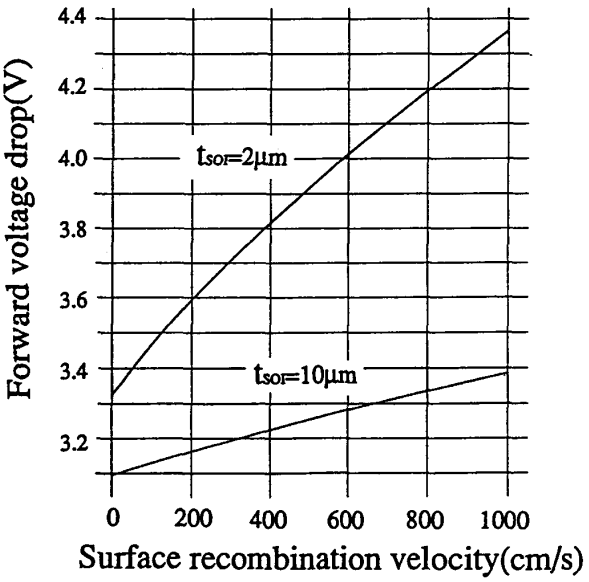

Fig. 11 Obtained forward voltage drops of the IGBTs as a function of surface recombination velocity.

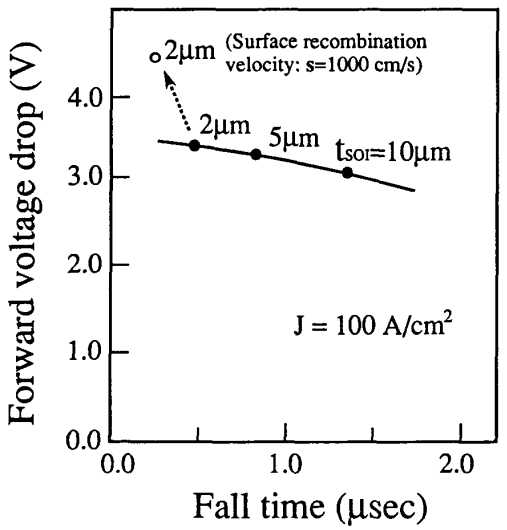

Fig. 12 Trade-off characteristic between the fall time and the forward voltage drop.

bulk recombination. The authors analyzed the effects of surface recombination on the characteristics of IGBTs on a 10 μm SOI and a 2 μm SOI.

Simulation results

The surface recombination velocity was assumed to be homogeneous along the surface and to be the same value for both the upper surface and the bottom surface of the SOI layer. Fig. 11 represents the calculated forward voltage drops of the IGBTs for a current density of 100 A/cm^2 as a function of the surface recombination velocity. The forward voltage rose as the surface recombination velocity became larger. The IGBT on the 2 μm SOI was about 5 times more sensitive to surface recombination than that on the 10 μm SOI.

The turn-off characteristics of the 2 μm SOI IGBT with a surface recombination velocity of 1000 cm/sec is shown in Fig. 12 as well as the characteristics of simulated IGBTs without considering surface recombination. Although the forward voltage rose by 1.0 V, the fall time was reduced to one half by adding surface recombination.

Switching speed enhancement mechanism

Surface recombination greatly affects the device characteristics if the SOI layer becomes very thin such as a 2 μm SOI. In a device on a thin SOI, the diffusion length of carriers in the bulk is much longer than the SOI layer thickness, thus surface recombination affects carriers as if the bulk carrier lifetime is reduced. The effective carrier lifetime τ_{eff} for a thin SOI, which takes into account the effect of recombination at the surface, is given by

$$1/\tau_{eff} = 1/\tau_{bulk} + (s_U + s_B)/t_{SOI} \qquad (1)$$

where τ_{bulk} is the bulk carrier lifetime, s_U and s_B are the surface recombination velocities at the upper surface and at the bottom surface, t_{SOI} is the SOI thickness. This implies that the influence of surface recombination on the device characteristics is in proportion to t_{SOI}^{-1}, which explains the simulation result shown in Fig. 11.

Fig. 13 represents the effective carrier lifetime τ_{eff} for a thin SOI as a function of the SOI layer thickness with the surface recombination velocity as a parameter. The bulk lifetime was assumed to be 1 μsec. For the 2 μm SOI IGBT, the calculated effective lifetime τ_{eff} became a small value of 91 nsec for a surface recombination velocity of 1000 cm/sec even when the bulk lifetime was assumed to be 1 μsec, thus carrier recombination at the surface greatly reduced the stored carriers in the n-base. This reduced the fall time and caused the forward voltage increase.

6. Conclusion

The electrical characteristics of SOI IGBTs including breakdown voltage has been discussed. The influence of recombination at the SOI layer surface was also esti-

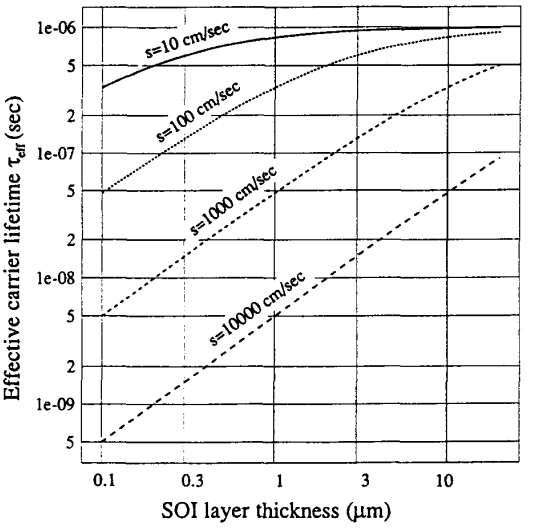

Fig. 13 Effective carrier lifetime τ_{eff} for a thin SOI as a function of SOI layer thickness with surface recombination velocity as a parameter($s=s_U=s_B$). Bulk carrier lifetime is assumed to be 1 μsec.

mated. It has been found that the switching speed of IGBT on a thin SOI is improved by reducing the SOI layer thickness without special design optimization. Recombination at the silicon surface works as if the bulk carrier lifetime is reduced for very thin SOIs.

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