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Application of General Purpose Power BiMOS Simulator TONADDEII to Double Gate Lateral Bipolar-Mode MOSFET Design.

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ABSTRACT

A rapid convergence Bipolar-MOS composite device simulator, TONADDEII, is presented. It was found that a combination of coupled method, complete Newton scheme, ILUBCG method, and 9 point discretization enables rapid convergence for both static and transient solutions regardless of bias conditions. TONADDEII can also utilize the so called Gummel's method (decoupled method) to reduce CPU time for low bias and reverse bias conditions.

The simulator was applied to a dielectrically isolated double gate lateral Bipolar-Mode MOSFET(DGLIGBT) to analyze the turn-off process, showing potential as a high frequency switching device.

1. INTRODUCTION

A rapid convergence bipolar-MOS composite device simulator, TONADDEII[1], has been developed. It reaches convergence within 4 or 5 Newton iterations regardless of bias conditions, if a proposed method is adopted. It was confirmed for a number of devices that inclusion of all the derivatives associated with three basic variables (p, n, ψ) in a Jacobian matrix for the complete Newton scheme is effective to accelerate convergence.

Conjugate gradient methods were successfully applied to a single differential equation (decoupled method)[2]. The present paper, first, shows that a combination of complete Newton scheme (coupled method), ILUBCG method and 9 point discretization realizes a rapid convergence bipolar device simulator not only for static cases but also for transient and high voltage cases(more than 600V). Second, the simulator was applied to analyze dielectrically isolated double gate lateral Bipolar-Mode MOSFET(DGLIGBT) characteristics.

2. COMPOSITE DEVICE SIMULATOR--TONADDEII

(TOshiba Numerical Analysis Program for Device DEsign)

TONADDEII is a general purpose two dimensional bipolar-MOS composite device simulator, being capable of 1)breakdown voltage prediction, 2)static and transient device characteristic simulation. It adopts the finite difference method, easily taking advantage of iterative solution techniques. It can deal with any device structures, including SiO_2 and air regions.

2.1 Physical model[3,4,5]

It was shown[3,5] that both the effects of bandgap narrowing and Fermi statistics can be included in the Boltzmann-like equation:

$$J_n=\mu_n kT \text{ grad } n-q\mu_n \text{ grad}(\psi+\delta V_c+\omega_n)$$
$$J_p=-\mu_p kT \text{ grad } p-q\mu_p \text{ grad}(\psi-\delta V_v-\omega_p)$$

,where δV_c and ω_n mean conduction band edge shift and effect of Fermi statistics, respectively, and are defined as follows:

$$N_c \exp q(F_n-E_c+q\omega_n)/kT = \int\rho(E-E_c)/(1+\exp(E-F_n)/kT)dE$$

$E_c=E_{c0}-q\delta V_c$ (E_{c0} means the conduction band edge for undoped silicon).

δV_v and ω_p are defined by a similar equation.

ω_n and ω_p can be assumed to be constant and depend only on the impurity concentration because they do not significantly change if excess carrier density is less than $10^{18}cm^{-3}$.

Thus, measured bandgap narrowing ΔV_G under the assumption of Boltzmann statistics should be considered to be equal to $(\delta V_c+\delta V_v+\omega_n+\omega_p)$ and to effectively include the effects of Fermi statistics.

The electron and hole mobilities including carrier to carrier scattering were modeled as follows (see [4] for the values of the constants):

$$\mu_n = \frac{\mu_{max}-\mu_{min}}{1+\left(\frac{N_D+N_A}{N_R}+\frac{n+p}{N_{R1}}\right)^{\alpha}} + \mu_{min}$$

Electron and hole lifetimes τ_p, τ_n are given by the following way:

$1/\tau_p = 1/\tau_i + 1/\tau_1$,

$\tau_i = 1\mu s\ [10^{18}/(N_D+N_A)]^{0.4}$,

Where τ_1 is the lifetime for a high resistivity region and τ_i expresses an impurity comcentration dependent component. Electron lifetime τ_n is given by the following expression:

$\tau_n = R\ \tau_p$, ($R=1.0, \tau_1=1.0\mu s$ for the present calculations) where R is chosen, depending on what lifetime killer is introduced.

Auger recombination is included using the following expression(see [4]).

$$R_{Aug} = (\gamma_n n + \gamma_p p)(np - n_i^2)$$

2.1 Solution technique

2.11 Coupled solution method

TONADDEII can utilize two solution methods: a decoupled method and a coupled method. The coupled method adopts a variable set(p,n,ψ) and the unique 9 point discretization scheme, which means that all variables associated with adjacent 9 grid points (A,B,C,D,E,F,G,H and I shown in Fig.1) appear in the discretized difference equations and are treated as variables also in Newton's iteration scheme. These are effective to accelerate convergence by including all the derivatives in Jacobian matrix for Newton's scheme[1]. For example, the Y- component of an electric field for point M (center of two grid points,B and C) must be calculated from 6ψ's associated with points B,C,D,E,F and G. Thus, the mobility derivatives associated with the adjacent 9 grid points must appear in the linearized difference equations. The obtained Jacobian matrix A for Newton's iteration has the form shown in Fig.2, where ⊠ denotes a 3 by 3 matrix.

TONADDEII adopts iterative solution techniques to solve a large set of linearized equations: $A\delta x=b$. However, for ill-conditioned problems, the direct solution method can be utilized as an option, although it requires a large memory size and a long computation time.

The authors published detailed test results obtained using iterative solution methods adopted in TONADDEII[1]. ILUCGS method was efficient for static manalysis[6].For high voltage transient analysis, ILUBCG method was more stable and efficient than ILUCGS and a larger time step increment Δt was allowable for the ILUBCG method. In general, ILUBCG was reliable for all the cases[1].

TONADDEII reached convergence within 5 Newton iterations regardless of bias conditions to assure more than 5 digit accuracy in current continuity as seen in Fig.3, if the proposed coupled method was adopted.

2.12 Decoupled solutiuon method

For calculations of a reverse biased PN junction or for low injection conditions, the decoupled method is sufficient and reaches convergence in less CPU time than when a coupled method is used. Figure 3 also shows a

typical convergence characteristic comparison between the decoupled method(Gummel's method) and the proposed coupled method when they are applied to a bipolar transistor. Users should choose the decoupled method to reduce CPU time, as long as it smoothly converges.

2.13 Time-dependent solution including external circuit.

In order to simulate transient characteristics for Bipolr-Mode MOSFETs, efficient solution algorithms (see Fig.4) have been developed. These are 1)adequate initial guess generator, 2)automatic time step generator and 3)efficient external circuit solution algorithm.

An automatic time step generator adopts a very simple but reliable method. Time increment Δt is repeatedly reduced to half its own value until all of the corrected $p+\delta p$ and $n+\delta n$ values become positive after the initial Newton cycle for each new time step. Since adequate judgement for Δt value was carried out based on the results obtained from the initial Newton cycle, CPU time can be greatly saved. Time increment Δt for the next time step is automatically set as twice the previous value when the convergence is successfuly obtained.

3.ANALYSIS OF DOUBLE GATE LATERAL BIPOLAR-MODE MOSFET(DGLIGBT) TURN-OFF CHARACTERISTICS.

A channel electron mobilty model, included in TONADDEII, adopts a modified Yamaguchi model[1]. Instead of decomposing the electric field into two components, vertical and pararell to the current vector, TONADDEII simply uses E_x and E_y in order to facilitate inclusion of mobility derivatives in a Jacobian matrix. For vertical and lateral Bipolar-Mode MOSFETs, this approximation gives only a small error of less than 1% in total drain current for 12.5V gate voltage[1].

$$\mu_{ch}=\mu_0(|E_x|)(1+1.539\cdot 10^{-5}|E_y|)^{-0.5} \quad ----(5)$$

This channel mobility is only applied for electrons in the channel region and in the accumulated layer beneath the gate electrode(see [1] for details).

Bipolar-Mode MOSFETs (IGBT) are nearly ideal power devices, achieving large current capability and high switching speed[7,8], simultaneously. Regarding vertical devices, even 1000V 300A devices have already been developed.

Figure 5 shows a cross-sectional view of the lateral DGIGBT analyzed in the present paper. The double gate structure was shown to be effective to improve switching speed[9]. The analyzed structure is different from that in Fig. 6 in regard to the location of the second gate. It was found that the structure in Fig. 5 attains a lower forward voltage drop, because the N^+-layer in the P-drain decreases the PNP transistor current gain if it is provided in a portion near to the source layer within the P-drain, as is the case shown in Fig.6. Figure 7 shows calculated current voltage characteristics. $50A/cm^2$ current density is attained for 2.75V forward voltage.

Figure 8 shows calculated inductive turn-off waveforms. In the calculation, the second gate was used to create a schort-circuit between the N-buffer and the drain electrode only in the turn-off transient to increase turn-off switching speed. First, the second gate voltage is raised to 12.5V to realize effective 'anode short', approximately 1.5μs before turning-off the first gate. An extremely short fall-time such as 20nsec was obtained for the present structure.

Figures 9(A) and (B) show the electron and hole density distributions for initial time step (t=0). It should be pointed out that the P^+-region facing the isolation

silicon dioxide layer is omitted from the hole density plot to show the internal hole density distribution. It is seen that the carrier distribution is very similar to that for a saturated PNP transistor.

Figures 10(A) and (B) show carrier distributions for 1.53μs time step and 10.2V drain voltage. Figures 11(A) and (B) show carrier distributions for 1.59μs time step and 100V drain voltage. It is seen in Fig. 11(B) that the hole current path is squeezed to a narrow portion in the P^--layer because the depletion layer develops in the P^--layer beneath the N^--drift layer and under the second gate electrode. The second gate shunts the N-buffer and the drain electrode, extracting the electrons from the N-buffer (namely, the N-base for PNP transistor)

Figure 12 shows the potential distribution corresponding to Figs.11(A), (B). Although 100V is applied, the N^--drift layer is not completely depleted, because the device is designed to have more than 500V breakdown voltage.

After the drain voltage reaches the electric source voltage, the drain voltage is clamped at 100V and the drain current rapidly reduces. Figure 13 shows the hole density distribution for 1.6μs time step. The hole injection into the N-buffer is completlely ceased at this stage.

It should be noted that, in the turn-off transient, hole and electron currents take different paths from each other when the anode voltage begins to recover. This is because the electron current flows in the N^--drift layer, whereas the hole current flows in the P-layer, namely the collector layer of the PNP transistor as seen in Fig.14.

4.CONCLUSION

A rapid convergence bipolar MOS composite device simulator TONADDEII was presented. The simulator was applied to a lateral dielectrically isolated double gate bipolar-mode MOSFET to show its potential as a high frequency switching device for high voltage power ICs.

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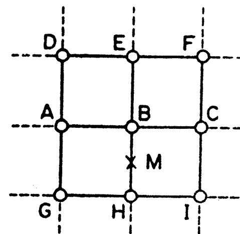

Fig.1 Grid system for 9 point discretization.

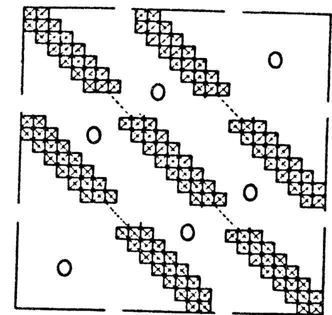

Fig.2 Jacobian matrix A for Newton iteration including all derivatives associated with adjacent 9 grid points. ⊠ shows 3 by 3 sub-matrix.

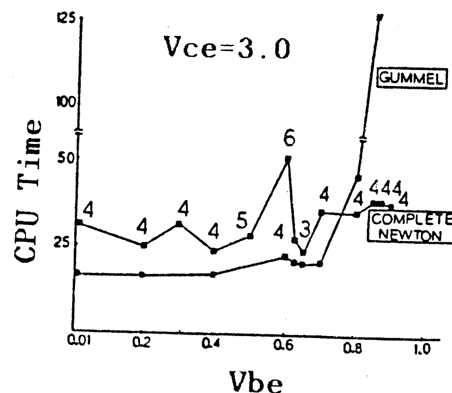

Fig.3 CPU time for convergence as a function of gate voltage is compared between Gummel' method and complete Newton's method, when they are applied to a bipolar transistor.

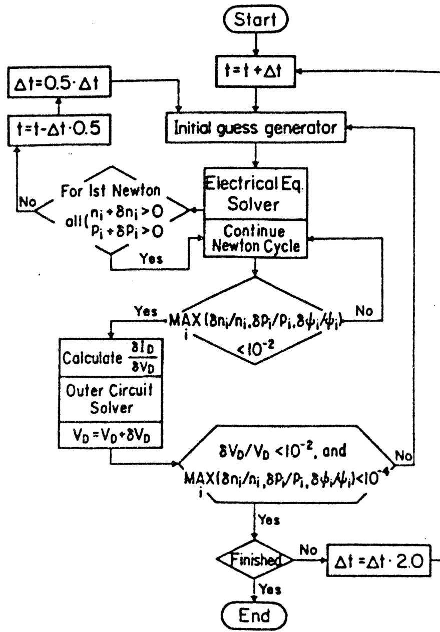

Fig.4 Flow chart for transient analysis.

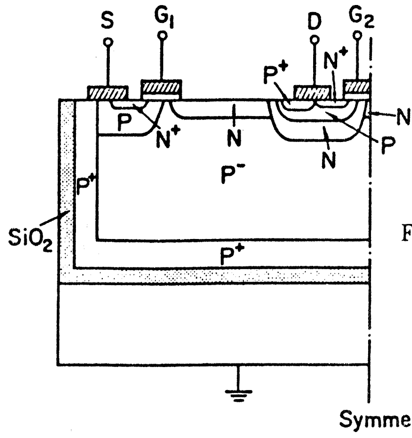

Fig.5 Analyzed dielectrically isolated 500V lateral double gate Bipolar-Mode MOSFET.

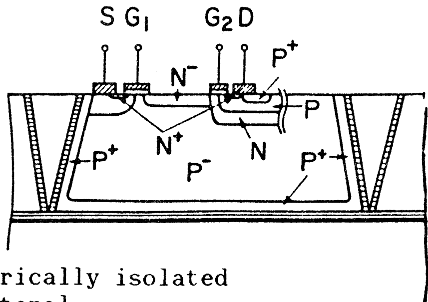

Fig.6 Dielectrically isolated 500V lateral double gate device.

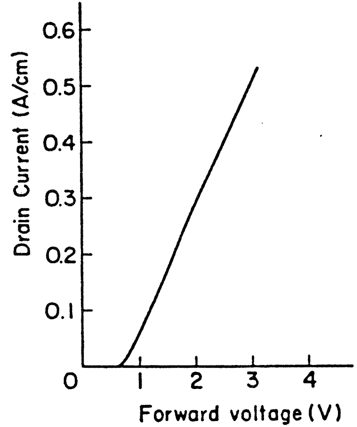

Fig.7 Calculated current voltage curve for the DG device shown in Fig.5.

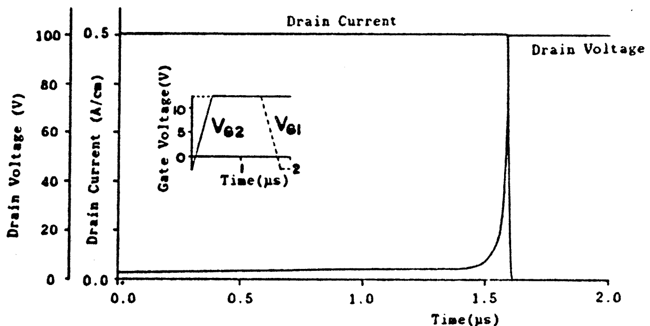

Fig.8 Calculated inductive turn-off waveforms. The second gate is turned-on, 1.5μs before turning-off the first gate.

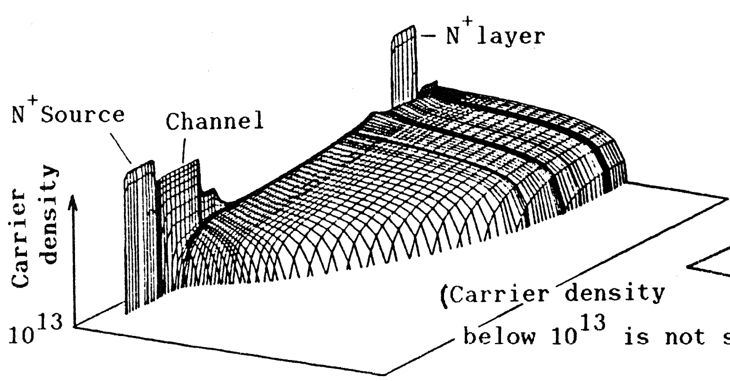

Fig.9(A) Electron density plot for t=0.

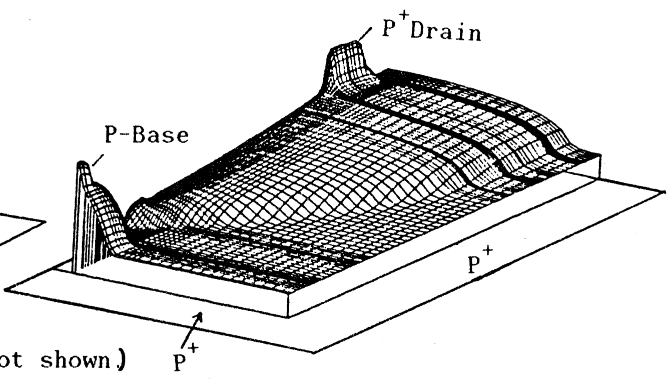

Fig.9(B) Hole density plot for t=0.

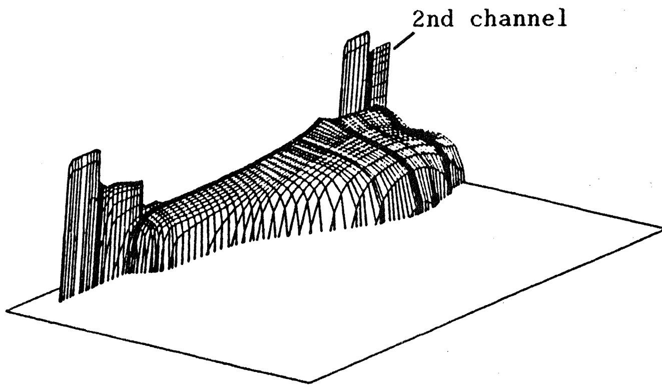

Fig.10(A) Electron density plot for t=1.53μs. (V_D=10.2V)

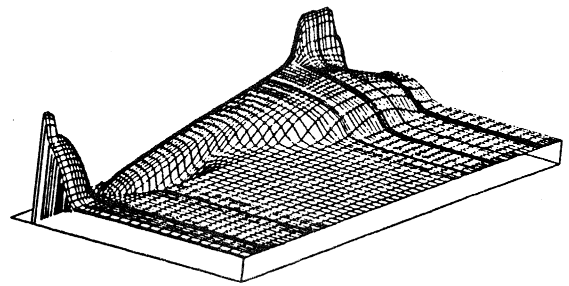

Fig.10(B) Hole density plot for t=1.53μs. (V_D=10.2V)

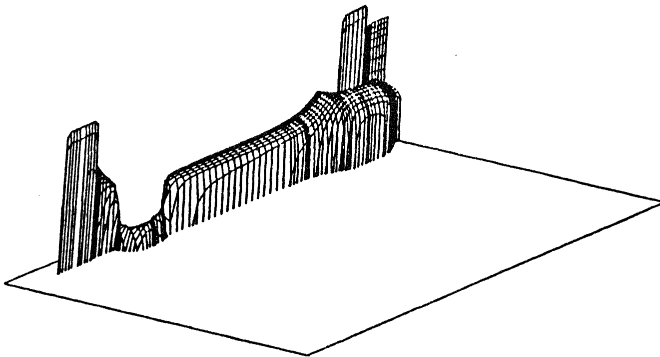

Fig.11(A) Electron density plot for t=1.59μs. (V_D=100V)

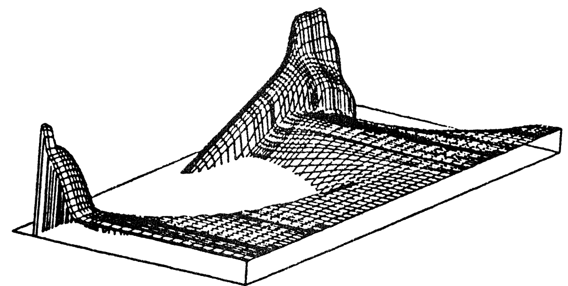

Fig.11(B) Hole density plot for t=1.59μs. (V_D=100V)

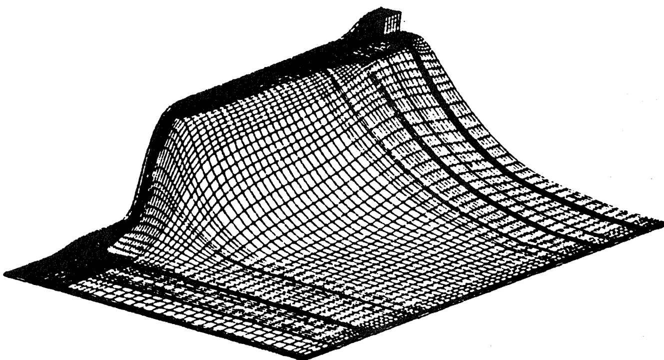

Fig.12 Potential distribution for t=1.59μs.

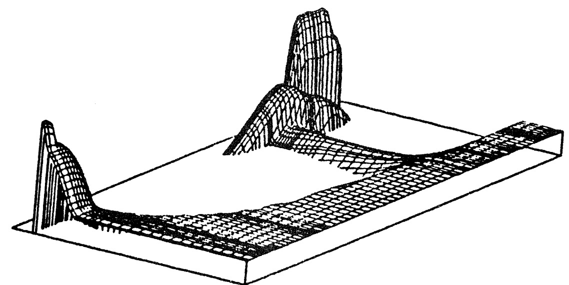

Fig.13 Hole density plot for t=1.6μs.

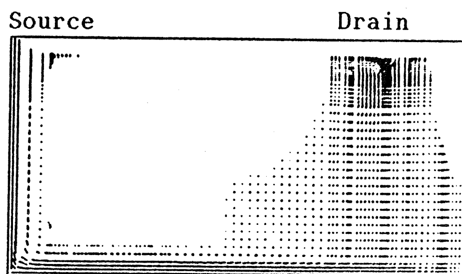

Fig.14 Hole current flow vector corresponding to Fig.11(B).