# New High Voltage SOI Device Structure Eliminating Substrate Bias Effects

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## ABSTRACT

The breakdown voltage of a conventional SOI device is limited because it requires a thicker buried oxide as well as a thicker silicon layer. A new SOI device structure and its substrate are proposed to breakthrough these constraints. The proposed new SOI is characterized by a SIPOS(Semi-Insulating POly-crystalline Silicon) layer inserted between the silicon layer and the buried oxide. Since the SIPOS layer effectively shields the influence of the substrate bias, 600V breakdown voltage SOI diodes and lateral IGBTs were successfully realized using 0.8μm SIPOS layer and 0.8μm buried oxide.

## INTRODUCTION

It is well known that the breakdown voltage of high voltage lateral SOI devices depends on the buried oxide thickness as well as silicon layer thickness[1]. Figure 1 shows typical experimental results, showing how the diode or MOSFET breakdown voltage depends on the two parameters. It is very difficult to achieve a high breakdown voltage exceeding 600V, because a thicker buried oxide layer of 4 μm or more is required in the conventional structure.

The present paper proposes a new high voltage SOI device structure, which is free from the above constraints. The original idea was first proposed by one of the authors in 1991[2]. The authors have experimentally verified, for the first time, the effectiveness of the proposed new SOI device structure and the new device design concept of realizing high breakdown voltage SOI devices by actually fabricating the proposed lateral diodes and lateral IGBTs (LIGBT).

## NEW SOI DEVICE STRUCTURE

In the conventional SOI diodes, maximum breakdown voltage is substantially limited by the breakdown voltage of the MOS diode portion (see Fig.2), consisting of $n^+$-cathode, $n^-$ layer, buried oxide and the substrate. The actual SOI device breakdown voltage is further determined by the $n^-$ layer lateral impurity profile or so called Resurf principle. If the influence of the substrate potential can be shielded, it is possible to achieve a higher breakdown voltage in the SOI device.

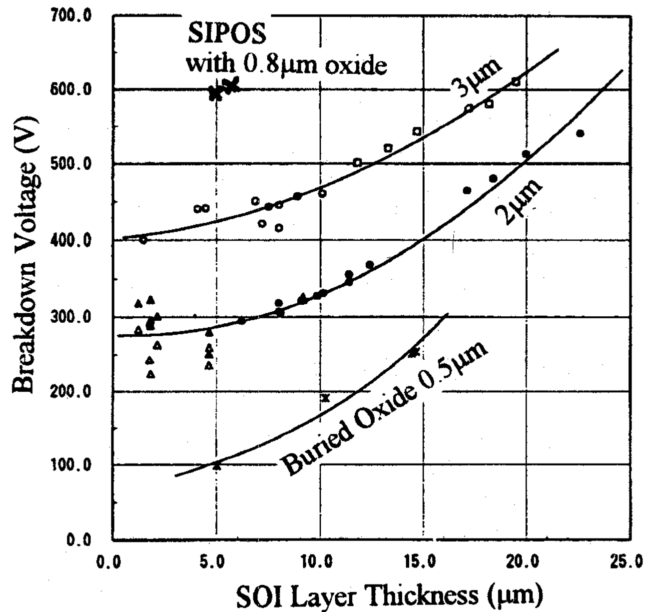


Fig.1 SOI diode breakdown voltage as a function of SOI layer thickness with buried oxide thickness as a parameter.
The breakdown voltage of the diode on new SOI with 0.8μm SIPOS layer and 0.8μm buried oxide is plotted as a comparison.

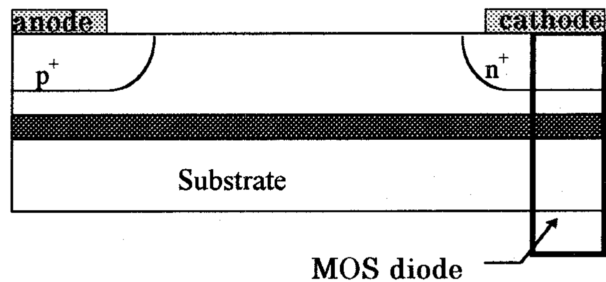


Fig.2 Conventional SOI diode



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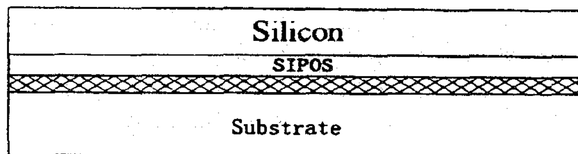
Figure 3 and 4 show the cross section of the proposed new SOI substrate and its spreading resistance profile, respectively. The new SOI structure is characterized by a SIPOS(Semi-insulating Poly-crystalline Silicon) layer inserted between the silicon layer and the buried oxide. If the SIPOS layer effectively shields the influence of the substrate bias, a high breakdown voltage SOI diode can be realized.




Cross section of new SOI substrate

Fig.3 New SOI structure

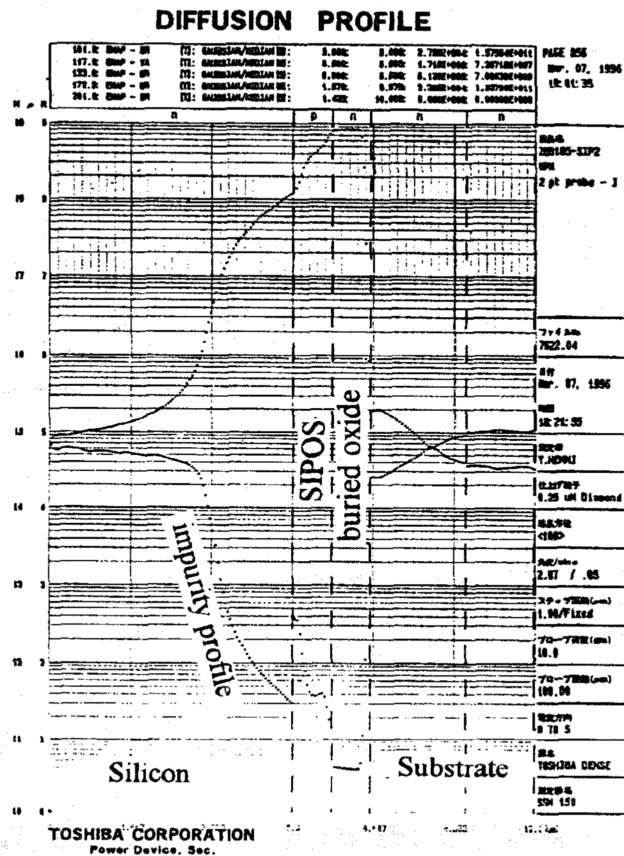



Fig.4 Spreading resistance profile of new SOI. Impurity out-diffusion into the SIPOS layer is observed.

## EXPERIMENT

### FABRICATION

We fabricated lateral diodes and lateral IGBTs on the new SOI wafers, consisting 5μm thick silicon layer / 0.8μm thick SIPOS layer / 0.8μm thick buried oxide. The fabrication process of the new SOI wafers are the following. First, a 0.8μm SIPOS layer and a 1μm thick undoped CVD oxide were subsequently deposited on a high resistance silicon wafer. Then, the wafer was bonded to a substrate wafer after polishing the CVD oxide surface. The wafer was grounded and polished to finally obtain a 5μm thick silicon layer over the SIPOS layer.

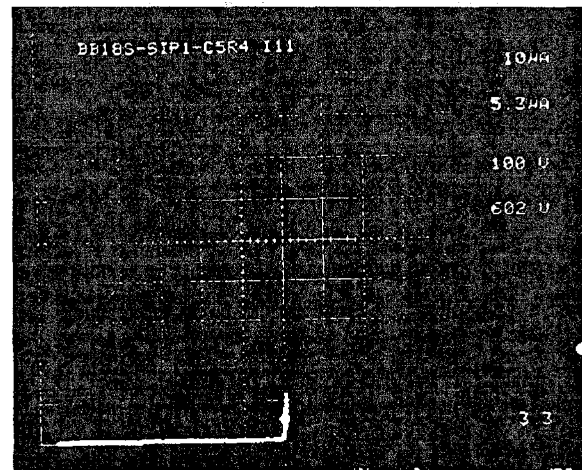



Fig.5 600V reverse current-voltage curve of the diode on new SOI.

Lateral diodes and IGBTs were fabricated both on the new SOI wafers and conventional SOI wafers (5μm thick silicon on 3μm thick buried oxide), using the same masks and fabrication processes. The diffusion depths of the diode $p^+$ and $n^+$ layers were more than 10μm and thus reached the buried SIPOS or the oxide. The diffusion depths of the IGBT p-base and the n-buffer were 4μm and more than 10μm, respectively.

### EVALUATION OF DIODEs

600V breakdown voltage was obtained by the new SOI diodes, using only 0.8μm thick buried oxide with 0.8μm thick SIPOS layer. Figure 5 shows the obtained diode reverse current voltage curve. The results are plotted in Fig. 1 as a comparison. The breakdown voltage of the new structure was even greater than those of the diodes on 3μm thick buried oxide.

Figure 6 shows the influence of the substrate

bias on the breakdown voltage of conventional SOI diodes and the new SOI diodes. In the conventional SOI, the diode breakdown voltage decreases as the negative substrate bias (source to substrate voltage) increases. As was expected, it was confirmed that the diode breakdown voltage on the new SOI was not influenced by the negative substrate bias. However, It was an unexpected fact that the positive substrate bias increased the diode breakdown voltage.

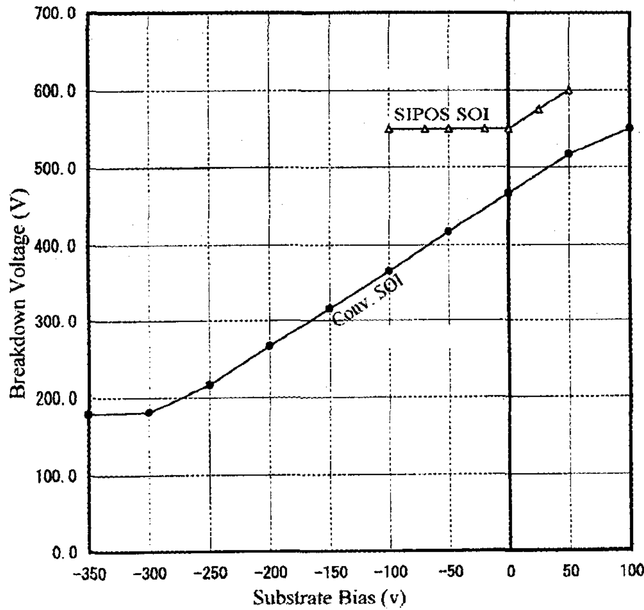



Fig.6 Substrate bias influence on breakdown voltage

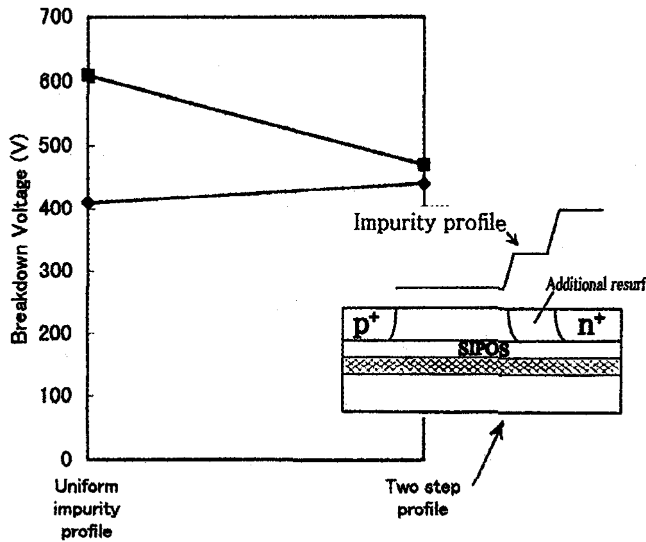



Fig.7 The breakdown voltage change with and without additional optimized Resurf layer. The breakdown voltage of SIPOS diode decreased when the optimized two step impurity profile for conventional SOI diodes was adopted.

The new SOI diode breakdown voltage is assumed to be determined by the conventional bulk pn junction theory and not by Resurf principle, which is believed to be valid for the conventional SOI device breakdown[2,3]. In other words, the breakdown voltage is determined by the high resistivity silicon layer impurity concentration ($5x10^{14}cm^{-3}$) and not by the total impurity dose of the SOI layer. Although an optimized two step lateral impurity profile, as illustrated in Fig. 7, increased the breakdown voltage of the conventional SOI diodes, the same impurity profile decreased the new SOI diode breakdown voltage because of the higher impurity concentration of the additional Resurf layer.

The measured leakage current increased as the temperature rose, as seen in Fig.8. Although the leakage current of 150°C is still acceptable level, efforts have to be necessary to improve the high temperature characteristics.

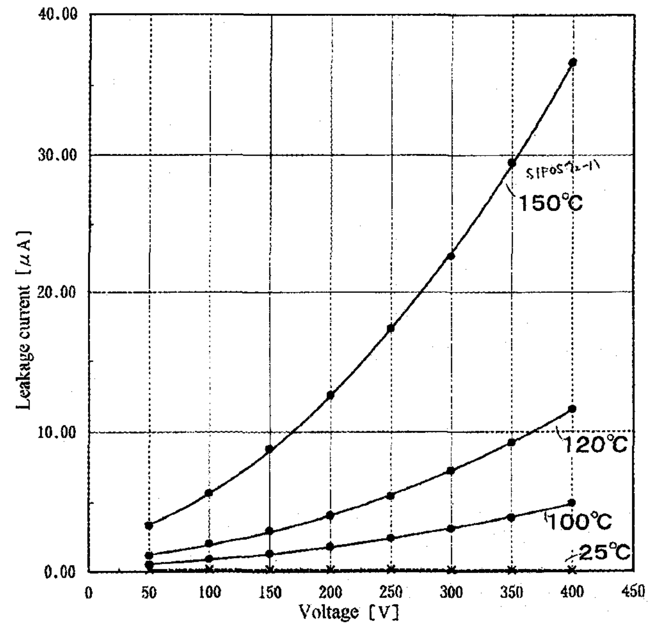



Fig.8 Reverse current voltage curves of new SOI

## EVALUATION OF LIGBTs

The advantage of the new SOI has been verified by fabricating lateral IGBTs on the new SOI (see Fig.9). The breakdown voltage of new IGBTs was 600V, and that of conventional LIGBTs on 5μm silicon/ 3μm buried oxide was 440V. Figures 10 shows the measured current-voltage curves of the fabricated lateral IGBTs on the new SOI. The forward voltage is 3.1V at $100A/cm^2$, which is slightly higher than that of conventional LIGBTs.

Figure 11 shows typical turn-off waveforms. The switching fall-time of 375nsec is faster than that of conventional LIGBTs. Figure 12 shows the trade-off relation of conventional LIGBTs together with the data of the fabricated new LIGBTs. The new structure has successfully increased the device breakdown voltage without sacrificing the device electrical characteristics.

## CONCLUSION

A new SOI device structure eliminating negative substrate bias influences and realizing a high breakdown voltage was proposed and experimentally verified. The proposed SOI structure is characterized by a SIPOS layer inserted between the silicon layer and the buried oxide. Since the SIPOS layer effectively shields the influence of the substrate bias, 600V breakdown voltage SOI diodes and lateral IGBTs were successfully realized using 0.8μm SIPOS layer and 0.8μm buried oxide.


References

[1]A.Nakagawa et al., 1992 IEEE IEDM Tech. Digest, p.229.

[2]A.Nakagawa, Proc. of ISPSD'91, p.16

[3]Y.S.Huang et al., Proc. of ISPSD'91, p.27.

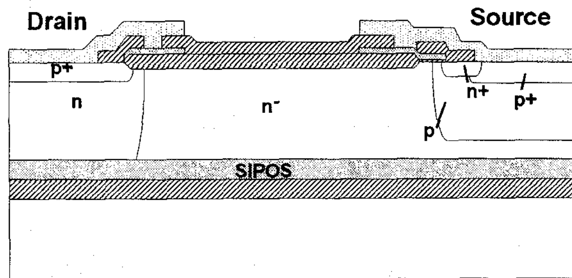




Fig.9 Lateral IGBT on new SOI substrate.

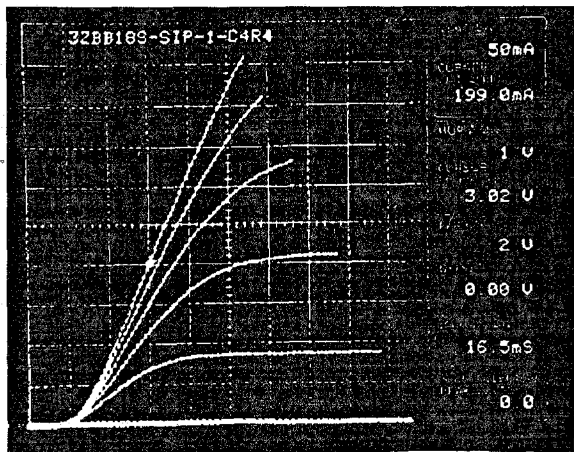



Fig.10 Current-voltage curves of fabricated lateral IGBTs on the new SOI.

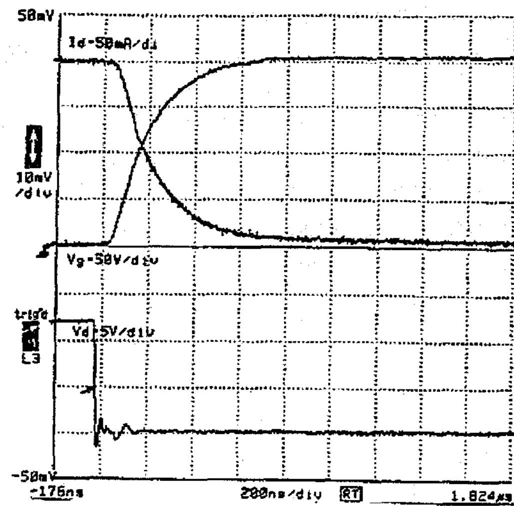



Fig.11 Typical turn-off waveforms of fabricated lateral IGBTs on the new SOI. The fall-time was 370nsec.

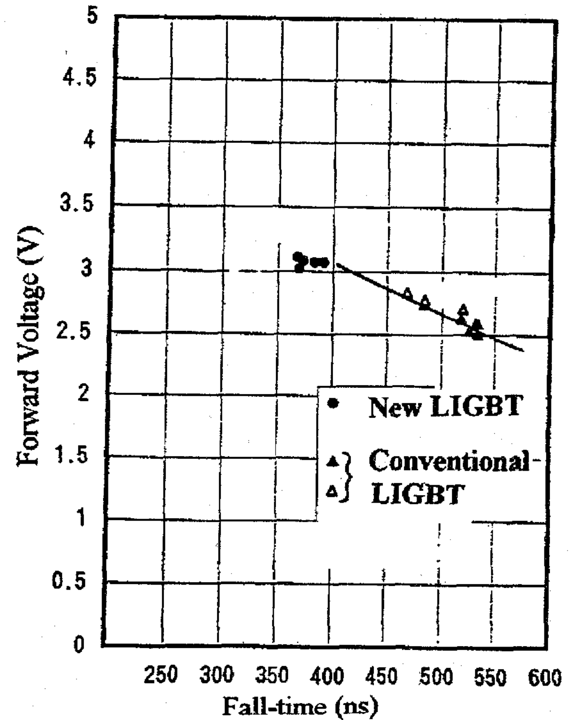



Fig.12 The trade-off relation of conventional LIGBTs together with the data of the fabricated new LIGBTs.