High Frequency 6000 V Double Gate GTOs

Tsuneo OGURA, Akio NAKAGAWA, Katsuhiko TAKIGAMI,
Masaki ATSUTA and Yoshio KAMEI

Research and Development Center, Toshiba Corp.,
1, Komukai Toshiba-cho, Saiwai-ku, Kawasaki-shi 210, Japan

ABSTRACT

A double gate GTO, consisting of an n-buffer and a second gate, has been developed for high frequency operation. A forward blocking voltage of 6000 V was realized, even at 150 °C when the second gate was shorted to the anode electrode. Turn-on and turn-off switching power loss can be reduced by adjusting the time interval between the two gate pulse triggering times for the first and second gates.

INTRODUCTION

High power gate turn-off thyristors (GTOs) have received much attention as key switching devices for high power inverters and choppers. To broaden the application range for the GTOs to PWM inverters, it is necessary to develop higher frequency GTOs operating above 3 kHz. The main problem in satisfying these requirements for the GTOs is the significant increases in on-state voltage and switching power loss caused by the increase in n-base width. In order to attain high blocking voltage simultaneously with low switching power loss, various device structures have already been proposed [1-4]. The authors also have already proposed a 6000 V GTO with a combination of an n-buffer and anode short structure [5]. However, the maximum operational frequency, even with this GTO, was still limited to less than 1 kHz. In order to attain high blocking voltage simultaneously with low turn-off switching loss, a double gate GTO has been developed and evaluated. The device was fabricated on a 33 mm diameter silicon wafer, using conventional diffusion and PEP techniques.

EXPERIMENTAL RESULTS

Forward blocking characteristics

Generally, there are three GTO structure categories: reverse blocking, anode short and n-buffer structures. The n-buffer structure is the most suitable to achieve high frequency operation in high blocking voltage GTOs, because the n-base width for the n-buffer structure is the narrowest in these three structures [5]. Therefore, the double gate structure has been combined with the n-buffer, as indicated in Fig.1. A second gate is placed on the n-buffer layer. A forward blocking voltage of 6000 V was realized by a 550 μm n-base with the n-buffer, even at 150 °C when the second gate was shorted to the anode electrode, as in Fig.2. The leakage current was 1 mA at 6000 V, approximately 1/10 of this value for conventional GTOs. This is because the hole injection from the p-emitter layer can be suppressed by shorting between the second gate and the anode electrode. The maximum allowable junction temperature for conventional GTOs is 125 °C, so the double gate GTO can operate at a higher temperature than conventional GTOs.

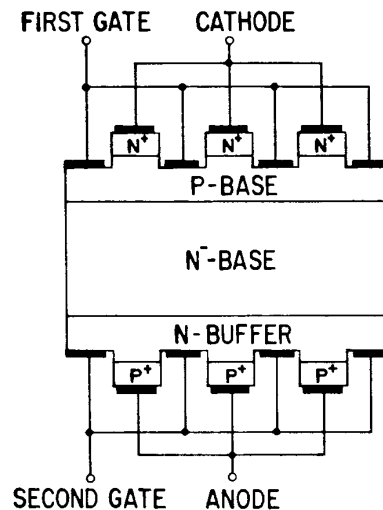
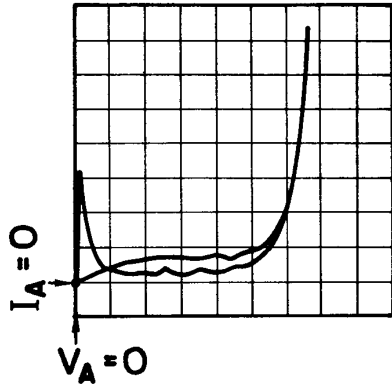


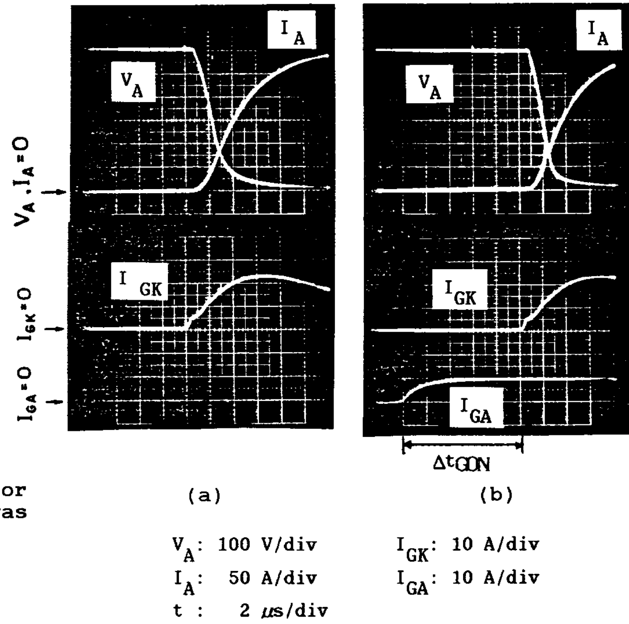
Fig.1 Cross-sectional view of double gate GTO

CH2528-8/88/0000-0610 $1.00 © 1988 IEEE



Tj = 150 °C
V_A : 1000 V/div, I_A : 0.5 mA/div

Fig.2 V-I characteristics at 150 °C for double gate GTO when second gate was shorted to anode electrode



V_A: 100 V/div I_{GK}: 10 A/div
I_A: 50 A/div I_{GA}: 10 A/div
t : 2 μs/div

Fig.3 Turn-on waveforms for anode voltage (V_A), anode current (I_A), first gate current (I_{GK}) and second gate current (I_{GA}) for (a) single gate triggering and (b) double gate triggering when Δt_{GON} =10 μs

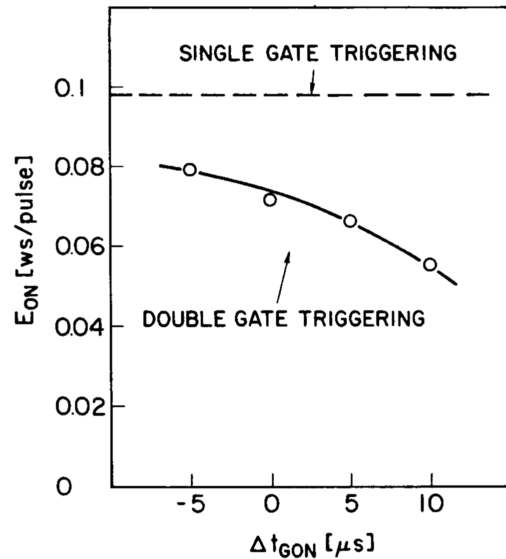


Fig.4 Turn-on switching loss (E_{ON}) dependence on Δt_{GON} for double gate GTO

Turn-on characteristics

It was found that the turn-on switching loss can be reduced by adjusting the time interval (Δt_{GON}) between the two turn-on gate pulse triggering times for the first and second gates. Figures 3 (a) and (b) show the turn-on waveforms from the anode voltage of 600 V for single gate and double gate turn-on triggering cases to compare the turn-on switching losses. It is apparent that the turn-on switching loss is decreased by the double gate triggering. The turn-on switching loss (E_{ON}) from 600 V anode voltage can be reduced by adopting a large Δt_{GON}, such as 10 μs, as is shown in Fig.4. However, it was found that this improvement by the double gate triggering diminished as the anode voltage increased over a voltage, where the whole n-base layer was depleted.

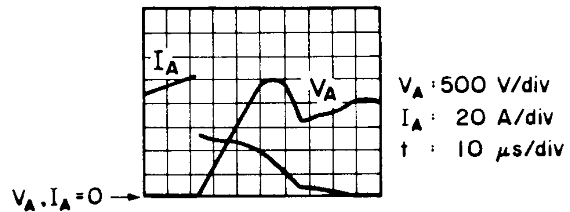
Turn-off characteristics and trade-off relation

The turn-off switching loss was greatly reduced by adjusting the time interval (Δt_{GOFF}) between the turn-off gate pulse triggering times for the first and second gates. The turn-off waveforms for three Δt_{GOFF} cases are shown in Figs.5 (a), (b) and (c), respectively. Figure 5 (a) shows the turn-off waveforms for the anode voltage (V_A) and anode current (I_A) when only the first gate is reverse biased during the turn-off period. The first gate can sweep away the excess carriers in the p-base and around the center junction. For single gate GTOs, it was been pointed out that the amount of excess carriers in the n-base at the initial stage for the tail current

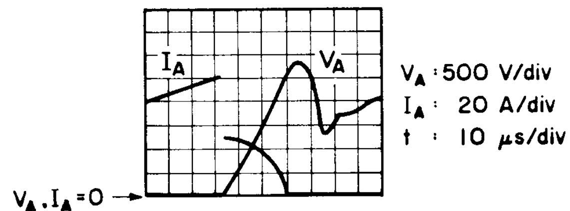
is nearly equal to that of the excess carriers at the on-state [6]. Therefore, a large tail current exists as seen in Fig.5 (a). The double gate GTO can sweep away the excess carriers in the p-base and n-base by the first and second gates. Figure 5 (b) shows the turn-off waveforms for the same device when the first and second gates were simultaneously reverse biased. In this triggering case, only a small amount of the excess carriers were swept away from the n-base before the recovery of the center junction, since the amount of the excess carriers in the n-base at the on-state was larger than that in the p-base. For the above reason, the peak value for the tail current in this case was almost equal to that in the case of Fig.5 (a). Therefore, it was necessary to adjust the time interval between the turn-off gate pulse triggering times for the first and second gates. The turn-off waveforms for the anode voltage, anode current, first gate current (I_{GK}) and second gate current (I_{GA}) for Δt_{GOFF}=55 μs are shown in Fig.5 (c). It is clearly seen that the tail current was greatly reduced by adopting a large Δt_{GOFF}, such as 55 μs. From these figures, it can be concluded that the second gate can sweep away the excess carriers in the n-base before sweeping away the excess carriers in the p-base by the first gate. The dependence of the turn-off loss (E_{OFF}) on Δt_{GOFF} is shown in Fig.6. This figure shows that the turn-off loss can be reduced by increasing Δt_{GOFF}.

The on-state voltage for the double gate GTO was compared with that for the single gate GTO. Figure 7 shows the experimental results for the n-base lifetime (τ_N) vs on-state voltage (V_T) for the double gate GTOs and single gate GTOs with identical n-base width. It can be concluded from this figure that the smaller p-emitter area caused by the mesa structure for the second gate portion does not affect the on-state voltage in the double gate GTO. Figure 8 shows a comparison in the trade-off relations between the on-state voltage and turn-off switching loss for the double gate GTO and the single gate GTO with an n-buffer and anode short [5]. The turn-off switching loss is reduced to approximately 1/20 of that for the single gate GTO by the double gate structure. This is because the turn-off loss can be reduced by adjusting the interval between the two gates, in addition to the second gate portion not affecting the on-state voltage.

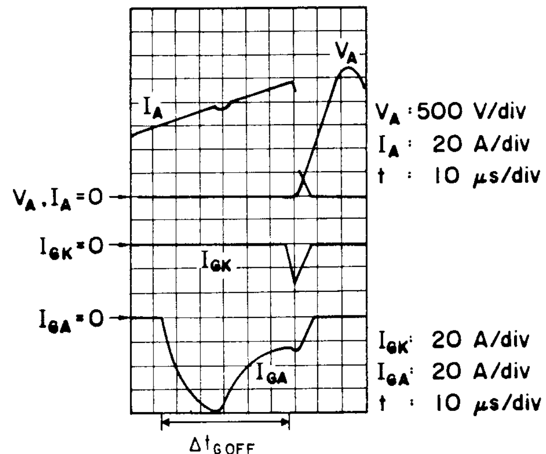
Figure 9 shows typical 400 A turn-off waveforms for the anode voltage, anode current, first gate current and second gate current during the turn-off transient. This device can turn off the anode current greater than 400 A, as shown in this figure.



(a) Turn-off waveforms for anode voltage (V_A) and anode current (I_A) when only the first gate is reverse biased



(b) Turn-off waveforms for anode voltage and anode current, when the first and second gates are simultaneously reverse biased (Δt_{GOFF} = 0 μs)



(c) Turn-off waveforms for anode voltage, anode current, first gate current and second gate current for Δt_{GOFF} =55 μs

Fig.5 Turn-off waveforms for double gate GTO

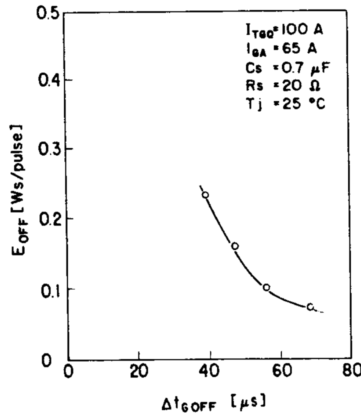


Fig.6 Turn-off switching loss (E_{OFF}) dependence on Δt_{GOFF} for double gate GTO

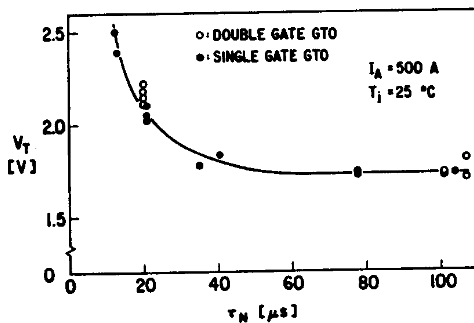


Fig.7 On-state voltage (V_T) dependence on n-base lifetime (τ_N) for double gate GTO and single gate GTO

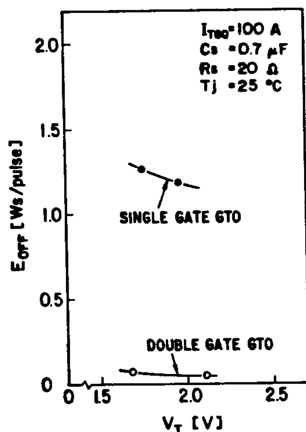
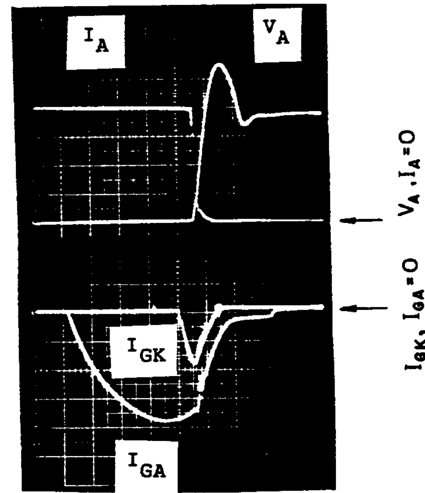


Fig.8 Trade-off relations between on-state voltage (V_T) and turn-off switching loss (E_{OFF}) for double gate GTO and single gate GTO with n-buffer and anode short [5]



V_A: 500 V/div I_{GK}: 50 A/div
I_A: 100 A/div I_{GA}: 50 A/div
t : 10 μs/div

Fig.9 Typical turn-off waveforms for anode voltage, anode current, first gate current and second gate current for double gate GTO

CONCLUSION

A double gate GTO, consisting of an n-buffer layer and a second gate on the n-buffer, has been developed to achieve low turn-on and turn-off losses in high blocking voltage GTOs. A forward blocking voltage of 6000 V was realized, even at 150 °C. The turn-off switching loss can be reduced to approximately 1/20 of that for a single gate GTO by adjusting the triggering times for the first and second gates.

REFERENCES

[1] T.Nagano, M.Okamura and T.Ogawa: IEEE-IAS Annual Meeting Record, 1978, p.1003.

[2] A.Tada, T.Miyajima, H.Hagino and M.Ishida: International Power Electronics Conf. Record, 1983, p.54.

[3] K.Murakami, N.Itazu, Y.Uetake, K.Mase and M.Takeuchi: International Power Electronics Conf. Record, 1983, p.42.

[4] M.Azuma, T.Shinohe, K.Takigami and H.Ohashi: 17th Conf. on Solid State Devices and Mater., 1985, p.393.

[5] T.Ogura, M.Kitagawa, H.Ohashi and A.Nakagawa: 19th Conf. on Solid State Devices and Mater., 1987, p.63.

[6] A.Nakagawa: Solid-State Electronics, 1985, p.677.

The Influence of Gate-Metallization Potential Drop on Transient GTO Characteristics

H. Bleichner, J. Vobecky[1], E. Nordlander[2].
Inst. of Technology, Dept. of Electronics,
Uppsala University, Uppsala, Sweden.

F. Vojdani, M. Bakowski.
ASEA Brown Boveri Drives, Västerås, Sweden.

ABSTRACT

A surveillance instrument has been developed for the measurement of the excess-carrier distribution in GTO samples at all stages of operation. The instrument, *i. e.* an optical scanner, admits visualization of the measurements as 3-D maps of the distributions for time- and space-resolved inspections of the electrical behaviour of the component.

The optical scanner was used to investigate if the gate-metallization pattern resistance would influence the transient characteristics of the GTO components. This paper will clearly show a strong dependence of, especially, turn-on behaviour upon lateral gate-metallization potential drop in a two-fingered structure.

INTRODUCTION

In power-thyristor manufacturing it is essential to control homogeneity of the electrical behaviour in the components. The GTO (gate turn-off thyristor) is an excellent example of the need for controllability due to the manner in which these components are made. A high-power GTO can be described as many elementary thyristors in parallel, with common anode and gate regions. The cathode emitters are uniformly distributed on the component surface, in a circular symmetry. Hence, the turn-on and turn-off characteristics is determined by the slowest cathode part of the component which calls for surveillance instruments combined with theoretical investigations of the component physics.

[1] Dept. of Microelectronics, Faculty of Electrical Engineering, Czech Technical University, Prague, Czechoslovakia.

[2] Gävle/Sandviken University College, Sandviken, Sweden.

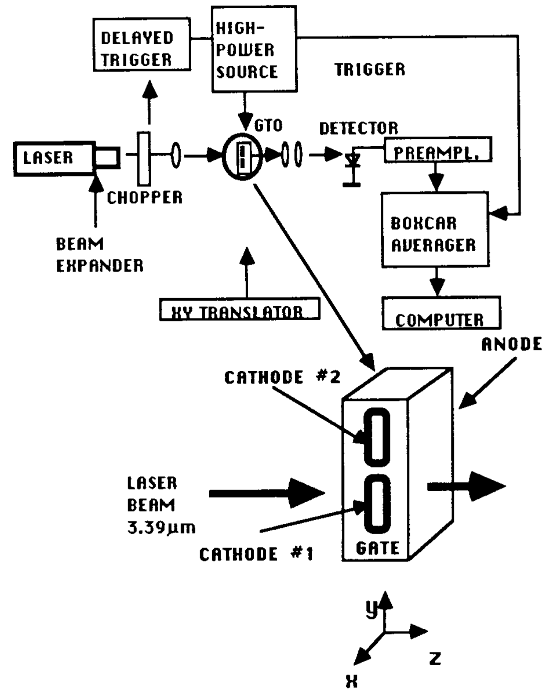


Fig. 1. Principle of optical-scanning equipment.

An optical scanner (fig. 1) has been developed as a surveillance instrument for the measurement of transient behaviour in individual cathode fingers. Carrier-distribution maps (fig. 2) in two spatial dimensions are produced, by means of free-carrier absorption of light, at numerous time intervals during the turn-on and turn-off procedures. Measurements under steady-state conditions may certainly also be performed. The use of a time and space resolved instrument based on absorption technique is novel in GTO applications, although the principles have been employed elsewhere for other kinds of measurements (1-3).

CH2528-8/88/0000-0614 $1.00 © 1988 IEEE