Study of Si-Wafer Directly Bonded Interface Effect on Power Device Characteristics

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Abstract

A high voltage transistor and an Insulated Gate Bipolar Transistor (IGBT) were fabricated by using Silicon-wafer Direct Bonding (SDB) technique to study the effect of direct bonded interface on power device characteristics. Prior to the device fabrication, heat treatment condition of SDB was investigated, and it was confirmed that electrically and mechanically stable SDB interface was obtaind at more than 1000°C. The transistor showed sufficiently high h_{FE}(=10) for this high voltage transistor. The fall-time and on-state voltage of IGBT were controlled by adjusting bonded interface position. All of these results encourage new SDB technique applications for power device improvements.

1. Introduction

Silicon-wafer Direct Bonding(SDB) technique has recently attracted notice as a new method for power device improvements. The SDB technique has many possiblities to improve problems, difficult to solve with conventional method[1],[2],[3]. At the 1986-IEDM, novel SDB technique applications were proposed and examined, showing successful results in replacing conventional epitaxy and dielectric device isolation techniques[4],[5]. In these applications, the silicon-wafer directly bonded interface was not embedded in a region where minority carrier plays important roles for power device behaviors. This work was done to study effect of the bonded interface on minority carrior behavior in power devices.

2. Stable SDB interface formation

In order to study the above mentioned problems, the authors discussed two category structures, shown in Table 1, fabricating Insulated Gate Bipolar Transistor (IGBT) and high voltage npn transistor for application feasibility study. Prior to device fabrications, SDB wafer heating temperature conditions were investigated to realize both mechanically and electrically stable interface formation, using 3-inches diameter wafers.

Before wafer heat treatment, a pair of mirror polished wafers are cleaned by treating with H_2O_2-H_2SO_4 mixture. Then, OH-group was formed on the wafer surfaces by treating in acid solution. These acid treated wafers were closely contacted face to face at room temperature in clean air. Wafer contact processing was carried out in a few minute just after the acid solution treatment to avoid natural oxide layer formation. The self-adhering wafer pairs were bonded under various heat treatment conditions in nitrogen atmosphere.

Fracture strength change with temperature was experimentally investigated. Figure 1 shows SDB-wafer infrared-images for various heating temperature conditions. As is schematically shown in Fig.2, it was found that observed fracture strength change is divided into 3-phases. Below 200°C in the first phase, measured fracture strength is almost constant, showing exsistence of self-adhesive force due to OH-group formation.

In the phase-2, as is shown in Fig.1, void generation begins, implying that hydrogen bonding change to Si-O-Si bonds by dehydration condensation reaction. As the reaction proceeds with temperature increase, vigorous void generation was observed. When temperature exceeds 700°C, void generation decreases rapidly, showing that the reaction completes as a result of OH-group consumption. Then, wafer bonding reaction gets into the phase-3. The wafer pairs are entirely bonded without any boid. However, understanding for residual oxygen atom behavior around the interface was not still clear in this work. The fracture strength reachs saturated value, resulting in excellent electrical and

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mechanical contact. All device fabrications described in this paper were made under the condition of more than 1000°C.

3. Device fabrication

Category-A device

In the cource of the category-A structure study, the authors fabricated a high voltage npn transistor, whose bonded interface was embeded inside the p-base layer. The structure and the impurity profile of the transisitor are shown in Fig.3. After lapping of the bonded wafer, an emitter layer impurity was diffused into the lapped side. The distance between the bonded interface and emmiter-base junction (Wp1) was adjusted from 6 to 14μm, by changing the lapping thickness.

Measured h_{FE} values are shown in Fig.4 with bonded interface position Wp1 as a parameter. Achieved maximum h_{FE} value was around 10, showing sufficient current amplification as a high voltage transistor (4kV). This high h_{FE} value means that, at least, 90% of injected carriers transport through the bonded interface. According to theoritical estimation, the collector current density, corresponding to the onset of base push-out, is 7A/cm² at V_{CE}=50V. This value well agrees with experimentally obtained value shown in the figure.

The bonded interface influence on the carrier lifetime was investigated by exact numerical device simulation. As is shown in Fig.5, numerically estimated average lifetime for the p-base with 10^{15}/cm³ impurity concentration is around 0.5 to 1μs. This rather short lifetime may be caused by the bonded interface.

Category-B device

For category-B structure investigations, impurity diffusion through bonded interface was observed. Figure 6 shows observed pn junction and bonded interface by newly developed copper plating method. Figure 7 shows relations between impurity diffsion length and heating time, showing that the bonded interface dose not act as obstacles against impurity diffusion. Noticing this feature, the authors fabricated an IGBT with a bonded interface, embeded inside the p-emitter substrate, to study carrier injection control feasibility by adjusting bonded interface position in the emitter. Figure 8 shows typical turn-off waveforms for different diffusion distance (Ld) IGBT, showing that fall-time increases with increase in diffusion distance from the bonded interface to pn junction. Figures 9 and 10 show bonded interface position influences on on-state voltage and fall-time for 1000V class IGBT. As is shown in the figures, on state voltage and switching time can be easily controlled without any conventional lifetime control techniques such as Au-diffsion and electron irradiation.

4.Discussions

As is previously described, the purpose of this work is to study SDB interface effect on power device characteristics. In the course of the category-A strcture study, it was found that the bonded interfaces effects on minority carrier lifetime is rather large, in comparison with conventional structure base layer. On the contrary, as is shown in the category-B study, influence of bonded interface on the lifetime will provide new means for switching time control.

According to the exact numerical calculation, estimated avarage lifetime degradation due to the bonded interface is one tenth of the conventional structure. The lifetime degradation may be caused by micro-defects around bonded interface[6]. Factors which have to be considered as causes of micro-defects are lattice mismatch of wafer pairs and residual oxygen atoms at the bonded interface. According to the lifetime measurement, carried out by a microwave photoconductive decay method[7], much difference in lifetime did not observed for various wafer pairs of which surface directions are different, implying less influence on carrier lifetime. Understandings for behavior of residual oxygen atoms at bonded interface will help to stimulate further new applications of the SDB technique.

5.Conclusion

High voltage transistor and IGBT were fabricated to study SDB interface effects on minority carrier behavior. The transistor with bonded interface in the base layer showed sufficient current amplification, eventhough slight lifetime reduction due to bonded interface was observed. In the IGBT fablication, switcing time control by adjusting the interface position in an emitter layer was succesfully confirmed.

All of these results encourage new SDB technique applications for power device improvments.

References

[1]J.B.Lasky,Appl.Phys.Lett.48(1986)78
[2]T.R.Anthony,J.Appl.Phys.58(1985) p.1240
[3]R.C.Frye et.al.,Solid State Sience and Tech.,133(1986)1673
[4]A.Nakagawa et.al,'86-IEDM Tech.Digest p.122
[5]H.Ohashi et.al.'86-IEDM Tech. Digest p.210
[6]K.Furukawa et.al,'86-SSDM Ext.Abs.p.533
[7]J.H.Reynolds et.al,J.Appl.Phys 45(1974) p.2584

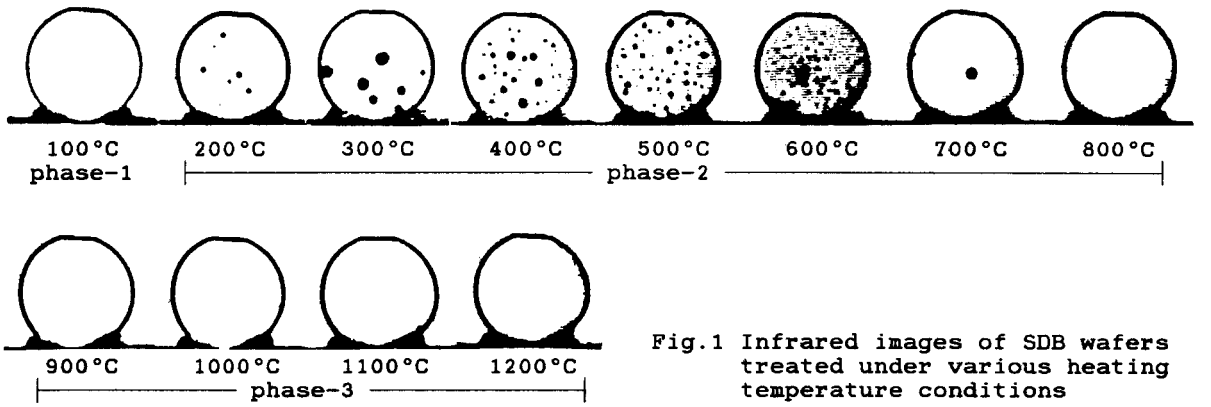

Fig.1 Infrared images of SDB wafers treated under various heating temperature conditions

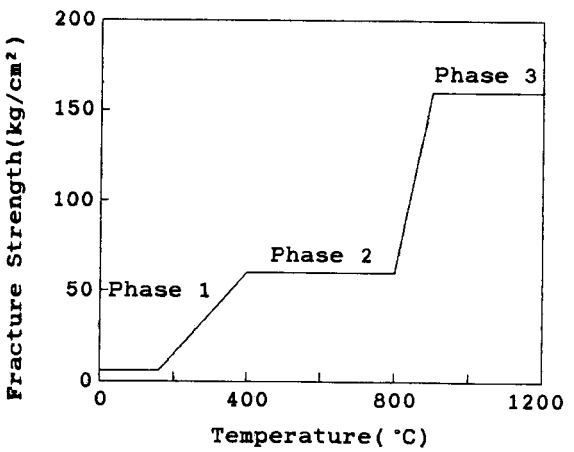

Fig.2 Fracture strength change with heating temperature change

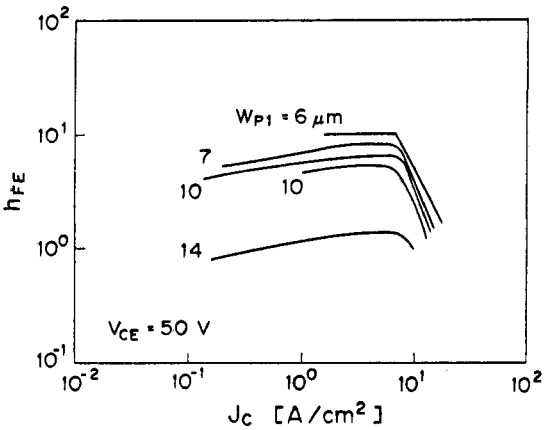

Fig.4 Dependency of h_{FE} on collector current density

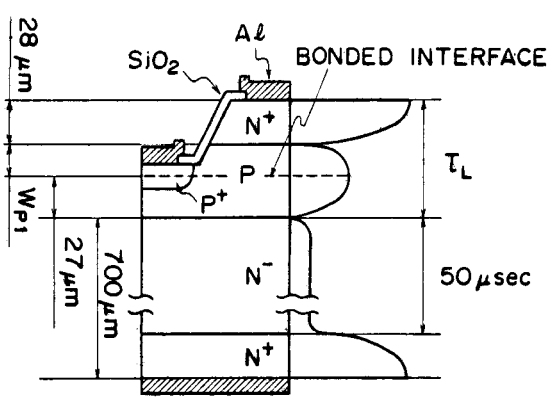

Fig.3 Cross-section, impurity profile and assumed lifetime for the simulation

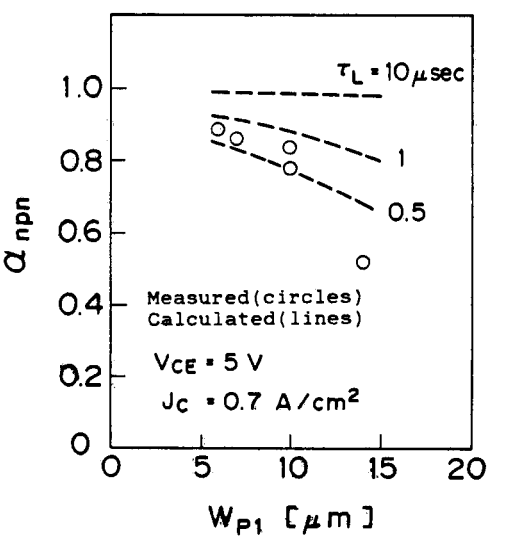

Fig.5 Alpha value vs. Wp1. Less influence of bonded interface on alpha was confirmed

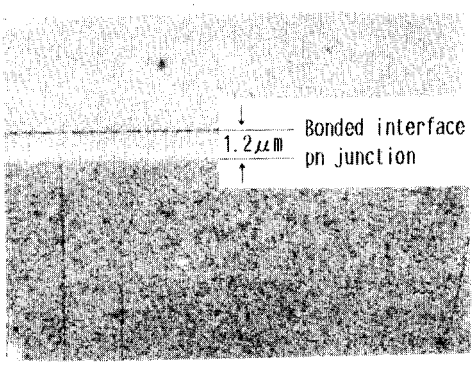

Fig.6 Observed bonded interface and pn junction by copper plating method

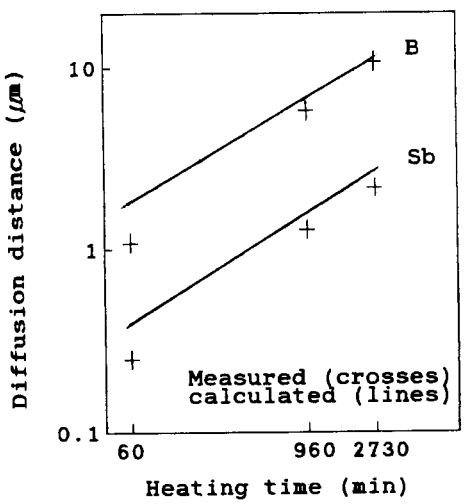

Fig.7 Relation between impurity diffusion through bonded interface and heating time

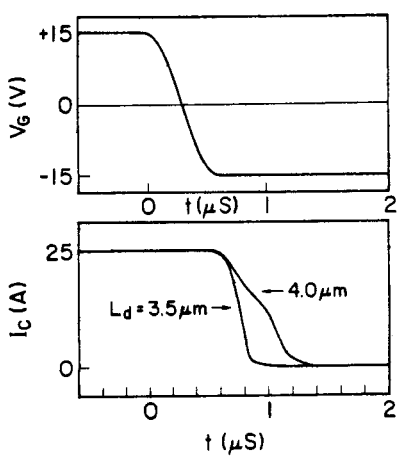

Fig.8 Typical turn-off waveforms for different diffusion distance (Ld) IGBT

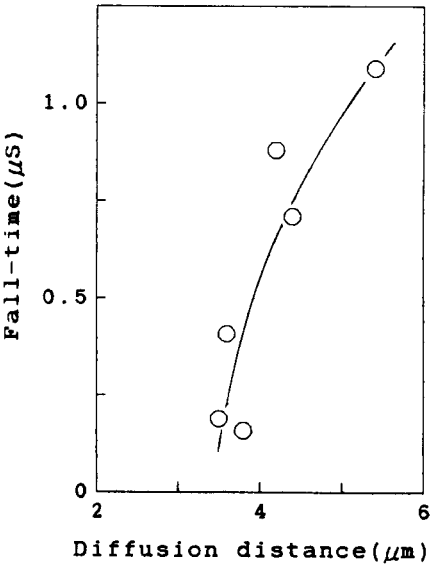

Fig.9 Fall-time vs. diffusion distance

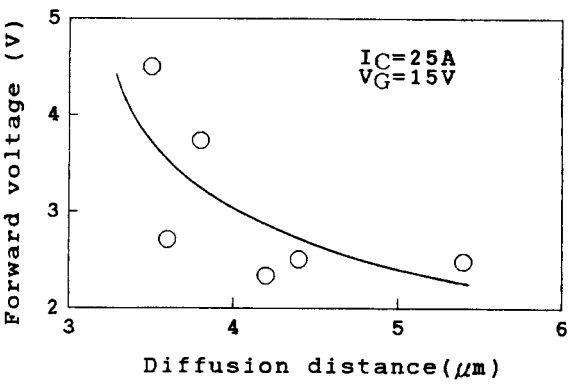

Fig.10 Forward voltage vs. diffusion distance

Table 1 SDB technique applications for power devices with pn junction

Categories		New applications
A	P+(N+) ← Junction BI N-(P-)	Impurity profile optimization
B	P+(N+) BI ← Junction N-(P-)	Carrier injection control

BI=bonded interface