10A 12V 1 chip digitally-controlled DC/DC converter IC with high resolution and high frequency DPWM

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***Abstract*— This paper introduces a 10A 12V single chip digitally-controlled DC/DC converter IC based on the low cost 0.6um BiCD process. This IC includes the digital pulse width modulator (DPWM) module with the dead-time programmability. The average time resolution is 1.22ns at the clock frequency 25MHz on 0.6um process. This resolution is as same as that for the counter-based DPWM with the clock frequency 817MHz. The chip adopted low impedance metal bump technology for reducing a parasitic interconnection resistance in the power stage. The fabricated chip achieves a low on resistance 9.7mΩ in the 20V output LDMOS (@drain current=5A, gate voltage=5V). The maximum efficiency is 86.4% at output current 5A when the input voltage, the output voltage and switching frequency and the dead-time are 12V, 1.3V, 780KHz and 15ns, respectively. The maximum voltage deviation and transient response time are 42mV and 8us, respectively in step-load (5A to 10A) transient response.**

***Keywords*— High frequency power converter, High voltage IC's, Pulse Width Modulation (PWM) and Regulation.**

I. INTRODUCTION

In recent years, researches in the area of digitally-controlled high-frequency DC-DC converter have attracted much attention. Digital control provides flexibility, programmability and opens up new control algorithm not possible in the converters with traditional analog control.

In pulse-width modulators, analog control system provides very fine resolution for output voltage adjustment. In principle, a voltage can be adjusted to any arbitrary value limited by loop gain, thermal effects and system noise levels. On the other hand, a digital control system has discrete set points resulting from the resolution of quantizing elements in the system. The output voltage resolution corresponds to the time resolution in the digital pulse-width modulators (DPWM). As the output voltage resolution is higher, the time resolution required in DPWM is higher.

Especially, in the digitally-controlled converter with high input voltage and high switching frequency, high resolution and high frequency DPWM are required to achieve precise voltage regulation.

In the DC/DC converter with synchronous rectifier, it is well known that optimum dead times achieve high converter efficiency [1]. Too long dead times result in additional losses due to the body diode conduction. Too short dead-times may result in simultaneous conduction of the main switch and the synchronous rectifier and the ineffective current from the input voltage source to the ground may flow. The dead-times programmability can make the tuning of the synchronous rectifier commutation timing easy.

With increase in clock speed of microprocessors, high efficiency, high power density, high current slew rate di/dt is strongly demanded for DC/DC converters. Precise voltage regulation under a large di/dt requires high switching frequency.

In order to improve the conversion efficiency at high switching frequency, not only the device structure of switching MOSFET but also the circuit parameters such as parasitic devices on board must be optimized. It has been pointed out that the parasitic inductance between the output MOSFET and the gate driver circuit decreases the conversion efficiency. Multi Chip Module or 1 chip solution are effective to reduce the parasitic wiring inductances [2, 3]. It was also predicted that a low impedance gate drive can reduce the mirror period in the turn-off transient, realizing ideal switching and low turn-off power loss [4]. 1 chip solution is favorable for achieving the ideal switching because the parasitic inductances are small and sufficiently low impedance gate driver circuits are easily integrated with power MOSFETs.

Up to now, the output current of 1 chip converter has been limited to a few or several amperes because the interconnection resistance becomes larger and even exceeds the on-resistance of the device itself if the size of LDMOS increases.

In this paper, we describe a 10A 12V single chip DC/DC converter IC including the DPWM module with

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the dead-time programmability based on the low cost 0.6um BiCD process.

Section II introduces the overall structure of the developed digital controller for DC/DC converter. Section III introduces the DPWM with the dead-time programmability. In the digitally-controlled converter with high input voltage and high switching frequency, high resolution, high frequency DPWM are required to achieve precise voltage regulation. The technique for realizing the average time resolution 1.22ns at the clock frequency 25MHz on 0.6um process is presented. Section IV introduces the integrated power stage driving high current. In order to reduce the interconnection resistance, the bump technology is applied to the power IC. The implementation and experimental results about 10A 12V single chip DC/DC converter IC are introduced. Conclusions from this research are drawn in Section VI.

II. DIGITAL CONTROLLER STRUCTURE

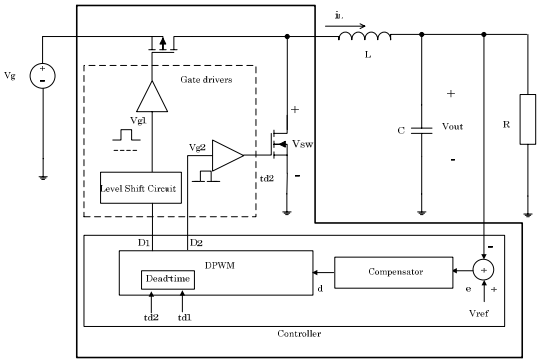


Figure1 Circuit diagram of a synchronous DC-DC buck converter with adjustable commutation dead times: Vg=12V,Vout=1.3V,max(IL)=10A

Figure 1 shows the circuit diagram of the developed synchronous DC-DC buck converter IC. The input voltage is Vg=12V, the reference voltage is Vref=1.3V, the filter parameters are L=0.67uH, C=230uF. It is composed of the flash A/D converter, control circuitry, power switches (the breakdown voltage=25V) and the drivers. The parameters of PID compensator and dead-times are loaded from external EEPROM or PC through a serial interface when the system is started or rebooted. The A/D converter is composed of only six comparators, resulting in a 7-level quantization (the least significant bit value=10mV). The error signal at the output of A/D is processed by a PID compensator, which provides the necessary duty-cycle command for the output voltage regulation.

A typical discrete-time PID control law has the form

$$d[n] = d[n-1] + a \cdot e[n] + b \cdot e[n-1] + c \cdot e[n-2] \quad (1)$$

where d[n] is the duty cycle command at discrete time n, e[n] is the error signal, a,b and c are constants.

Equation (1) indicates that an implementation of the compensator generally involves the use of digital adders and digital multipliers, which devices increases the size of controller and which tend to increase the clock frequency requirement. Look-up table architecture is applied to the compensator instead of the duty calculation including multiplication [5].

In the controller design, once the coefficients a, b and c are selected (to achieve a desired closed-loop bandwidth and adequate phase margin, for example), the produces a · e, b · e, and c · e are precomputed. Since digital error signal outputted by six comparators is a small number of values, the number of entries (a · e, b · e, and c · e) in the lookup tables is correspondingly small. The PID compensator can be accomplished in small size and in a small number of system clock cycles.

III. PWM MODULE WITH THE DEAD-TIME PROGRAMMABILITY

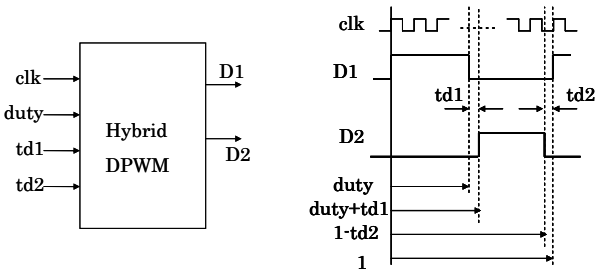


Figure2 Input and output signal entered in the DPWM Block and timing diagram

Figure 2 shows the input and output signal entered in the DPWM Block and timing diagram. In the DPWM, the dead-time programmability is provided to achieve optimum efficiency. The DPWM module with the dead-time programmability suitable for FPGA implementation has been reported [6]. But many input control signals are required to adjust the DPWM. The wiring region between the DPWM and the controlled module must occupy a large space on 0.6um process. The simple analog feedback circuit is applied to the developed DPWM.

The DPWM provides three outputs, clock signal, high side MOSFET ON/OFF signal D1 and low side MOSFET ON/OFF signal D2. The output D1 is a signal with a duty cycle determined by the input duty cycle command. The input dead-time td1 and td2 are applied to the output signal D2.

The output voltage resolution corresponds to the time resolution required in the DPWM. If the desired output voltage tolerance is 1.3 volts +/- 1% in the input voltage 12V and the switching frequency 780KHz, the time resolution and the number of bits required in the DPWM are less than 1.38 ns and more than 10 bits, respectively. In the counter-based DPWM, more than the clock frequency 725MHz is required. Although clock rates of

that magnitude, or higher, can be produced in IC devices, they require more advanced process than 0.6um process and driving power that is likely to exceed practical values in most DC/DC conversion products. The hybrid DPWM[7] are introduced to provide the high resolution without the need for a very high clock frequency.

Figure 3 shows the developed hybrid DPWM with the dead-time programmability. The developed 10-bit DPWM is composed of 5-bit counter and 5-bit delay line. The clock period, Tclk is divided into 32 time steps by 5-bit delay line as shown in figure 3. The required clock frequency, 22.7MHz is 32 times smaller than that for the equivalent counter.

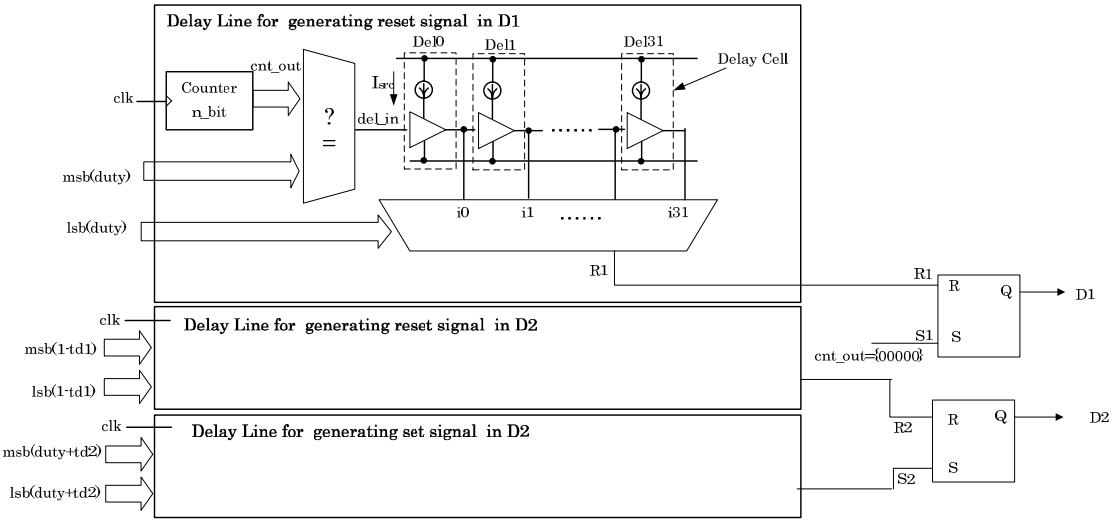


Figure 3 Developed hybrid DPWM with the dead-time programmability

This DPWM is composed of 3 delay lines with 32:1 multiplexer and two SR latches. The delay lines are configured with the same delay cell so that the total propagation delay time of delay cells matches the period of clock. The propagation time in the delay cell can be controlled by the supply current Isrc in figure 3. The supply current Isrc is depended on the clock frequency.

The counter provides the most significant bit(msb) portion of the signal command, for example, the duty cycle command and the delay line provides the least significant bit(lsb) portion. Figure 4 shows a timing diagram implemented with the duty cycle command for the DPWM in case that the duty is 00101_00001. The counter counts at each clock period of input, clk. The output, D1, is set at the zero value of the counter(S1="00000"). The output of the counter is compared with 5 most significant bits of the input duty cycle command, msb(duty), "00101" and the comparator outputs the signal del_in. The signal del_in is propagated through the delay line. The output of each delay cell is tapped out and connected to a 32:1 multiplexer. The propagated signals, i0-i31, in the output of the delay cells, Del0-Del31 are shown in figure 3. The selection of the multiplexer output, "i1" is made by observing the least significant portion of the input duty cycle command, lsb(duty),"00001" and "i1" is connected to R. The signal R resets D1. It is important that the required clock frequency is lower as compared to the counter-based DPWM with the same resolution.

The leading and trailing edge of the low side MOSFET ON signal D2 is generated in the same way as the reset signal of the duty cycle command. The setting time resolution for adjusting dead-time is the same as the time resolution of duty cycle command.

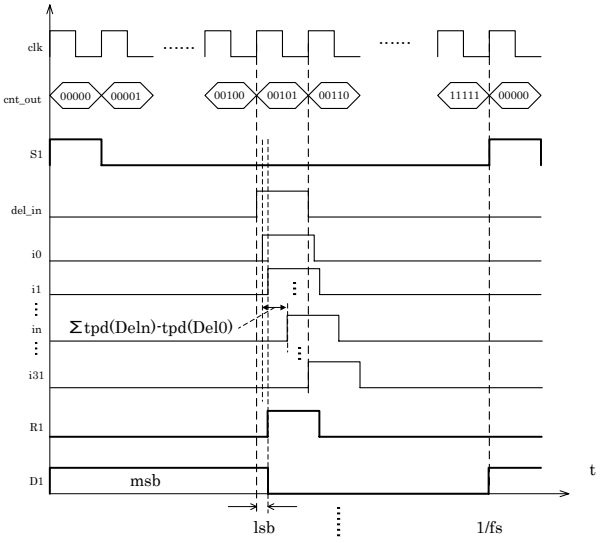


Figure 4 Timing diagram implemented with the duty cycle command for the DPWM in case that the duty is 00101_00001.

In the developed DPWM, the digital dither technique is additionally used to improve the time resolution. The LC output filter averages any pulse train that is fed into it. If the output pulse width from the DPWM is increased only once every eight switching periods by the equivalent of the minimum step time, the temporally-smoothed value of the pulse train will be increased by an amount equal to (1/8)*resolution of the minimum step time. The effective time resolution 1.38ns/8=172.5ps is obtained in the DPWM.

Figure 5 shows the measured propagation delay summation of delay cells from Del0 to Deln, for the different clock frequency. The lines are the ideal summation of minimum step time for the each clock frequency (fclk), (Tclk)/32*n. As shown in figure 6, the average resolution is 1.22ns at the clock frequency 25MHz in the developed hybrid DPWM. This resolution is as same as that for the counter-based DPWM with the clock frequency 817MHz.

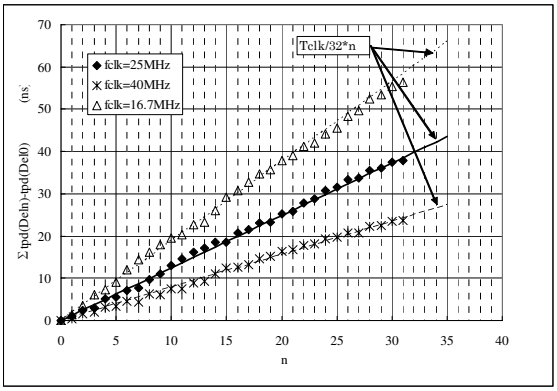


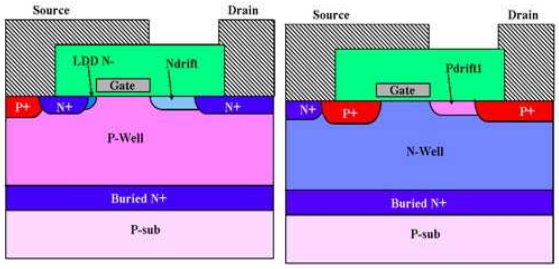
Figure 5 Measured propagation delay summation of delay cells from Del0 to Deln. The lines are the ideal summation of minimum step time for the each clock frequency (fclk), (Tclk)/32*n.

IV. Integrated Power Stage Driving High Output Current

A. Device Structures

Figure 6 shows a cross-sectional view of 20V output LDMOS devices based on the low cost 0.6um BiCD process. The capacitance between gate and drain is depended on the switching loss.

The device is fabricated in the p-well so that gate drain capacitance is minimized. The buried N+ layer is electrically connected to the source electrode to reduce the coupling between the drain and the substrate. Three metal layers with a 3um thick top metal layer are utilized. The drift region is self-aligned to the gate electrode in order to reduce the parasitic gate-drain capacitance which affects the switching loss. Additionally, the source electrode extended over the gate poly-silicon is effective to reduce the parasitic gate-drain capacitance. In case of the optimized Nch LDMOS, the breakdown voltage, the threshold voltage and the specific on-resistance is 25.0V, 0.85V and 23.1mΩmm2, respectively.



(a)Nch LDMOS (b)Pch LDMOS

Figure.6 Cross-sectional view of 20V output power devices based on the low cost 0.6um BiCD process.

B. Power IC Using Bump Technology

The on resistance of lateral MOSFETs with wire bonding deteriorates considerably with increase in device size due to the parasitic resistance. Interconnection resistance not only increases overall device resistance but also causes debiasing effect in active cells [8]. In order to reduce the interconnection resistance, we have adopted wafer bumping technology [9].

Figure 7 shows the assembled image, the layout of the top metal in IC and the Cu pattern on a printed circuit board (PCB). The chip is attached to the intermediate PCB through bump balls.

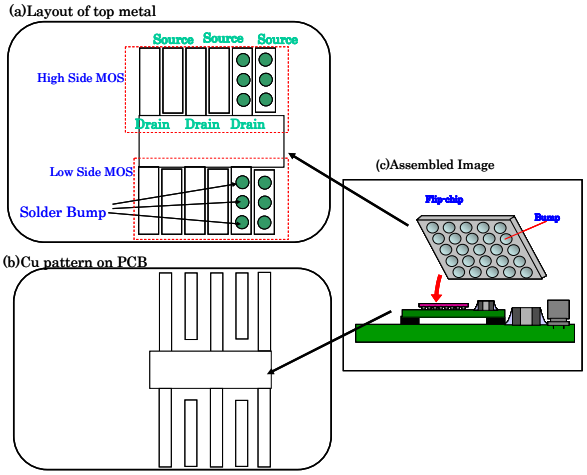


Figure.7 Assembled image, layout of top metal in IC and Cu pattern on printed circuit board (PCB). The drain and the source bumps are electrically connected by parallel running thick Cu metals in the PCB

We have adopted Pch LDMOS for high side switching device in DC/DC converter. The source and drain metals are alternately formed and the drain metals of Pch LDMOS and Nch LDMOS are connected each other. The PCB connects drain and source bumps by parallel running thick Cu metals. The resistance that current laterally flows in the top metal is made as small as possible.

When the input voltage and the output voltage are 12V and 1.3V, respectively, the on time of the low side MOSFET is about 90% in a switching period. It is important to reduce the on resistance of the low side Nch LDMOS. Figure 8 shows the measured output characteristics of a large area Nch LDMOS (the effective area 3.6mm2). The on resistance is 9.7mΩ(@drain current=5A, gate voltage=5V). We have achieved that the value of on resistance is below 10mΩ in 20V LDMOS of Pw IC.

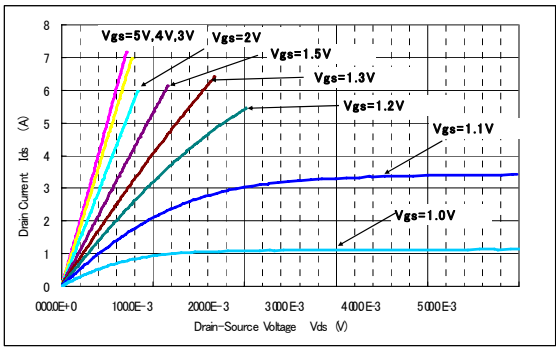


Figure.8 Output characteristics of a large area device (the effective area 3.6mm2).

V. Implementation and Results

Figure 9 shows a die photo of the fabricated 10A 12V 1chip DC/DC converter IC based on the low cost 0.6um BiCD process. The A/D converter, control circuitry, power switches (the breakdown voltage=25V) and the drivers are integrated on the same die.

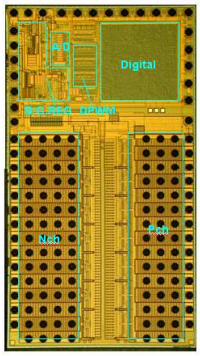


Figure 9 Micrograph of the fabricated 10A 12V 1chip DC/DC converter IC based on the low cost 0.6um BiCD process

Figure 10 shows the measured output voltage ripple, w hen the input voltage, the output voltage, switching frequency and the load current are 12V, 1.3V, 780KHz and 0A, respectively. As shown in the figure 10, the output voltage ripple is suppressed to below 11mV. The developed DPWM achieves high resolution and high frequency.

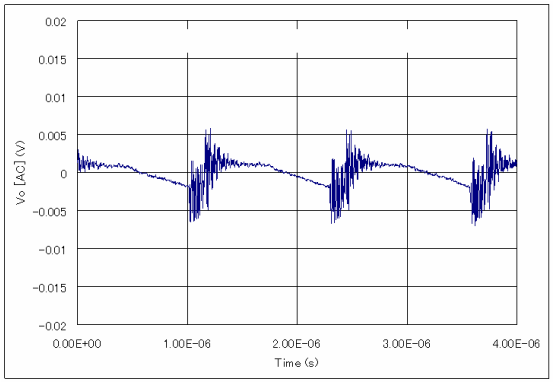


Figure 10 Measured output voltage ripple: Vg=12V, Vout=1.3V, fsw=780 KHz, IL=0A

Figure 11 shows the measured converter efficiency as functions of the dead time td1 in figure 2. It is easy to adjust the dead-time by changing the stored parameter. The clock frequency and switching frequency are 25MHz and 780KHz, respectively. The maximum efficiency is achieved at td1=11.3ns. It is more important to optimize the dead-time in the higher switching frequency.

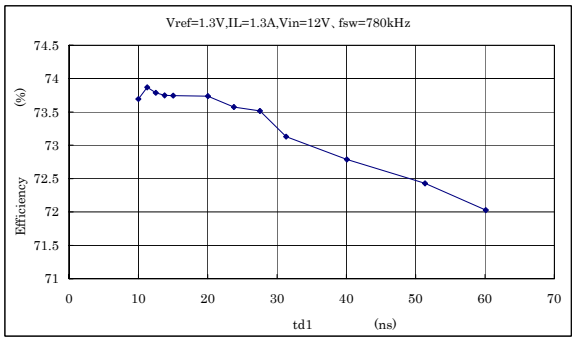


Figure 11 Measured converter efficiency as functions of the dead time td1:Vg=12V,Vout=1.3V,IL=1.3A

Figure 12 shows the measured efficiency of fabricated 1chip DC/DC converter IC when the input voltage, the output voltage and switching frequency and the dead-time(td1,td2) are 12V, 1.3V , 780KHz and 15ns, respectively. The maximum efficiency is 86.4% at output current 5A. The fabricated chip has accomplished the high efficiency.

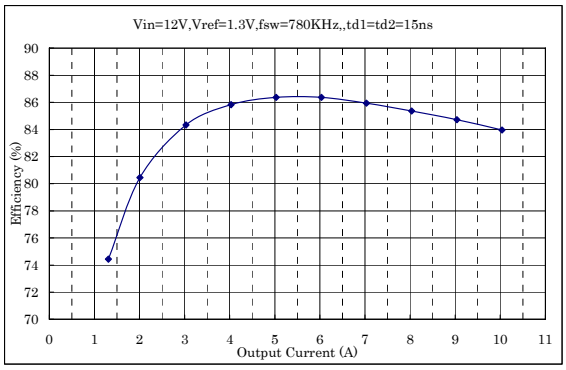


Figure 12 Measured efficiency of fabricated 1chip DC/DC converter IC when the input voltage, the output voltage and switching frequency and the dead-time(td1,td2) are 12V, 1.3V , 780KHz and 15ns, respectively.

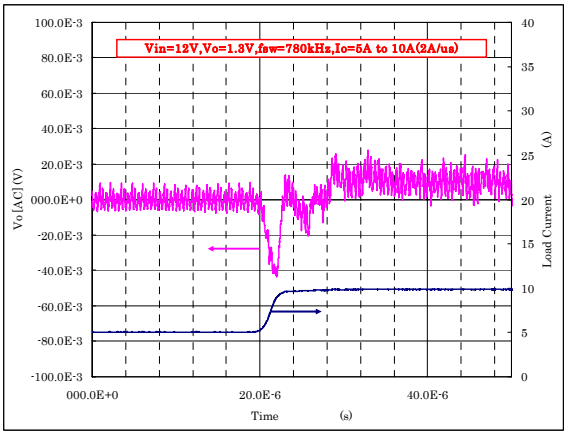


Figure 13 Experimental step-load(5A->10A)transient response. The maximum voltage deviation and transient response time are 42mV and 8us, respectively.

Figure 13 shows the experimental step-load(5A->10A)transient response. The maximum voltage deviation and transient response time are 42mV and 8us, respectively. The transient response of the developed chip is equivalent to that of analog controlled IC.

VI CONCLUSIONS

This paper introduces a 10A 12V single chip digitally-controlled DC/DC converter IC based on the low cost 0.6um BiCD process. This IC includes the digital pulse width modulator (DPWM) module with the dead-time programmability. The average time resolution is 1.22ns at the clock frequency 25MHz on 0.6um process. This resolution is as same as that for the counter-based DPWM with the clock frequency 817MHz. The chip adopted low impedance metal bump technology for reducing a parasitic interconnection resistance in the power stage. The fabricated chip achieves a low on resistance 9.7mΩ in the 20V output LDMOS (@drain current=5A, gate voltage=5V). The maximum efficiency is 86.4% at output current 5A when the input voltage, the output voltage and switching frequency and the dead-time are 12V, 1.3V, 780KHz and 15ns, respectively. The maximum voltage deviation and transient response time are 42mV and 8us, respectively in step-load (5A to 10A) transient response.

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