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High Voltage SOI Technology (Invited Paper)

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1. Introduction

A SOI layer with a thick buried oxide is of great interest for high voltage power IC applications[1]. The reasons are: (1)dielectric device isolation can be achieved in a reasonable cost by trench technique; (2) a high breakdown voltage is obtained on an SOI with a thick buried oxide, because a large share of the applied voltage can be sustained by the buried oxide. For example, 600V devices can be realized on 14μm silicon on 3μm buried oxide. This paper reviews recent advances on high voltage SOI technology.

2. Device Breakdown Voltage

First, we show how device breakdown voltage depends on SOI thickness and/or buried oxide thickness. For simplicity, we deal with SOI diodes.

2.1 Uniformly doped SOI diode

Device breakdown voltages on SOI is generally determined either by the vertical 1-D MOS diode or by the lateral diode structure (SOI-Resurf) as illustrated in Fig.1. It is widely recognized that SOI device breakdown voltage is determined by so-called Resurf concept[2,3]. However, most of the breakdown voltages of the interesting SOI devices are determined by the breakdown voltage of the 1-D MOS diode[4], consisting of n^+/n^-/oxide/substrate. Figure 2 shows the diode breakdown voltage on 10μm thick SOI as a function of the impurity dose in the SOI layer with buried oxide thickness as a parameter. Figure 3 compares the both breakdown voltages of the 1-D MOS diode and the SOI diode. It is seen that the 1-D n^+/n^-/oxide/substrate diode breakdown voltage substantially determines SOI diode breakdown voltage. The 1-D diode breakdown voltage depends on the impurity dose of the SOI layer and increases with the increase in the impurity because the n^- layer impurity concentration under the n^+ layer increases and a larger voltage is sustained by the buried oxide.

The situation is quite different for the cases where the buried oxide thickness is over 5μm as seen in Fig.3. Even if the impurity dose in the n^- SOI layer is optimized, the SOI diode breakdown voltage cannot reach the ideal 1-D MOS diode breakdown voltage and is substantially limited by the lateral device structure.

2.2 Optimized lateral SOI diode

There are following two cases where SOI diodes breakdown voltages are determined by lateral device structures (SOI-Resurf).

1: SOI layer is thinner than a few hundred nanometers.

2: SOI substrates whose buried oxides are thicker than 5μm

Case 1: Merchant et al.[5] showed that the SOI diode breakdown voltage is significantly enhanced, if the SOI layer thickness is very thin such as 0.1μm. For such thin SOI diodes, the lateral impurity distribution have to be optimized. Merchant et al. proposed a linearly graded impurity profile of the n^- SOI layer for an optimum $n^+n^-p^+$ lateral diode. The authors found from exact 2-D simulations that the ideal profile for lateral diode is a near tangent function as shown in Fig.4(a). The important points are that the p layer impurity profile should be graded and that the linearly graded portion is terminated by the exponentially increasing ending portions. By using this profile, a 5000V lateral diode was predicted to be realized on 0.1μm SOI on 600μm thick quartz substrate . A completely uniform lateral electric field is realized at 5000V(see Fig.4(b)).

Case 2: The 1-D MOS diode breakdown voltage cannot be realized simply by optimizing the n^- layer impurity concentration, if the buried oxide thickness exceeds 5μm and the n^- layer is uniformly doped. A practical mean is to use multiple n type diffusion layers (Resurf diffusion layers) to make a proper impurity profile gradient. A guide for this is the proposed ideal profile for the very thin SOI case.

3. High Voltage Power ICs on SOI

A whole power system can be integrated on a single silicon chip if high voltage power devices can be integrated with analog and digital circuits. Key technologies are CMOS analog circuits and high speed high voltage output devices. IGBTs are suitable for high voltage large current output devices.

3.1 Lateral IGBTs on SOI

The switching speed of IGBTs improves as the SOI thickness decreases, because carrier lifetime is effectively decreased by a large carrier recombination at the silicon dioxide interfaces[4]. High voltage IGBTs, fabricated on less than 5μm thick SOI, automatically exhibits high switching speeds. This means that low cost power ICs can be fabricated by utilizing conventional CMOS processes without special lifetime control processes.

3.2. High Temperature Operation[6]

The leakage current of SOI devices simply decreases in proportion to the thickness of the SOI layer. It was experimentally verified that IGBTs can be operated at a switching frequency of 20kHz at more than 200℃, if they are fabricated on 1.5μm SOI/3μm oxide. The breakdown voltage of the IGBTs were 440V.

4. Conclusion

High voltage SOI technology has a possibility to integrate high voltage power devices and LSI circuits including MPUs. This will produce vast application fields.

References:

[1]A.Nakagawa et al.,1992 IEEE IEDM Tech Digest, p.229
[2]A.Nakagawa, Proc. of ISPSD'91, p.16
[3]Y.S.Huang et al., Proc. of ISPSD'91, p.27
[4]I.Omura et al., Proc. of ISPSD'93, p.248
[5]S.Merchant et al., Proc. of ISPSD'91, p.31
[6]A.Nakagawa et al., 1993 IEEE IEDM Tech. Digest, p.687

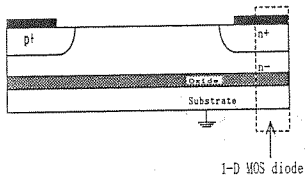
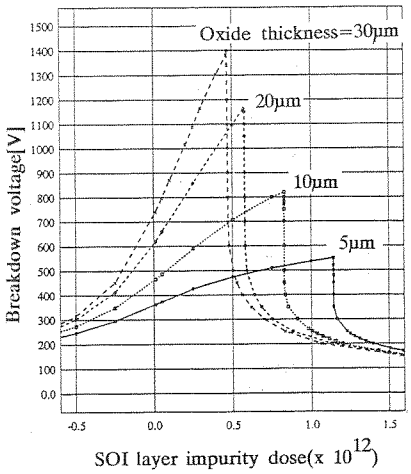


Fig.1 SOI diode structure and 1-D MOS diode



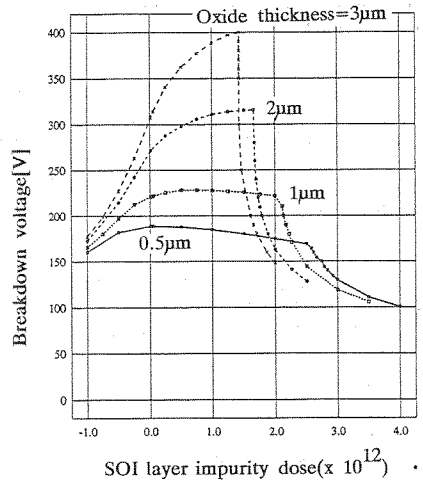


Fig.2 10μm thick SOI diode breakdown voltage as a function of SOI layer impurity dose with oxide thickness as a parameter.
Negative dose means p type.

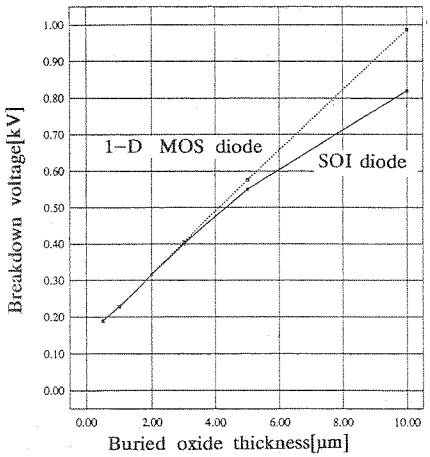


Fig.3 Comparison of breakdown voltages of 10μm thick SOI diode and 1-D MOS diode.

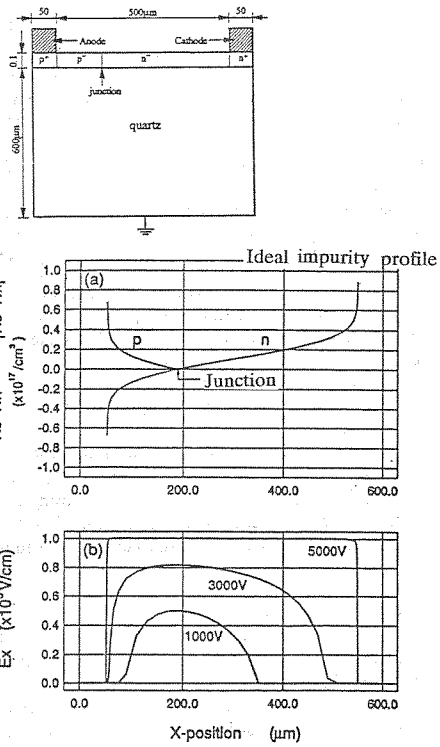


Fig.4 (a)Ideal impurity profile for very thin SOI diode.
(b)Calculated electric field distribution for 0.1μm thick SOI diode on quartz substrate.