# APPLICATION OF DIELECTRIC ISOLATION TECHNIQUE BASED ON SILICON WAFER DIRECT-BONDING TO POWER ICs

Akio Nakagawa, Kazuyoshi Furukawa, Yoshihiro Yamaguchi
Katsujiro Tanzawa, Hiromichi Ohashi

Toshiba Research & Development Center,
1 Komukai Toshibacho Saiwai-ku Kawasaki, 210, JAPAN

## ABSTRACT

Application of silicon wafer direct bonding to dielectrically isolated 500V power ICs is discussed. The three developed key techniques are 1) high speed 500V lateral IGBTs(Bipolar-Mode MOSFETs) as output devices, 2) isolation technique for integrating junction isolated bipolar logics in a dielectrically isolated silicon island, and 3) 500V SIPOS resistive field plates, preventing breakdown voltage reduction due to overlying metal interconnection.

## INTRODUCTION

Bipolar-Mode MOSFETs(1)(IGBTs(2,3)) have been recognized as excellent high voltage power devices, because of the MOS gate controlled large current capability and fast switching speed. It was experimentally(4) and theoretically(5) shown that a vertical IGBT safe operating area (allowable maximum power dissipation) can exceed the bipolar transistor theoretical limit ($2x10^5 W/cm^2$). Large current devices, such as 400A,500V and 300A,1000V(6), are now available on the market. Lateral devices(7,8) are also attractive as high voltage output devices for power ICs.

This paper describes key techniques for realizing dielectrically isolated high voltage power ICs. These are 1) dielectrically isolated 500V high speed lateral Bipolar-Mode MOSFETs(IGBTs) for output power devices, 2) novel isolation technique, based on silicon wafer direct-bonding, being capable of integrating junction isolated bipolar and CMOS logics and dielectrically isolated high voltage IGBTs, and 3) a SIPOS resistive field plate, effective for shielding external electric field influence on the device breakdown voltage.

## LATERAL BIPOLAR-MODE MOSFET(IGBT)

Figure 1 shows a developed 500V lateral IGBT structure formed only by diffusions on a dielectrically isolated $P^-$ silicon island. Figure 2 shows an overview of the developed LIGBT, which was formed on a 0.9mm$^2$ dielectrically isolated silicon island. It was experimentally found(9) that a lateral N channel IGBT, formed on a P type silicon island, is superior to the counterpart N channel device on an N type silicon island. The reason is the following: 1)In the N channel device formed on a $P^-$ silicon island, the depletion layer develops beneath the N-buffer layer, ie, in the $P^-$ layer, where the largest excess carrier density exists in the device. 2) The $P^-$ layer is electrically connected to the source electrode without any electrical barriers. Thus, most of the stored carriers in the $P^-$ layer are swept away automatically by the depletion layer development in the turn-off transient. This results in a small tail current and resultant fast switching speed.

The developed device structure(Fig.1) is similar to that for the double gate lateral IGBT(Fig.3), presented at 1988 IEDM(9). Double gate operation was shown to be effective for improving switching speed. However, it was found that single gate operation of an optimized double gate device, with the second gate being shorted to the drain, exibited sufficiently high speed switching. For example, Figure 4 shows a typical switching waveform for 250nsec fall-time and 200mA drain current(0.43mm$^2$ active region). The reason is that the additional $N^+$ diffusion layer in a P-drain layer acts as an electron absorber in a high injection condition, realizing the same effects as an anode short. Moreover, this structure is better than the anode short because the forward voltage can be low even for a low current density level. Figure 5 shows a trade-off relation between the drain current for 3V forward voltage vs. fall-time. It is seen that an N type diffusion layer in a P-drain and a high concentration N-buffer are both effective for short fall-time. 200nsec fall-time was realized with 0.075Ωcm$^2$ Ron area product for 40A/cm$^2$ current density(drain current over active region). 0.035Ωcm$^2$ was attained with 80A/cm$^2$ current density when a relatively long 600nsec fall-time was acceptable.

## MERGER OF DIELECTRIC ISOLATION AND JUNCTION ISOLATION

Silicon Wafer Direct-Bonding(SDB) technique was tested and applied to acctual devices independently by two groups in 1985(14) and 1986(11,12,13). In this section, application of dielectric isolation technique, based on silicon wafer direct-bonding(DISDB), to power ICs is described.

The dielectrically isolated P type silicon island is advantageous to merge dielectric isolation(DI) and semi-well junction isolation(JI)(14) to integrate both BiCMOS logics and high voltage lateral IGBTs. Figure 6 shows the proposed structure, where low voltage bipolar devices are junction-isolated by well etching and buried $N^+$ diffusion layers. Figure 7 shows the developed processes for realizing merger of dielectric isolation and junction isolation.

1)After a $P^+$ diffusion on the mirror surface of a high resistivity P type bulk wafer and thermal oxidation, this wafer is bonded to a substrate wafer.

2) Well etching and an $N^+$ diffusion on the etched well surfaces are carried out after wafer thinning and flattening.

3) Then, V-groove formation and successive $P^+$ diffusion on the V-groove surfaces are accomplished.

4) $N^-$ layer epitaxial growth on the etched wells and poly-silicon layer growth on the oxidized V-grooves are simultaneously implemented.

Figure 8 shows a cross sectional image for simultaneously grown epitaxial and poly-silicon layers. BiCMOS logics can be formed on these wells after flattening the wafer.

Dielectric isolation is used only where it is necessary to isolate high voltage bipolar devices, such as IGBTs or thyristors. Thus, the V-groove area for dielectric isolation can be minimized to occupy a small portion of the total chip area.

## SIPOS RESISTIVE FIELD PLATES

Another important technique for high voltage ICs is a junction termination and passivation technique, which should not be affected by overlying interconnection metal layers. SIPOS resistive field plate(RFP), combined with an $N^-$ drift layer (Resurf) and a metal field plate, has been developed for high voltage ICs. An inserted figure in Fig.9 shows a cross section view of the developed Junction termination structure. A high resistivity SIPOS layer is electrically connected to the gate polycrystaline silicon and the drain metal, serving as a resistive field plate(RFP). A part of the drain metal layer directly contacting the SIPOS layer serves as a metal field plate(MFP).

Breakdown voltage and electric field shielding effect for the resistive field plate was experimentally examined by fabricating devices with and without overlying drain interconnection metal layers over the SIPOS layer(diode and LDMOS). It can be confirmed from Fig. 9 that breakdown voltage was not reduced by overlying interconnection metal layers. It was shown that 500V breakdown voltage can be obtained for more than 60$\mu$m drift layer length even with overlying metal interconnection layers.

## CONCLUSION

Key techniques for dielectrically isolated high voltage power ICs have been developed. These are 1) novel isolation techniques, merging DI and JI for junction isolated BiCMOS logics. 2) 500V high speed lateral Bipolar-Mode MOSFETs(IGBTs) for output power devices, and 3) a

SIPOS resistive field plate for stable high breakdown voltage. These techniques enable more than 500V intelligent power ICs.


REFERENCES

(1)A.Nakagawa et al, Ext.Abs.of 16th ISSDM, p.309 (1984)
(2)B.J.Baliga et al, 1982 IEEE IEDM Tech.Dig.,p.264.
(3)A.M.Goodman et al, 1983 IEEE IEDM Tech.Dig.,p.79.
(4)A.Nakagawa et al, IEEE Trans. Electron Devices, ED-34,p.351(1987).
(5)A.Nakagawa, 1988 IEEE PESC Record, p.84.
(6)Toshiba data sheet.
(7)M.R.Simpson et al, 1985 IEEE IEDM Tech.Dig.,p.740.
(8)A.L.Robinson et al, 1985 IEEE IEDM Tech.Dig.,p.744.
(9)A.Nakagawa et al, 1988 IEEE IEDM Tech. Dig.,p.817.
(10)J.B.Lasky et al, 1985 IEEE IEDM Tech. Dig.,p.684.
(11)Y.Ohata et al, 1986 IEEE Custum Integ. Circ. Conf.,p.443.
(12)A.Nakagawa, 1986 IEEE IEDM Tech. Dig.,p.122.
(13)H.Ohashi et al, 1986 IEEE IEDM Tech Dig.,p210.
(14)T.Okabe et al, Proc. of 1988 ISPSD, p.96.



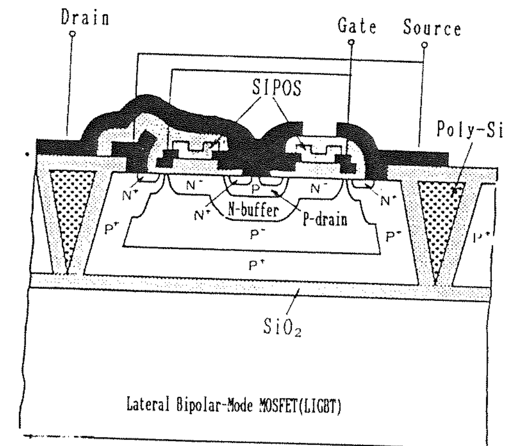




Fig.1 500V lateral Bipolar-Mode MOSFET(IGBT)

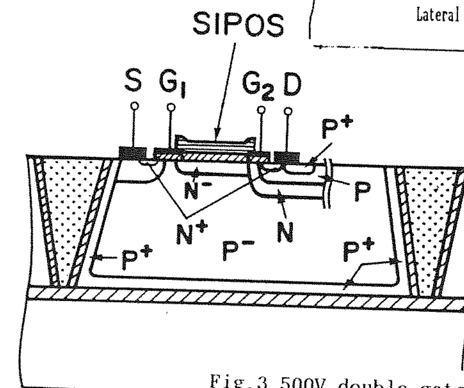



Fig.3 500V double gate LIGBT.

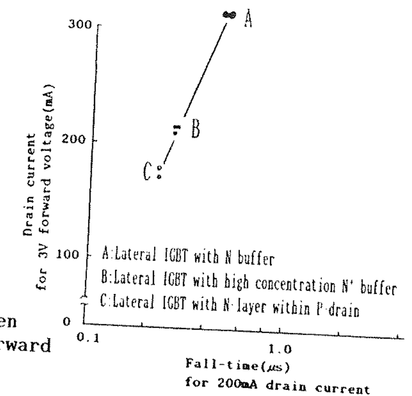



Fig.5 Trade-off relation between the drain current for 3V forward voltage vs. fall-time.

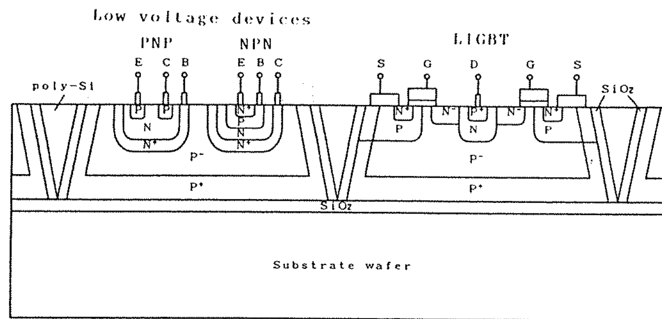
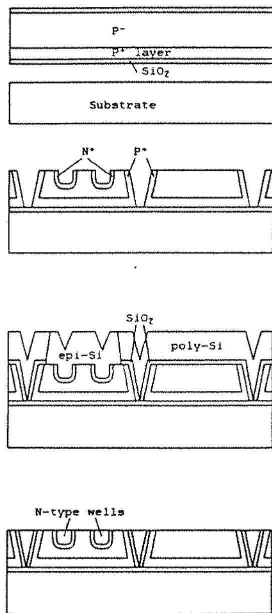



Fig.6 Proposed IC structure for
Merged JI and DI.



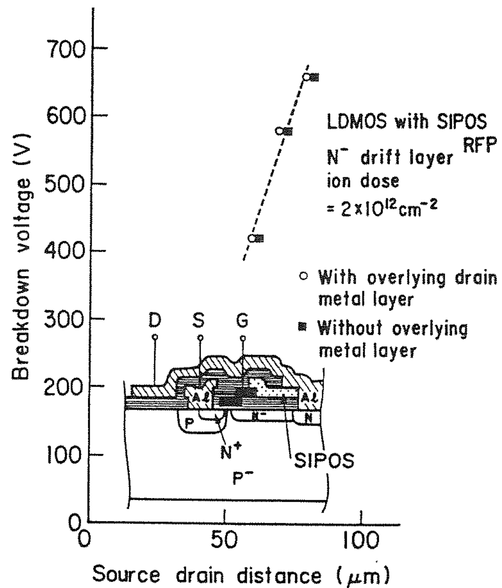




Fig.7
Developed merger
process for JI and DI.

Fig.9 Breakdown voltage comparison
between devices with and without
overlying metal interconnection layers.



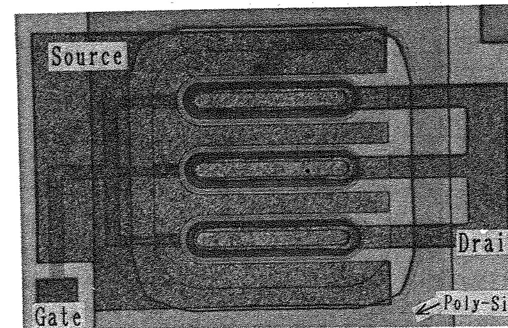



Fig.2 Over view of dielectrically
isolated LIGBT.

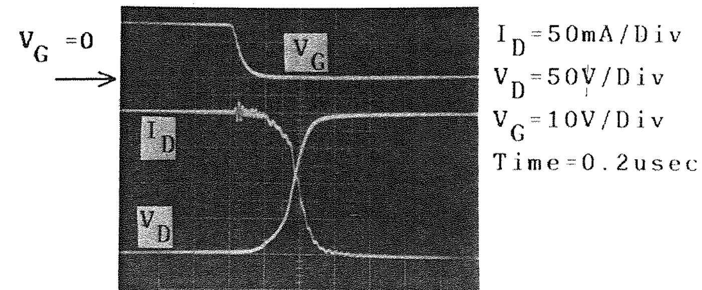



Fig.4 Typical turn-off waveform.

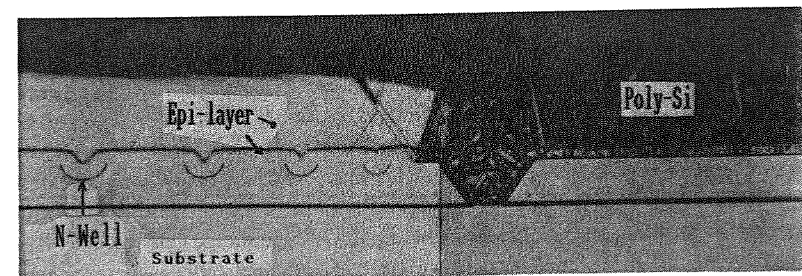



Fig.8 Cross-sectional image of
simultaneously grown epitaxial
and poly-silicon layers.