10A 12V 1 chip DC/DC converter IC using bump technology

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Abstract — **In this paper, we demonstrate high frequency and 10A operation of 1 chip DC/DC converter. The chip adopted low impedance metal bump technology and a high speed gate driving technique for large LDMOS, what we call "distributed driver circuit". The fabricated chip achieves the switching time 3ns at load current 10A and high efficiency 88.9% for the input voltage, the output voltage and switching frequency of 12V, 1.3V and 780kHz, respectively.**

Index Terms — **Power device, DC/DC converter, LDMOS.**

I. Introduction

With recent increase in clock speed of microprocessors, high efficiency, high power density, high current slew rate di/dt is strongly demanded for DC/DC converters. In order to improve the conversion efficiency, Multi Chip Module has been proposed to reduce parasitic inductances[1,2].MCM consists of a driver IC and two power MOSFETs(Low Side and High side) in one package. Not only small size but also high frequency operation is simultaneously realized.

In the case of 1chip DC/DC converters, although the parasitic inductances are negligible and package size can be even smaller, the output current of 1 chip converter has been limited to several amperes because of the large on-resistance of output lateral devices. In this paper, we demonstrate 10A operation and high speed switching in one-chip converter by applying a metal interconnect with bump technology and adopting distributed driver circuit layout.

II. Device Structures

Figure 1 shows a cross-sectional view of 20V output LDMOS devices based on the low cost 0.6um BiCD process. The device is fabricated in the p-well so that the gate drain capacitance is minimized. The buried N+ layer is electrically connected to the source electrode to reduce the coupling between the drain and the substrate. Three metal layers with a 3um thick top metal are utilized. The drift region is self-aligned to the gate electrode in order to reduce the parasitic gate-drain capacitance which affects the switching power loss. In case of N-ch LDMOS in figure 1(a), the breakdown voltage degrades as the drain current increases, and the I-V curves show snapback characteristics. We have applied 2-step shallow n-implant structure (Adaptive Resurf) to the N-ch LDMOS as shown in figure 1(b)[3]. Figure 2 shows the measured I-V characteristics of the fabricated N-ch LDMOS. The applied gate-source voltage is 5V and the channel width is 157um. The 2-step shallow n-implant structure improves the on-state breakdown voltage of 25V, as shown in figure 2. The measured values of the device characteristics are listed in Table I. The optimized breakdown voltage, on-state voltage, threshold voltage and specific on-resistance is 24.4V, 25.0V, 0.85V and 23.6mΩmm^2, respectively.

III. Power IC Using Bump Technology

The on-resistance of lateral MOSFETs with bonded wires deteriorates considerably with increasing device size due to the parasitic resistances. The interconnect resistance, including that of bonding wires, not only increases overall device resistance but also causes a debiasing effect in active cells. In order to reduce the interconnect resistance, we have adopted bump technology.

Figure 3 shows the assembled image, the layout of the top metal in IC and the Cu pattern on a printed circuit board (PCB). The chip is attached to the intermediate PCB through bump balls. We have adopted P-ch LDMOS for high side switching device in DC/DC converter. The source and drain metals are alternately formed and the drain metals of P-ch LDMOS and N-ch LDMOS are electrically connected. The drain and the source bumps are electrically connected by parallel running thick Cu metals in the PCB. The resistance between two adjacent bumps in the top metal is made as small as possible.

Figure 4 shows the output characteristics of a large area N-ch LDMOS (the effective area 3.6mm^2). The on resistance is 9.7mΩ when the drain current and the gate voltage is 5A and 5V, respectively.

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IV. Distributed Driver Circuit Layout

When the area of LDMOS is large, the gate current between the gate driver and LDMOS becomes increasingly large. The whole LDMOS device doesn't uniformly turn-on or -off because the gate drive delay may occur within the large LDMOS. The parasitic resistances and capacitances of the gate interconnects induce the gate signal delay. Especially in the turn-off period, the gate delay may cause significant non-uniform switching because of the small threshold voltage (0.85V). Thus, we propose "distributed driver circuit layout."

Figure 5 compares the distributed driver circuit layout with the conventional concentrated driver circuit layout. In the concentrated driver circuit layout (a), a large gate charging or discharging current flows in one large gate driver signal bus line and the parasitic resistance of the signal bus line causes non-uniform gate voltage distribution. In the distributed driver circuit layout (b), a number of gate driver circuits are located beside the segmented LDMOS and the length of the gate charging or discharging current flow path is made as short as possible. The current magnitude of the signal bus line is substantially small, and does not cause the gate signal delay.

Table II shows the simulated switching loss of the distributed driver circuit and the concentrated driver circuit under resistive switching when the input voltage, the load resistance and switching frequency is 12V, 1.2ohm and 780 kHz, respectively. The simulated condition is that the channel width of the gate driving MOSFET in the concentrated driver circuit is equal to the total channel width of the gate driving MOSFETs in the distributed driver circuit. As shown in table II, the turn off loss of distributed driver circuit is reduced to 54% of that of concentrated driver circuit.

Figure 6 shows the micrograph of fabricated chip based on the low cost 0.6um process. The chip size is 20.3mm^2. A number of driver circuits are placed between N-ch and P-ch LDMOS.

Figure 7 shows the equivalent circuit of the fabricated chip. This circuit is consisted of driver circuits for N-ch and P-ch LDMOS, level shift circuit and a regulator circuit which generates 5V and VIN1-5V (VIN1: input voltage) for driver circuits.

Figure 8 shows the switching characteristics of the fabricated chip at the condition of an inductance, 2uH. The rise time of switching node is 3ns. The fabricated devices in the one-chip DC/DC converter indicates high speed and high current switching capability of 10A .

Figure 9 shows the measured dependence of efficiency on output current, when the input voltage Vin, the output voltage Vout and switching frequency fsw is 12V, 1.3V and 780kHz, respectively. The maximum efficiency is 88.9% at output current 5A. The fabricated chip has accomplished the high efficiency.

V. Conclusion

In this paper, we demonstrated high speed 10A DCDC converter by applying a metal interconnect with bump technology and adopting distributed driver circuit layout.

Acknowledgement

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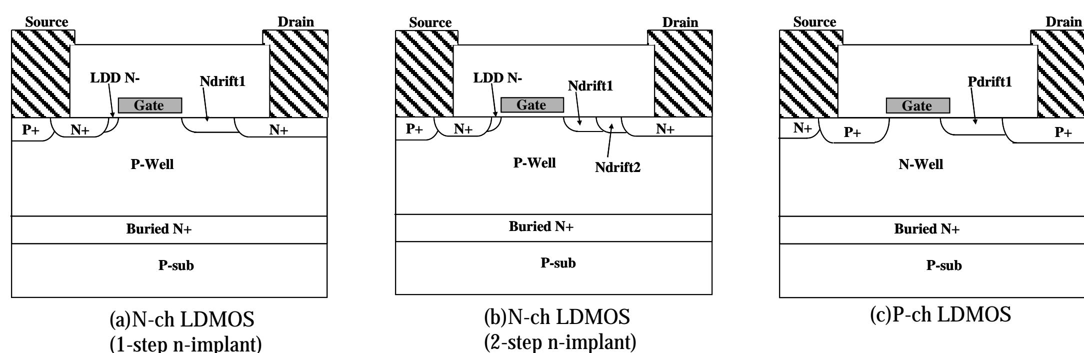
References

[1] Y.Kawaguchi et al., "Multi Chip Module with Minimum Parasitic Inductance for New Generation Voltage Regulator," *ISPSD'05*, pp.371-374

[2] M.Shiraishi et al.,"Low Loss and Small SiP for DC-DC Converters," *ISPSD'05*, pp.175-178

[3] K. Kinoshita et al.,"A New Adaptive Resurf Concept for 20V LDMOS Without Breakdown Voltage Degradation at High Current," *ISPSD'98*, pp. 65-68.



(a)N-ch LDMOS (1-step n-implant)

(b)N-ch LDMOS (2-step n-implant)

(c)P-ch LDMOS

Figure.1 Cross-sectional view of 20V output power devices based on the low cost 0.6um BiCD process. In case of N-ch LDMOS, we have adopted 2-step shallow n-implant structure (Ndrift1&Ndrift2) which improves the on-state breakdown voltage.

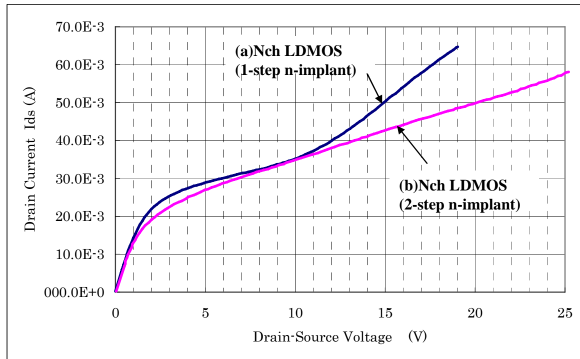


Figure.2 Measured I-V characteristics for fabricated N-ch LDMOS (@Vgs=5V, Channel width=157um). The 2-step n-implant structure improves the on-state breakdown voltage of 25V.

Table I Device characteristics

	Nch LDMOS (1-step n-implant)	Nch LDMOS (2-step n-implant)	Pch LDMOS
Static Breakdown Voltage (V)	25.0	24.4	23.4
On-state Breakdown Voltage (V)	19.0	25.0	25.0
Threshold Voltage (V)	0.85	0.85	-0.85
On-resistance (mohm・mm^2)	23.1	23.6	42.1

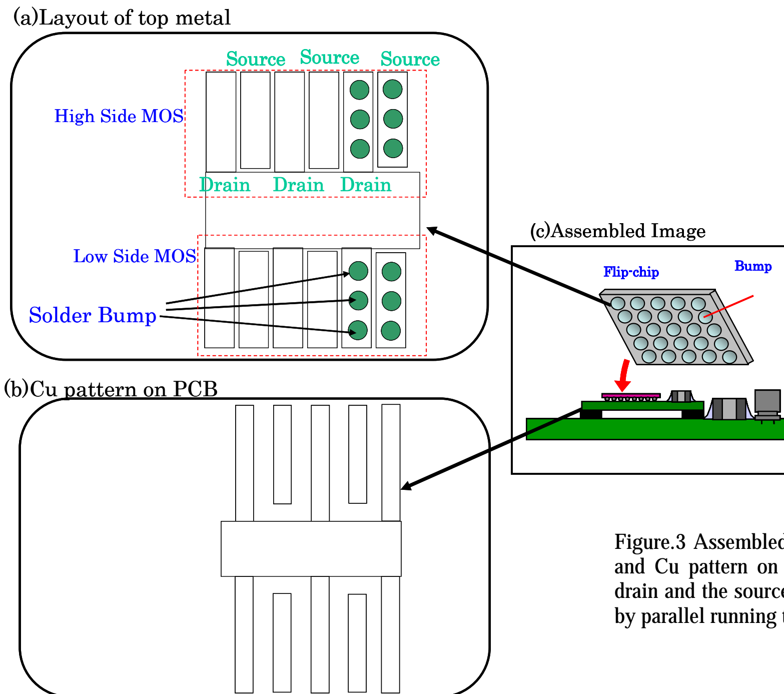


Figure.3 Assembled image, layout of top metal in IC and Cu pattern on printed circuit board (PCB). The drain and the source bumps are electrically connected by parallel running thick Cu metals in the PCB

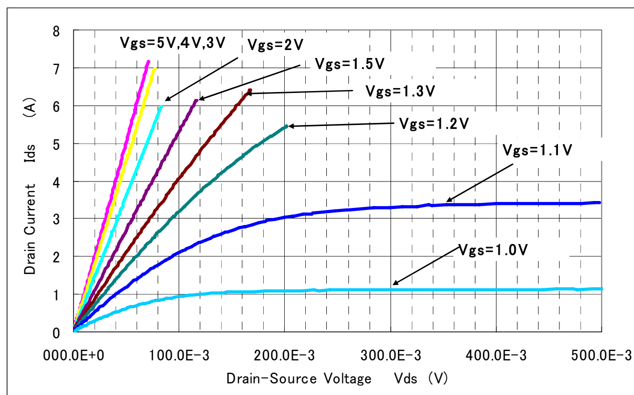
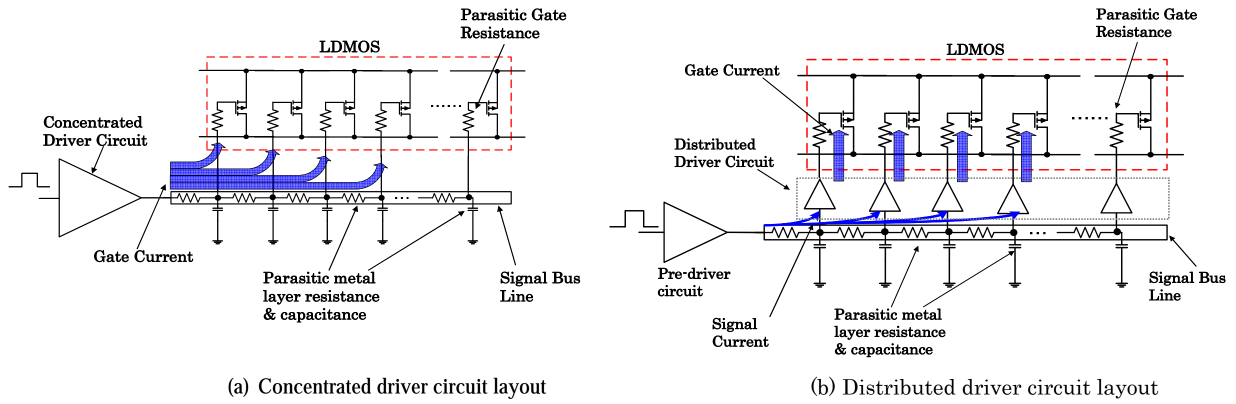


Figure.4 Output characteristics of a large area device (@effective area =3.6mm^2). Ron is 9.7m Ω (@Vgs=5V, Ids=5A)



(a) Concentrated driver circuit layout (b) Distributed driver circuit layout

Figure.5 Comparison of the distributed driver circuit layout with the conventional concentrated driver circuit layout

Table II. Simulated Device characteristics

	Concentrated driver circuit layout	Distributed driver circuit layout
Turn-on loss (mW)	12.1	5.48
Turn-off loss (mW)	48.6	26.6

@Vin=12V, Resistance =1.2ohm, Switching frequency=780kHz

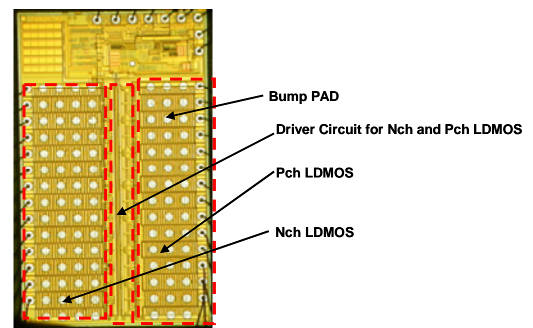


Figure.6 Micrograph of fabricated chip based on low cost 0.6um process. The chip size is $20.3mm^2$

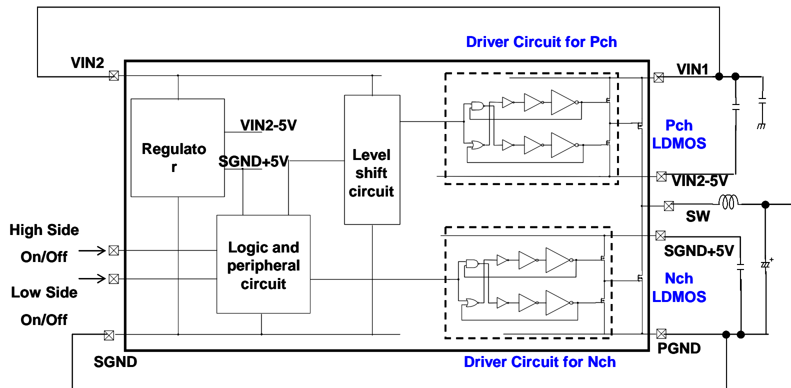


Figure.7 Equivalent circuit of fabricated chip

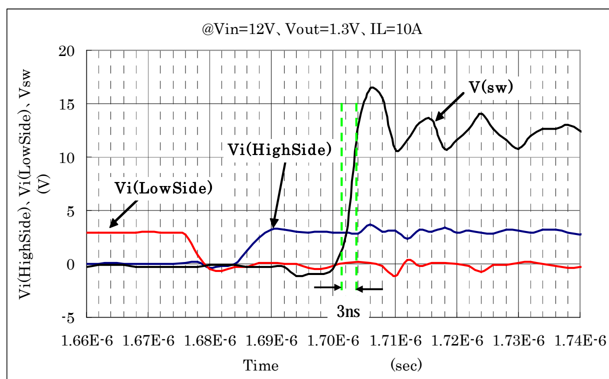


Figure.8 The switching characteristics of the fabricated chip at the condition of an inductance 2uH. The rise time of switching node is 3ns.

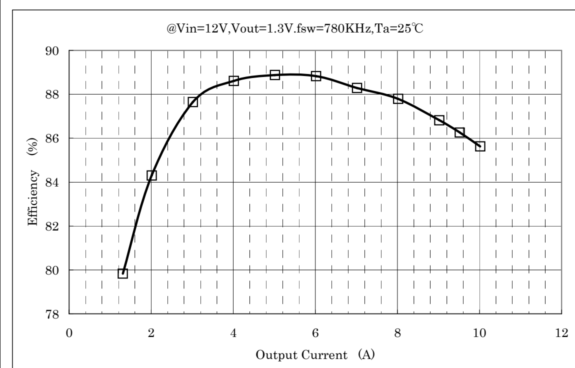


Figure.9 The measured dependence of efficiency on output current, (Vin=12V, Vout=1.3V, fsw=780kHz)