Recent Advances in High Voltage SOI Technology for Motor Control and Automotive Applications

- Invited paper -

Materials & Devices Lab. Toshiba Corp. 1 Komukai Toshibacho Saiwaiku, Kawasaki, 210, Japan
Akio Nakagawa

Abstract

One of the drawback of the conventional high voltage SOI devices requires a thick buried oxide. In the present paper, first, we propose a new high voltage SOI device structure, which does not require a thick buried oxide.

Second, we propose a method to reduce the chip size of high voltage power ICs by developing new LIGBTs, operating in a higher current density. Third, we demonstrate on-chip integration of MPUs, analog digital circuits and 60V power NMOS for automotive applications.

1. Introduction

SOI technology has been paid great attention because it provides complete dielectric device isolation at a reasonable cost in addition to high breakdown voltage capability[1,2]. A whole power system can be integrated on a single silicon chip if high voltage power devices can be integrated with analog and digital circuits as well as MPUs. Key technology is integration of high speed high voltage large current output devices, CMOS analog circuits, and MPUs etc. All the integrated devices should be fabricated by conventional CMOS processes so that conventional circuit libraries can be utilized without changes.

In the present paper, recent technological advances will be focused with brief review of high voltage SOI technology.

2. New high voltage SOI device structure

Figure 1 shows our experimental results, showing SOI diode breakdown voltage as a function of SOI layer thickness with buried oxide thickness as a parameter[2,3,4,5]. Figure 2 shows a basic SOI diode structure. It was found that an SOI diode breakdown voltage is determined by Resurf principle[6]. Maximum breakdown voltage is limited by the breakdown voltage of the 1-dimensional MOS diode portion[3], as illustrated in Fig.2, consisting of substrate(M)/ buried oxide(O) /silicon layer(S) under the n^+ emitter layer. The maximum breakdown voltage depends on the thickness of the buried oxide and the n-type silicon layer. For example, a 500V breakdown voltage diode requires 3μm buried oxide and 13μm thick silicon layer. The requirement of a thick buried oxide practically limits the application fields of SOI to below 600V.

In the present paper, we propose a novel SOI diode structure, which drastically increases the device breakdown voltage. Figure 3 shows the new structure, which is characterized by a SIPOS layer inserted between the silicon layer and the buried oxide. It was experimentally verified that diodes fabricated on the proposed SOI substrate (5μm thick silicon layer/0.8μm SIPOS/0.8μm SiO_2) exhibited above 600V breakdown voltages, which were far larger than the breakdown voltage 200V of the corresponding conventional SOI diodes fabricated on the same SOI substrate without the SIPOS layer(5μm thick silicon layer/0.8μm SiO_2). If the SIPOS layer works as a field shielding layer, the diode breakdown voltage no more depends on the substrate bias and the Resurf principle is no more valid for this structure.

It is expected that the proposed structure has a potential to realize over 1000V high voltage power ICs, because the structure does not require a thick buried oxide for high voltage structure.

3. High voltage large current lateral IGBTs for motor control applications.

Lateral IGBTs have been paid great attention because they simultaneously handle a high voltage and a large current. It is important to realize high speed switching without use of lifetime control processes, which are not included in conventional CMOS processes. One of effective methods to achieve high speed switching is to fabricate LIGBTs on relatively thin SOI layers. The turn-off fall-time of IGBTs simply decreased as the thickness of the silicon layer decreased, as seen in Fig.4, although the forward voltage drop slightly increased. The measured effective lifetime decreased as the SOI layer thickness decreased. This is because the effective lifetime is dominantly determined by the surface recombination velocity and is a function of SOI layer thickness[7]. Turn-off fall-time of LIGBTs on relatively thin SOI shows good temperature characteristics. The fall-time did not increase very much even as temperature increased, because the surface recombination velocity does not change very much as temperature changes.

500V lateral IGBTs have been developed for output devices of 500V, 1A DC brushless motor control ICs. Lateral IGBTs have now been scaled up to handle a current as large as 5 amperes. Figure 5 shows typical switching-off waveforms of 5A drain current. The current density is $175A/cm^2$.

Practical maximum current rating of lateral IGBTs is limited by chip area consumption and not by the actual current capability of the devices. This is because output

devices occupy most of the chip area and the cost of the power ICs deeply depends on the size of the power devices. Thus, it is extremely important to increase operating current density in order to reduce chip size as well as the chip cost in high voltage power ICs.

We propose multi-channel trench gate lateral Injection Enhanced IGBTs(IEGTs). Typical IEGT structure is illustrated in Fig.6. Figure 7 compares current voltage curves of conventional IGBT and proposed IEGT. The forward voltage is improved by introducing plural number of closely spaced trench gate channels and reducing channel resistance. A largest improvement was observed for the IEGTs with meshed trench gates, which is illustrated in Fig. 8. The proposed IEGTs successfully increased current density by 50% to 100% for the same forward voltage, as compared with conventional IGBTs, with retaining the same switching speed.

4. 60V lateral power MOSFET with integrated 4 bit MPU for automotive application

Another prospective application of SOI technology is automotive field. Currently, conventional pn junction isolated power ICs are frequently used for automotive applications. However, reliability of junction isolated power ICs is not sufficient.

The present paper shows that SOI technology provides a practical solution. The reasons are that developed 60V lateral NMOSFETs on SOI attained a sufficiently low specific on-resistance[8,9,10,11] such as 100mΩmm^2 [12], which is lower than that of conventional up-drain vertical 60V DMOSFETs. The developed 60V power NMOS automatically operates as a high side switch, as is described, in detail, later in this section. Moreover, the price of SOI wafers has become almost the same as that of epi-wafers.

4.1 60V Lateral Power MOSFET fabricated by CMOS fabrication processes

Figure 9 shows the cross-sectional view of the high voltage NMOSFET on 5μm thick p-type SOI substrate. The p-body region was formed by CMOS p-well. The n-drift layer was formed, using the same thermal process for the CMOS n- and p-wells. Since the channel region is formed not by DSA (diffusion self-align) but by the same processes as low voltage CMOS, the channel length depends on the accuracy of mask alignment.

Taking advantage of the SOI structure, the n-drift layer resistance can be minimized by choosing an optimum p layer doping. Figure 10 shows calculated on-resistance and breakdown voltage dependence on the impurity dose of n-drift layer for three cases of p type silicon layer concentration.

The experimentally obtained current-voltage curves for the developed power NMOS are shown in Fig. 11. The measured breakdown voltage is 60V and specific on-resistance is 100mΩ·mm^2 at Vgs = 5V.

High side switching operation is an important function in automotive applications, especially in case of H-bridges for motor control. The on-resistance of conventional high voltage MOSFETs on SOI is influenced by the substrate bias. However, the developed NMOSFET is free from substrate bias influence[11]. This is because the hole accumulation layer is induced on the buried oxide, shielding the influence of the source to substrate bias, as illustrated in figure 9. These results indicate that this device can be used for high side switch without on-resistance increase.

4.2 Possibility of system integration

This section experimentally shows the possibility of integration of an MPU together with BiCMOS analog circuits and 60V lateral NMOSFETs. 4 bit MPUs, vertical npn, pnp and 60V NMOSFETs have been fabricated on 2μm SOI substrates by conventional 0.8μm BiCMOS processes[11]. A schematic cross section of our BiCMOS and 60V NMOS structure is shown in Fig. 12.

The fabricated SOI 4 bit MPU chips, consisting of 30,000 FETs for core, 6,000 FETs for cash and 120,000 FETs for ROM, operated at a 20% faster clock speed of 50 MHz at 25 ^{o}C as compared with 42 MHz of the bulk version MPU and even operated at over 200 ^{o}C. It was found that clock speed can be improved and that a large latch up immunity at high temperature was realized even if any MOSFET is not isolated by trenches and if the SOI layer is not so thin as SIMOX. The maximum operating temperature was more than 300 ^{o}C. It was found that the yield of the MPU, fabricated on SOI, is the same as that on bulk wafers, verifying that the crystal quality of the currently available SOI wafers is sufficiently good. It was also found that both SOI and bulk MPUs can be operated at 300 ^{o}C if MPUs consist of pure CMOS, although the power consumption of the bulk MPU is larger than that of the SOI MPUs.

One of the characteristic features of the proposed SOI power IC structure, shown in Fig.12, is that there is no buried layers for bipolar transistors. It was found that vertical npn and pnp transistors fabricated on the n-well and p-well layers exhibited sufficiently good characteristics, as is shown in Ref.[11]. The current gains h_{FE} obtained for the vertical npn and pnp transistors were 80 and 30, respectively.

References

[1]A. Nakagawa et al., Proc. of ISPSD'90, p.97
[2]A. Nakagawa, Proc. of ISPSD'91, p.16
[3]A. Nakagawa et al.,1992 IEEE IEDM Tech. Digest, p229
[4]W. Wondrak et al., Proc. of ISPSD'92, p.278
[5]S.Merchant et al., Proc. of ISPSD'91, p.31
[6]Y.S.Huang et al., Proc. of ISPSD'91, p.27
[7]I. Omura et al., Proc. of ISPSD'93, p.248
[8]R.S.Wrathall et al., 1990 IEEE IEDM Tech. Digest, p.954

[9]T. Efland et al., 1992 IEEE IEDM Tech. Digest, p.237
[10]T. Efland et al., Proc. of ISPSD'1996, p.147
[11]H. Funaki et al., 1995 IEEE IEDM Tech. Digest, p.967
[12]Y. Kawaguchi et al., to appear in Ext. Abst. of 1996 SSDM

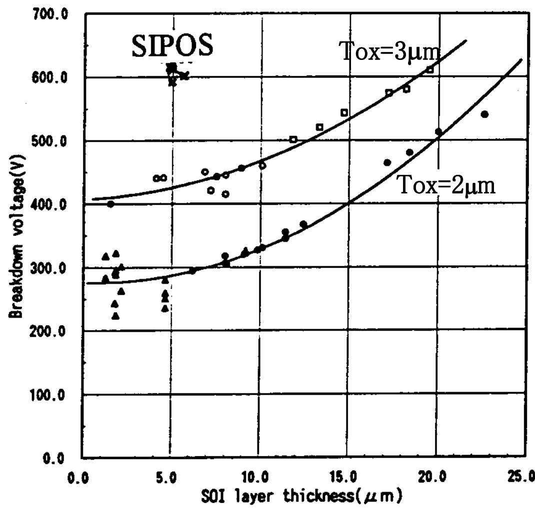


Fig.1 Breakdown voltage as a function of SOI layer thickness with buried oxide thickness as a parameter. Breakdown voltage of SIPOS SOI structure is plotted as a comparison.

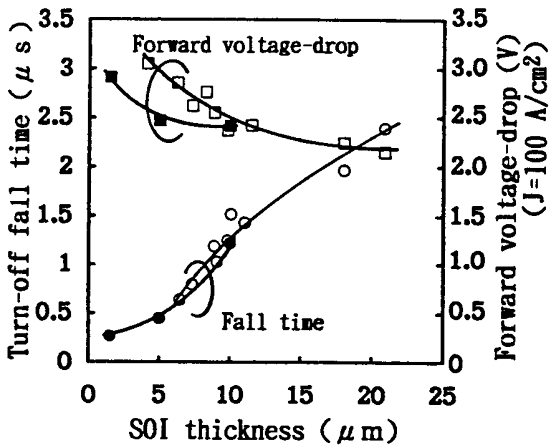


Fig.4 Turn-off fall-time and forward voltage drop as a function of SOI layer thickness.

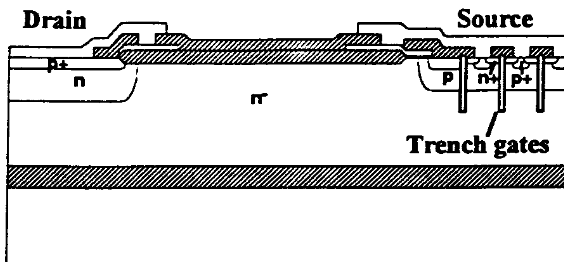


Fig.6 Lateral IEGT structure.

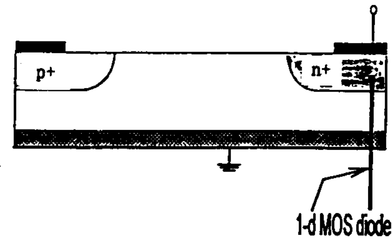


Fig.2 Typical SOI diode. 1-d MOS structure determines maximum breakdown voltage.

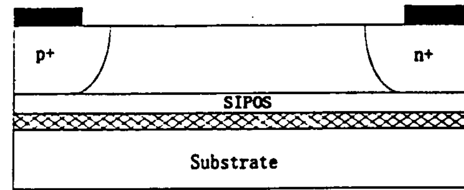
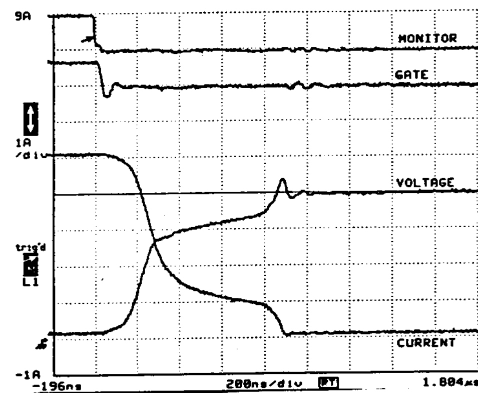


Fig.3 Proposed new diode structure.



Current:1A/Div , Voltage:100V/Div
Gate: 5V/Div, Time:200ns/Div
Fig.5 Typical 5A switching waveforms of a lateral IGBT

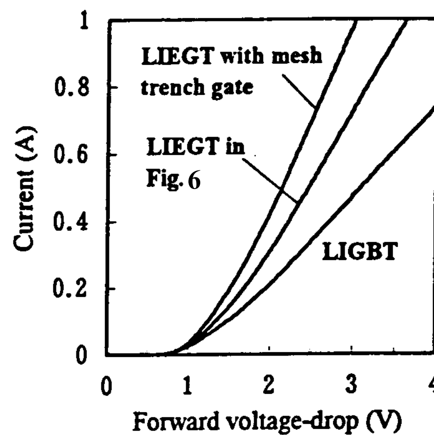


Fig.7 Comparison of IEGT and IGBT current voltage curves.

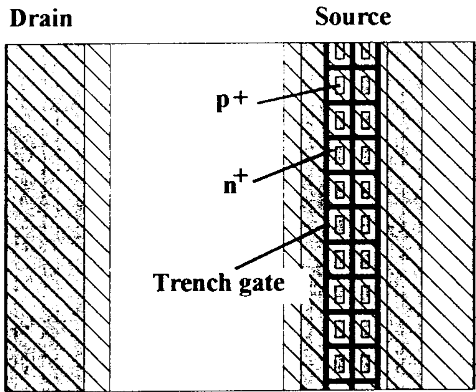


Fig.8 IEGT structure with meshed trench gates

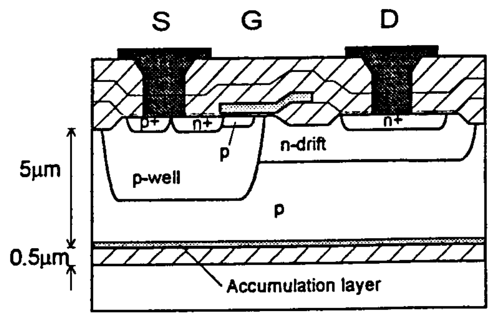


Fig.9 Cross sectional view of the developed 60V NMOSFET. When used as high side switch, hole accumulation layer appears on the buried oxide, shielding the substrate bias.

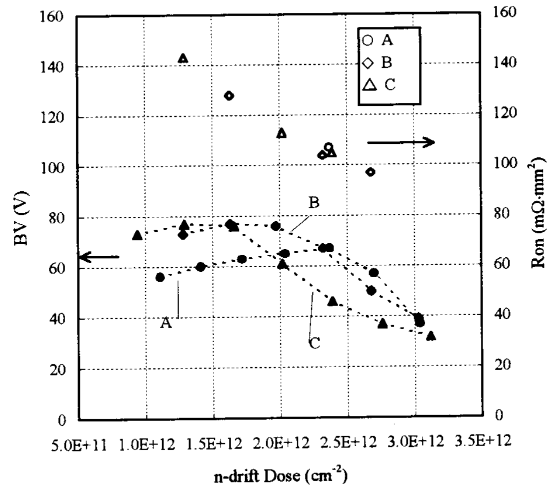
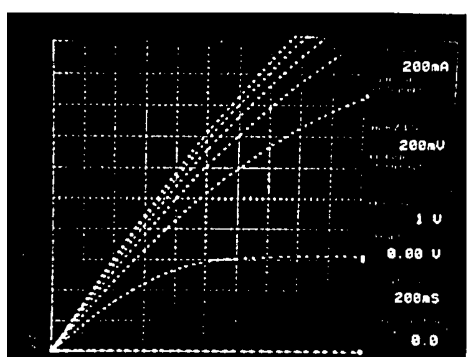


Fig.10 Calculated on-resistance and breakdown voltage dependence on the impurity dose of n-drift layer for three different p-layer doping A > B > C.



Current: 200mA/Div Voltage: 200mV/Div

Fig.11 Measured current voltage curves of 60V power NMOS. Devices area is $0.15mm^2$.

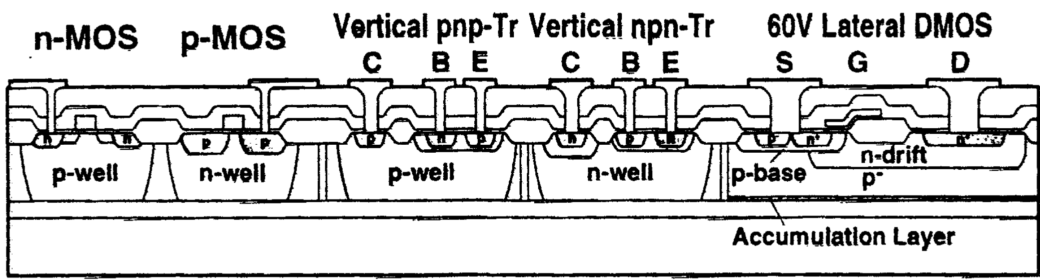


Fig.12 Schematic cross section of 60V NMOS and BiCMOS devices