20A 5V single chip DC-DC converter IC with 5mohm MOSFET switch

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***Abstract*- In this paper, we demonstrate 20A operation and high switching frequency 980 KHz of single chip DC/DC converter. The fabricated chip consists of the digitally control block, the low on-resistance MOSFET switches and the drivers. The chip adopted low impedance metal bump technology. The on resistance of Nch MOSFET is 4.3mΩ (@drain current=10A, gate voltage=5V) comparable to the discrete device. The fabricated chip achieves maximum output current 24A and max efficiency 91.2% for the input voltage, the output voltage and switching frequency of 5V, 1.083V and 980KHz, respectively. The efficiency without power loss by the parasitic resistance on PCB and output filter is 81.9% at the output current 20A.**

I. INTRODUCTION

A high efficiency, high power density, high current slew rate di/dt is strongly demanded for DC−DC converters. A high switching frequency operation would significantly reduce the value of inductor and capacitance in the output filter of DC-DC converter with benefits of lower cost, smaller footprint, and higher current slew rate. Switching loss and inductor loss increase with increasing frequency, which limits the operating range of conventional DC-DC converters to several hundred kHz.

In order to improve the conversion efficiency at high switching frequency, there have been many studies on optimizing the device structure of switching MOSFET and the circuit parameters such as parasitic devices on board.

In terms of device structure, gate-drain capacitance of the switching MOSFET should be small to reduce switching loss. In a discrete MOSFET, especially in a trench MOSFET, a power MOSFET with a thicker oxide at the bottom of the trench is proposed to reduce the gate-drain capacitance. The method needs the complicated process to achieve the structure.

On the other hand, in a lateral MOSFET used in a power IC, it is easier to reduce gate-drain capacitance by applying the self-aligned process between the gate electrode and the drift layer.

In terms of the parasitic devices, it has been pointed out that the parasitic inductance between the output MOSFET and the gate driver circuit decreases the conversion efficiency. Multi Chip Module or 1 chip solution are effective to reduce the parasitic wiring inductances [1,2]. It was also predicted that a low impedance gate drive can reduce the mirror period in the turn-off transient, realizing ideal switching and low turn-off power loss [3]. The achievable minimum turn-off power loss is just the main junction charge/discharge loss and is determined by the new FOM proposed in Ref.[3,4]. 1 chip solution is favorable for achieving the ideal switching because the parasitic inductances are small and sufficiently low impedance gate driver circuits are easily integrated with power MOSFETs.

However, the output current of 1 chip converter has been considered to be small of several amperes because of the large on-resistance of output lateral devices. We demonstrated 10A 12V single chip switching regulator IC by applying a metal interconnect with bump technology and adopting distributed driver circuit layout[5].

In the 5V power ICs, integrated lateral power devices bring smaller specific on-resistance, compared to discrete power devices [6]. The on resistance in discrete devices is composed mostly of a channel resistance, drift resistance and N+ substrate resistance. The substrate resistance occupies a larger part of the total device resistance at the low breakdown voltage discrete devices. This is why the discrete power devices need thick N+ substrate for wafer handling. On the other hand, integrated lateral power devices don't require the thin substrate because both the source and drain electrode are formed on the wafer surface. 5V lateral power devices can have the capability to drive as large output current as discrete devices.

In recent years, researches in the area of digitally-controlled DC-DC converter have attracted much attention. Digital control provides flexibility, programmability and opens up new control algorithm not possible in the converters with traditional analog control.

In this paper, we demonstrate 20A operation and high switching frequency 980 KHz of single chip DC/DC converter with digitally control.

II. SINGLE CHIP DC/DC CONVERTER IC WITH DIGITALLY CONTROL

Figure.1 shows the circuit diagram of the developed synchronous DC-DC buck converter IC. The input voltage is Vg=5V, the reference voltage is Vref=1.083V, the output-coil is L=0.2uH. It is composed of the flash A/D converter, the digital pulse-width modulators (DPWM), control circuitry, power switches and the drivers. The parameters of PID compensator and dead-times are loaded from external EEPROM or PC through a serial interface when the system is

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started or rebooted. The A/D converter is composed of only six comparators, resulting in a 7-level quantization (the least significant bit value=10mV). The error signal at the output of A/D is processed by a PID compensator, which provides the necessary duty-cycle command for the output voltage regulation. Look-up table architecture is applied to the compensator instead of the duty calculation including multiplication and the PID compensator can be accomplished in small size and in a small number of system clock cycles[7].
In pulse-width modulators, analog control system provides very fine resolution for output voltage adjustment. On the other hand, a digital control system has discrete set points resulting from the resolution of quantizing elements in the system. The output voltage resolution corresponds to the time resolution in the DPWM. We developed a hybrid 10-bit DPWM. The developed 10-bit DPWM is composed of 5-bit counter and 5-bit delay line[8]. The clock period is divided into 32 time steps by 5-bit delay line

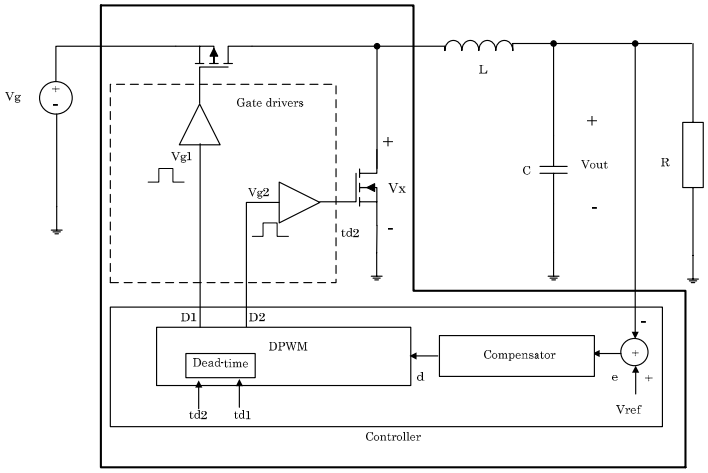


Figure.1 Circuit diagram of the developed synchronous DC-DC buck converter: Vg=5V,Vout=1.083V

III. Device Structures

Figure 2 shows a cross-sectional view of 5V output devices based on the low cost 0.6um BiCD process[6]. During dead-time period, a negative bias is applied on the drain contact with respect to the substrate of low side MOSFET due to the switching of an inductive load. As the technology employs junction isolation, this may lead to unwanted injection of minority charge carriers into the substrate. The resulting currents can be of considerable magnitude and may lead to malfunction of the whole Power IC device. Minority carriers injected into the substrate can cause disturbances of the signals in the low power circuitry or latch-up in the CMOS structures. The buried N+ layer is electrically connected to the source electrode to reduce the coupling between the drain and the substrate. Three metal layers with a 3um thick top metal layer are utilized.

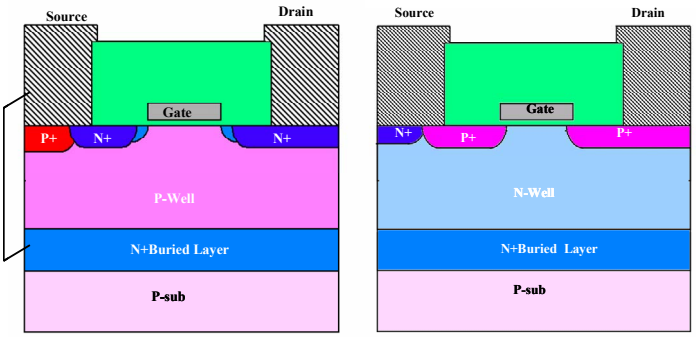


Figure.2 Cross-sectional view of output power devices based on the low cost 0.6um BiCD process.

IV Power IC Using Bump Technology

The on resistance of lateral MOSFETs with wire bonding deteriorates considerably with increase in device size due to the parasitic resistance. Interconnect resistance not only increases overall device resistance but also causes debiasing effect in active cells [9]. This imposes a fundamental limit on the maximum die size practically achievable with lateral MOSFETs. In order to reduce the interconnect resistance; we have adopted bumping technology [10].

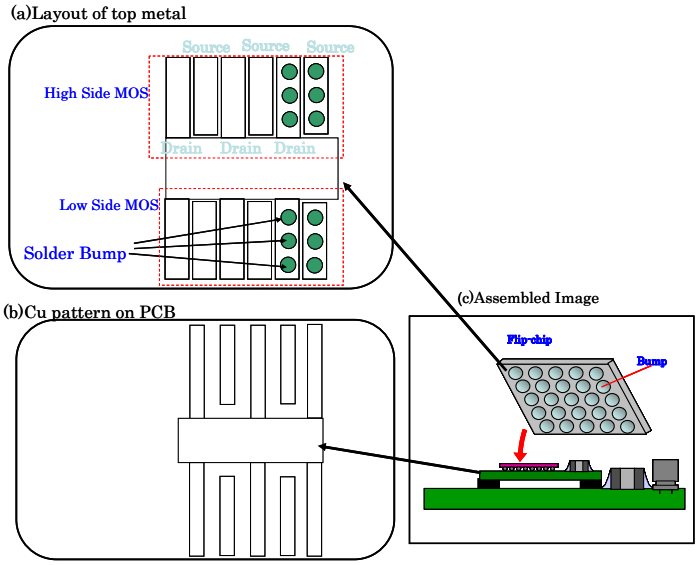


Figure.3 Assembled image, layout of top metal in IC and Cu pattern on printed circuit board (PCB). The drain and the source bumps are electrically connected by parallel running thick Cu metals in the PCB.

Figure 3 shows assembled image including the layout of top metal in IC and Cu pattern on printed circuit board (PCB). The

chip is attached to the intermediate PCB through bump ball. We have adopted Pch MOSFET for high side switching device in DC/DC converter.

The source and drain metals are alternately formed and the drain metals of Pch MOS and Nch MOS are connected each other. The PCB connects drain and source bumps by parallel running thick Cu metals. The resistance that current laterally flows in the top metal is made as small as possible.

V. Implementation and Results

Figure 4 shows the micrograph of fabricated chip based on the low cost 0.6um process. The two output devices, driver circuits and control block are integrated into a die. A number of driver circuits are placed between N-ch and P-ch MOS. A number of driver circuits are formed along a long side of the output devices and the length that large gate charging or discharging current flow path is made as short as possible. The whole output device can uniformly turn on or off [5].

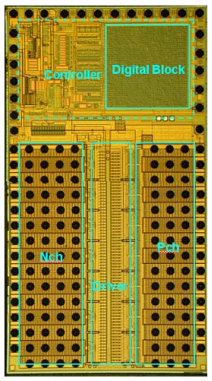
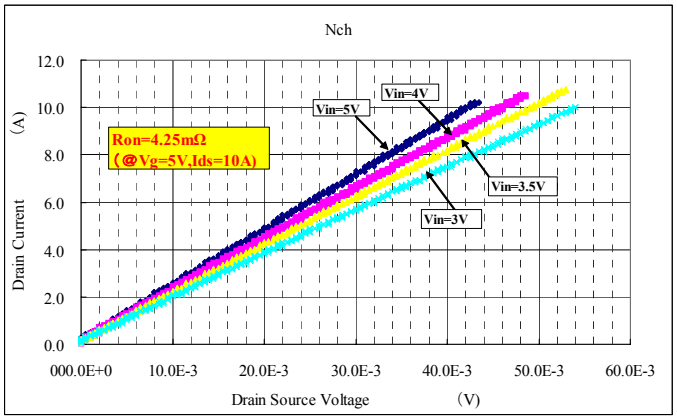
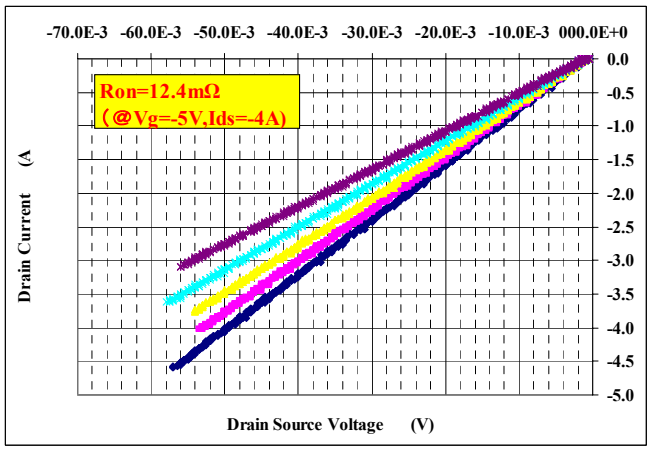


Figure.4 Micrograph of fabricated chip based on low cost 0.6um process.

Figure 5 shows the measured output characteristics of a large area Nch MOS and Pch MOS. The on resistance of Nch MOS and Pch MOS are 4.3mΩ (@drain current=10A, gate voltage=5V) and 12.4mΩ (@drain current=4A, gate voltage=-5V), respectively.



(a)Nch MOSFET



(b)Pch MOSFET

Figure.5 Output characteristics of a large area device

This value is measured with the developed IC mounted on the PCB, and therefore includes all possible parasitic resistance (including solder joint resistance and Cu pattern resistance on the PCB). We have achieved that the value of on resistance is below 5mΩ, comparable to the discrete device.

Figure 6 shows the photograph of board for evaluating the developed IC. The chip is attached to the intermediate PCB through bump ball and the intermediate PCB is mounted on the mother board. In the EEPROM, the PID parameters and the various configuration parameters are stored.

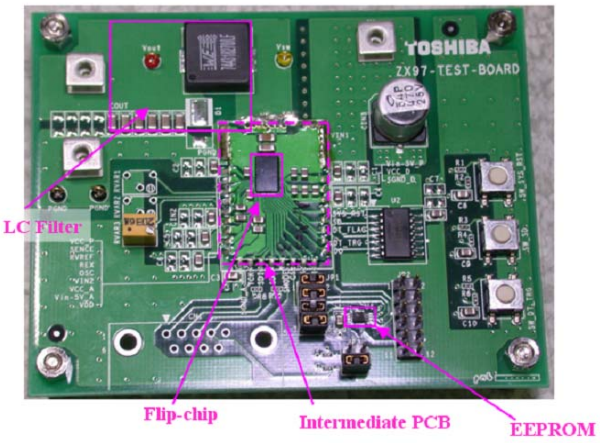


Figure.6 Photograph of board for evaluating the 20A 5V single chip DC/DC converter IC

Figure 7 shows the transient characteristics of the voltage at the intermediate node Vx between high side MOS and low side MOS at the output current 24A. The fabricated chip indicates high current switching capability of more than 24A.

Figure 8 shows the dependence of the converter efficiency on output current obtained by both experiment and simulation

when the output voltage and switching frequency are 5V, 1.083V and 980 KHz, respectively.

The blue line shows the efficiency without power loss by the parasitic resistance on PCB and output filter and the pink line shows efficiency including power loss by the parasitic resistance on PCB and output filter. The maximum efficiency is 91.2% at output current 4A. The efficiency without power loss by the parasitic resistance on PCB and output filter is 81.9% at the output current 20A.

The green line shows the simulated efficiency including power loss by the parasitic resistance on PCB and output filter. Using SPICE model for high and low side MOSFET, time domain simulation can be executed for entire DC-DC converter system, considering distributed parasitic resistance and inductance. The efficiency can be obtained by monitoring the injected power into DC-DC converter.

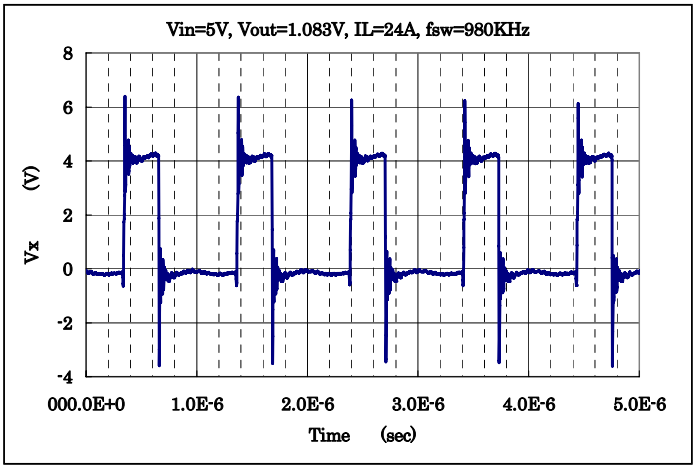


Figure.7 Transient characteristics of the intermediate node between high side MOS and low side MOS at the output current 24A

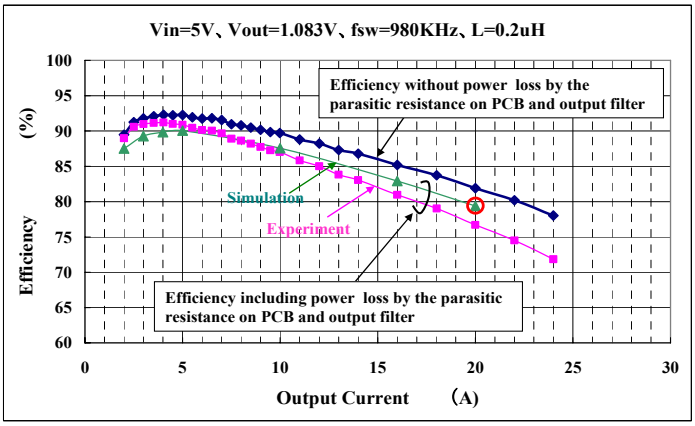


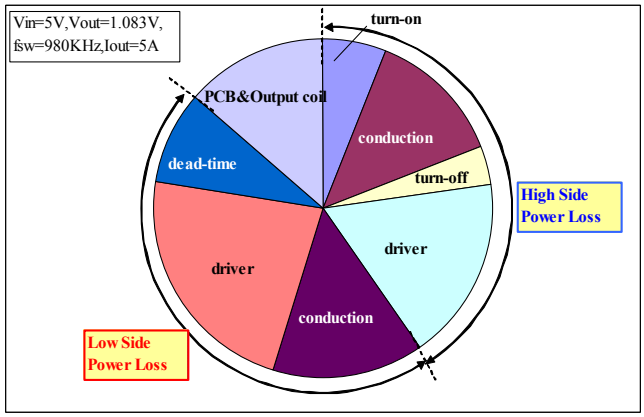
Figure.8 Measured and simulated efficiency on output current (The input voltage: 5V, the output voltage:1.083V, the switching frequency: 980KHz)

Figure 9 shows the simulated power loss distributions for 5A and 20A of the output current.

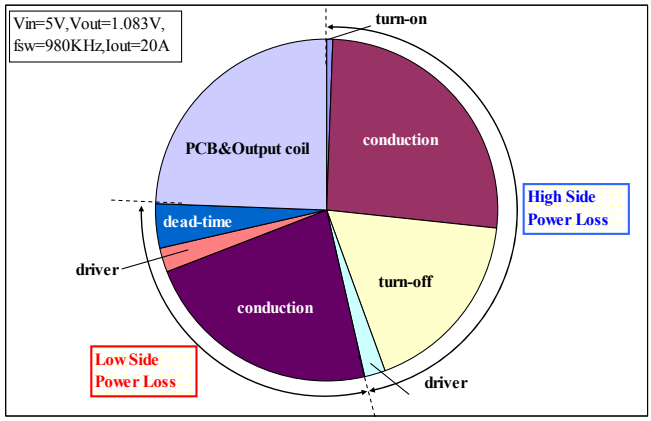
At the output current 5A, the switching power loss at high side MOSFET and the power loss to drive the MOSFETs are dominant.

At the output current 20A, the parasitic resistances on PCB and output filter are equivalent to the on-resistance of the output devices. The parasitic resistance has a significant impact on the decrease of the efficiency in the large output current. The turn-off loss of high side MOSFET is large because of the spike voltage generated by the parasitic inductance in the main current flowing path. As the spike voltage is over the breakdown voltage of the high side MOSFET, the avalanche breakdown occurs and the turn-off loss increases sharply.

In the high output current and high speed gate driving, the turn-off loss of high side MOSFET with low breakdown voltage is susceptible to the parasitic inductance.



(a)Iout=5A



(b)Iout=20A

Figure.9 Simulated power loss distributions for 5A and 20A of the output current.

Figure 10 shows the simulated dependence of high side MOSFET power loss on the summed parasitic inductance in the main current flowing path (Ls) at the output current 20A.

The high side MOSFET turn-off loss decreases as the parasitic inductance (Ls) decreases. It is important to reduce the parasitic inductance between the input capacitance and the flip-chip.

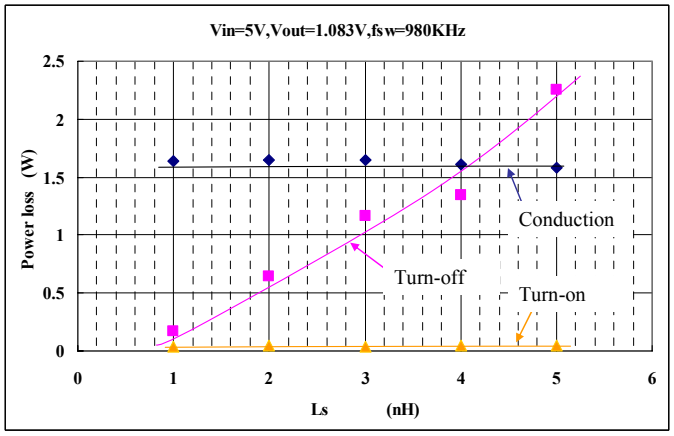


Figure.10 Dependence of high side MOSFET power loss on parasitic inductance in the main current flowing path(simulation).

VI. Conclusion

We demonstrated 20A operation and high switching frequency 980 KHz of single chip DC/DC converter. The fabricated chip consists of the digitally control block, the low on-resistance MOSFET switches and the drivers. The chip adopted low impedance metal bump technology. The on resistance of Nch MOSFET is 4.3mΩ (@drain current=10A, gate voltage=5V) comparable to the discrete device. The fabricated chip achieves maximum output current 24A and max efficiency 91.2% for the input voltage, the output voltage and switching frequency of 5V, 1.083V and 980KHz, respectively. In high output current, the turn-off loss of high side MOSFET is large because of the spike voltage generated by the parasitic inductance in the main current flowing path. It is important to reduce the parasitic inductance between the input capacitance and the flip-chip.

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