Proposal of the Method for High Efficiency DC-DC Converters and the Efficiency Limit Restricted by Silicon Properties

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Abstract— **In this paper, we analyzed details of power loss in DC-DC converters and proposed the method for improving efficiency. Before the analysis was carried out, we verified the accuracy of SPICE simulation for DC-DC converters by comparing with measured data and a result from 3D electromagnetic simulation which can solve the entire device package and PCB directly. After that, we analyzed the details of the influence of various parasitic inductances on the efficiency by the circuit simulator. The power loss does not decrease monotonically as the parasitic inductance decrease. This is because high side turn-on loss increases as the parasitic inductance decreases. A large voltage drop occurs across the high side MOSFET, because the parasitic inductance is too small to restrict the di/dt. The total parasitic inductance in the main current path for the MCM module is chosen to be equivalent to the optimum value.**

One of the most important design parameters is the total resistance in the gate driver circuit for power MOSFETs because it is important to reduce the gate resistance in order to reduce high side switching loss and to achieve a short dead time without causing self-turn-on of the low side MOSFET.

Finally, we discussed maximum DC-DC converter efficiency restricted by silicon limit. It is predicted that the maximum efficiency for ideal silicon MOSFET is 96% for 1MHz. The results predict that the switching frequency is limited to as high as 5MHz, if we assume more than 86% conversion efficiency, as far as the large current, 12V input voltage VRM are concerned.

I. Introduction

With recent increase in clock speed of CPU, low voltage, large current, high di/dt DC-DC converters are strongly demanded. Many studies on high speed switching MOSFETs and on the effects of circuit parasitic components on PCB board have been carried out [1, 2].

In the present paper, we will present the optimized conditions for the gate driver circuits and the power train in order to achieve high efficiency DCDC converters as well as the ultimate silicon limit efficiency of the converters.

It is often pointed out in buck converters that the parasitic source inductance of the high side MOSFET decreases the conversion efficiency. In this paper, we first show what the optimum inductance is in the power train. We executed the detailed analysis on the influence of the parasitic inductances along the main current path in the power train. It was generally believed that the conversion efficiency simply increases as the parasitic inductance values decrease. In contrast to the general belief, we find, for the first time, that there is an optimum value for the circuit inductance including parasitic ones that maximizes the conversion efficiency, depending on the impedance of the gate circuit. The optimal value is 1 or 2 nH in the condition that total gate circuit impedance is as low as 0.4 Ω.

One of the most important design parameters is the impedance values of the gate driver circuits for power MOSFETs. We will verify that the very low impedance gate drive drastically improve the conversion efficiency by almost 4%. The rapid gate drive reduces not only the high side MOSFET switching loss but also the low side MOSFET loss.

Finally, we discuss the maximum DC-DC converter efficiency restricted by so-called “silicon limit”. We predict the maximum converter efficiency and the maximum operating frequency, assuming practically optimized ideal silicon MOSFETs as well as the optimized gate driving condition.

II. Accuracy Verification of Calculated Efficiency by Circuit Simulation

In the present paper, we will use a circuit simulator with a newly developed sub-circuit model for power MOSFETs. In order to check the validity of the model, we calculated the power loss of a multi chip module (MCM), shown in fig. 1. The feature of the MCM is that two power MOSFET chips and the driver circuit are integrated in the small QFN56 package, whose size is 8mm by 8mm square. The values of the parasitic inductances and capacitances in the MCM were extracted by electromagnetic simulation and were considered in the circuit simulation, as shown in fig. 2. In order to execute accurate circuit simulation, the trench MOSFET was modeled as the sub-circuit shown in fig. 3[3]. As the value of Cgd depends on both Vgd and Vds, it was given as a newly developed function to fit the measured characteristics of the trench MOSFETs. DBD represents the body diode in trench MOSFETs. Figure 4 shows the dependence of the converter efficiency on output current, obtained by both experiment and simulation. The

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simulated value is in good agreement with experimental value.

In addition, in order to verify the accuracy of calculated efficiency by the circuit simulation, 3D electromagnetic simulation (Speed2000 [4]), which can solve the entire device package and PCB directly and have SPICE interface, was carried out. Using SPICE model for high and low side MOSFET, time domain simulation can be executed for entire DC-DC converter system, considering distributed parasitic LCR. In order to simulate the effect of distribution in MOSFET chip, developed SPICE model of high and low side MOSFET are divided into 17 and 55 regions, respectively, as shown in fig. 5. Figure 6 shows low side MOSFET turn off waveforms of A and B area in fig. 5. The results indicate that the distributed parasitic LCR slightly affect gate voltage, and does not seriously affect the drain current. This result concludes that lumped spice model can be used for efficiency simulation considering distributed parasitic LCR in the circuit.

III. Efficiency Improvement by Optimization of Parasitic Inductance

The influence of various parasitic inductances on the efficiency is examined by the circuit simulator. The same power MOSFETs as used in the MCM were adopted in the analysis. Figure 7 shows the dependence of total power loss on the summed value of the parasitic inductances in the main current flowing path (Ls). The parameter in the figure is the total resistance value of the gate driver circuit. The total power loss dissipated both in power MOSFETs and in driver circuits, does not decrease monotonically as the parasitic inductance decreases. Instead, there is an optimum inductance value that minimizes the total power loss. This is because the turn-on loss of the high side MOSFET increases as the parasitic inductance decreases, as shown in fig. 8. In addition, when total resistance value of the gate driver circuit is reduced, the optimum inductance value and the minimum value of the total power loss are decreased. These will be explained next section. Figure 9 (a) and (b) show the turn-on and turn off waveforms of the MOSFET for the two cases of the inductance value, Ls, of 0.1nH and 2nH, respectively. In the case of Ls=0.1 nH, a large power loss occurs in the high side MOSFET during the period of the high side MOSFET turn-on, because a large reverse recovery current of the body diode of the low side MOSFET flows in a short time period. A large voltage drop occurs across the high side MOSFET, because the parasitic inductance is too small to restrict the di/dt.

In the case of L=2.0 nH, a large di/dt is prevented by the parasitic inductance of 2nH. Instead, a large voltage, L*di/dt, appears across the parasitic inductance and the turn-on loss of high side MOSFET is reduced.

It should be noted that the total parasitic inductance in the main current path for the developed MCM module is carefully chosen to be equivalent to the optimum value.

IV. Efficiency Improvement by Reduction of Gate Resistance

In this section we will propose low impedance gate drive of power MOSFETs for high efficiency converters. Figure 7 shows the dependence of the converter efficiency on the total gate resistance. It is found that the efficiency is significantly improved by reducing the gate resistance. The calculated efficiency is increased by almost 4% for the output current of 30 amperes. Note that the gate resistance is defined as the sum of the MOSFET internal gate resistance and the gate driver circuit resistance.

The main reason is that the mirror period, which is determined by the Qgd value divided by the magnitude of the supplied gate current, can be significantly reduced by the small gate resistance. When the gate resistance is 0.4 Ω, the observed switching time is as small as 2nsec! The validity of the very short switching time was confirmed by the device simulator, Dessis, assuming the same small gate resistance. The TCAD results, shown in Fig.10, indicate that the trench MOSFET can be switched off actually at 2nsec, if 0.4 Ω gate circuit resistance is achieved.

The dead time is optimized to allow maximum efficiency. Distribution of each power loss element is shown in fig. 11. Reduction of the gate resistance reduces not only the high side MOSFET switching loss, but also the losses in the dead time and the self turn-on-loss of the low side MOSFET. Figure 12 (a) and (b) shows the calculated waveforms of the low side MOSFET after the device turns-off and the high side MOSFET turns-on. Figure 12 (a) shows an example for the optimum dead time condition for the low gate resistance case of Rg+Rdriver=0.4Ω. Although the same short dead time can be used even for the case where the gate resistance is as high as 3.66Ω, self-turn-on occurs in the low side MOSFET and a large power loss occurs, as seen in fig. 12 (b). Therefore, it is important to reduce the gate resistance in order to achieve a short dead time without causing the self-turn-on of the low side MOSFET.

V. Future Maximum Efficiency limit restricted by Silicon properties

In this section we estimate the maximum achievable converter efficiency if the present power MOSFET is improved up to its material limit. From the existing theory, the lowest on-resistance value for 30V range silicon MOSFET (BV=37.2V) is 5 mΩmm2. Figure 13 shows the dependence of the efficiency on the output current for the current MOSFET (RonA=29mΩmm2) and the silicon limit MOSFET whose on-resistance is assumed as low as 5mΩmm2 with retaining the same value of the gate-drain capacitance. The FOM, RonQgd for the current MOSFET is 18.8 mΩnC and that for the ideal MOSFET is assumed 3.28 mΩnC.

The calculated results predict that the maximum efficiency for the ideal silicon MOSFET is 96% for 1MHz. Distribution of each power loss element is shown in fig. 14. Figure 15 shows the dependence of efficiency on switching frequency. According to the result, 86% efficiency at 3.5 MHz will be possible in future, if the MOSFET technology improves. It is also predicted that the maximum practical operation frequency and efficiency will be 5 MHz and 86% for large current VRMs.

References

[1] Y. Kawaguchi et al. Proceedings of ISPSD 2005 pp. 371-374
[2] M. Shiraishi et al. Proceedings of ISPSD 2005 pp. 175-158
[3] K. Kinoshita et al. Proceedings of IPEC 2005 pp. 971-975
[4] http://www.sigrity.com/products/speed2000/spd2k.htm

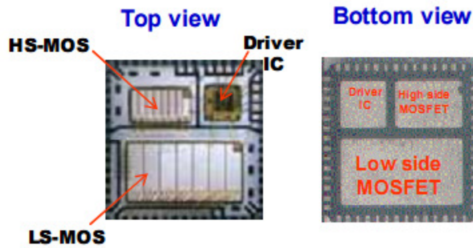


Figure 1 Top and bottom view of the Multi Chip Module for DC-DC converter

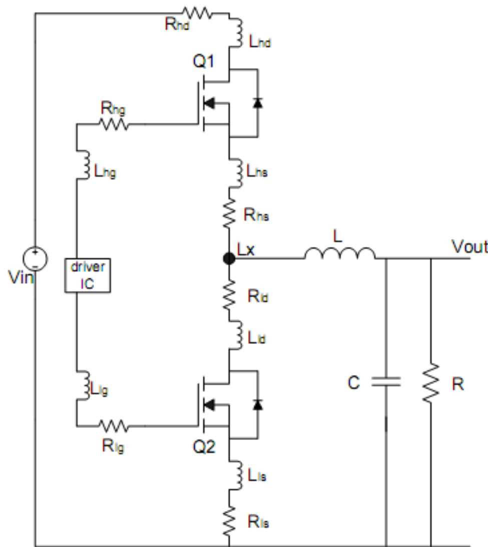
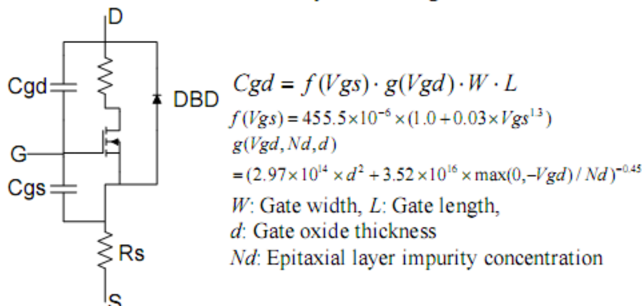


Figure 2 Parasitic components in DC-DC converter circuit. The values of parasitic inductances and resistances in the MCM package and circuit board were extracted by electromagnetic simulation.



$$Cgd = f(Vgd) \cdot g(Vgd) \cdot W \cdot L$$

$$f(Vgs) = 455.5\times10^{-6}\times(1.0+0.03\times Vgs^{1.3})$$

$$g(Vgd, Nd, d)$$

$$= (2.97\times10^{14}\times d^2 + 3.52\times10^{16}\times \max(0, -Vgd)/Nd)^{-0.45}$$

W: Gate width, *L*: Gate length,
d: Gate oxide thickness
Nd: Epitaxial layer impurity concentration

Figure 3 Spice model for Trench MOSFET. As the value of Cgd depends on both Vgd and Vds, it was given as a newly developed function to fit the measured characteristics of the trench MOSFETs. DBD represents the body diode in trench MOSFETs

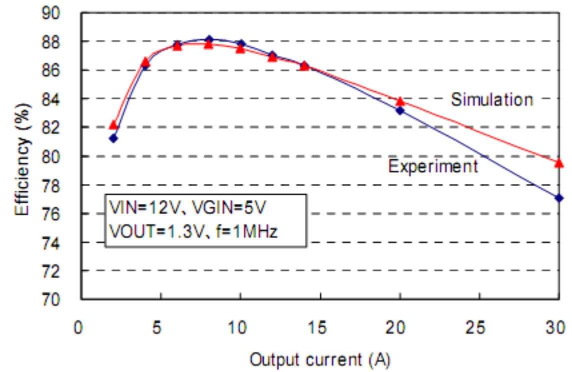


Figure 4 Dependence of efficiency on output current obtained by experiment and circuit simulation. The simulated value is in good agreement with experimental value.

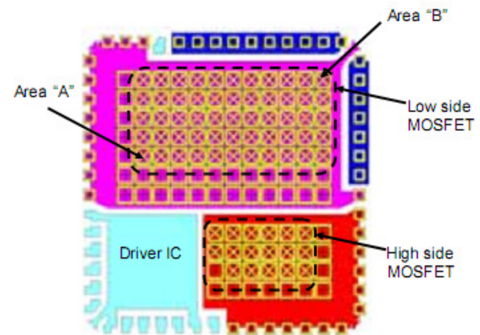


Figure 5 MCM model for 3D electromagnetic simulation considering distributed parasitic LCR. High side MOSFET and low side MOSFET is divided into 17 and 55 areas, respectively.

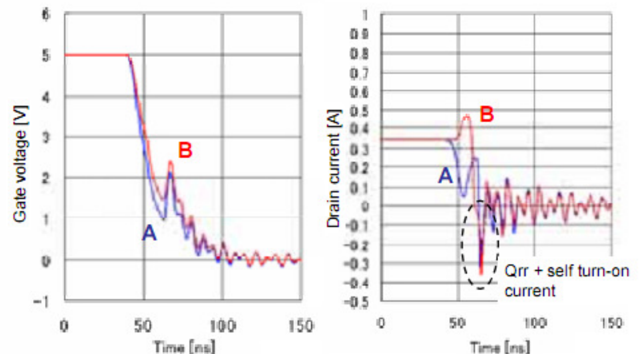


Figure 6 Simulated gate voltage and drain current waveform of low side MOSFET turn-off period for area A and B in fig. 5. Distributed parasitic LCR slightly affect gate voltage, but does not seriously affect the self turn-on current.

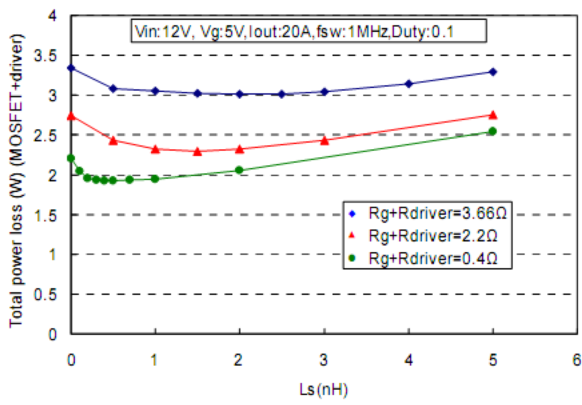


Figure 7 Dependence of power loss on parasitic inductance in the main current flowing path. The total power loss does not decrease monotonically as the parasitic inductance decrease.

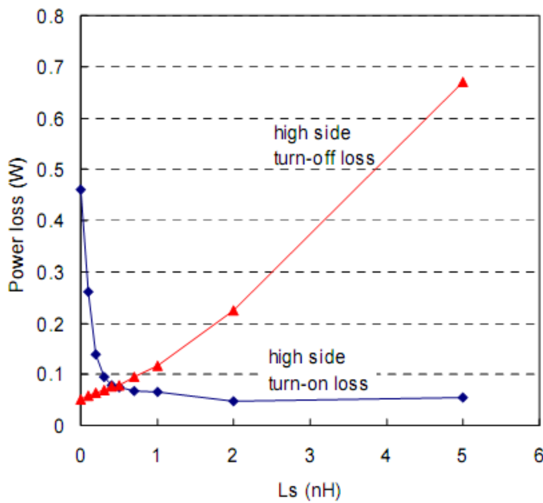
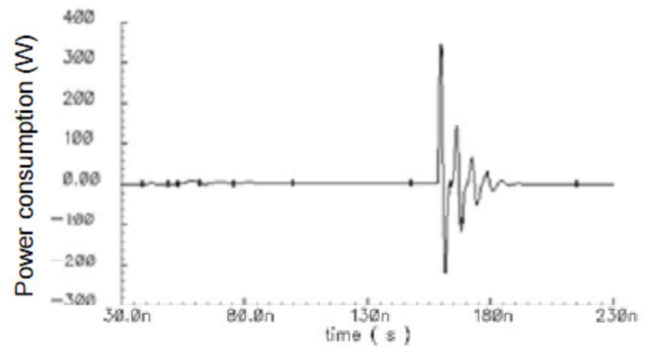
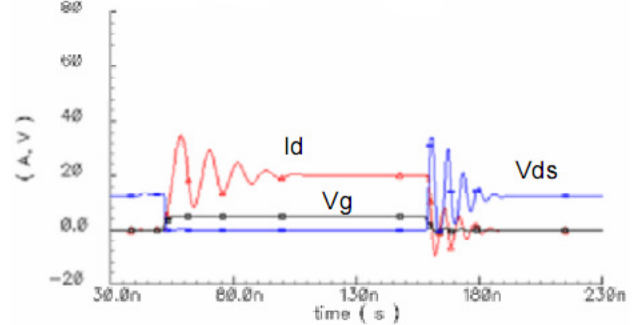
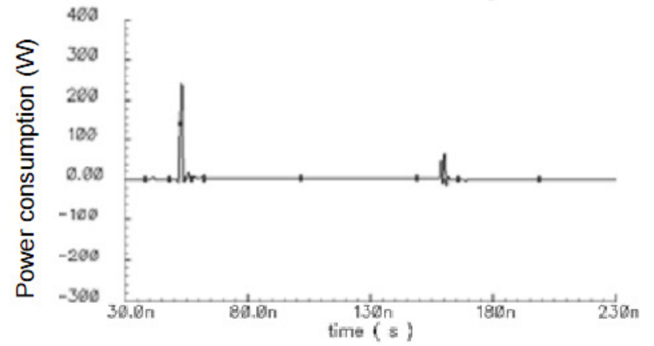


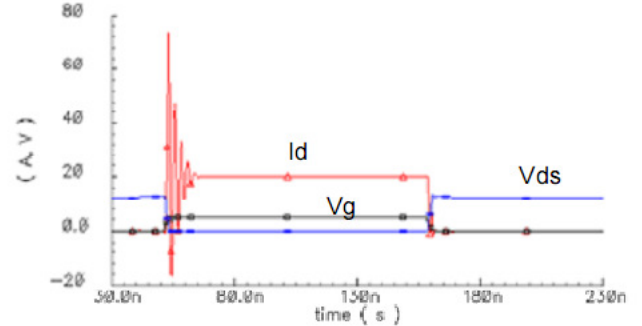
Figure 8 Dependence of high side MOSFET turn-on and turn-off loss on parasitic inductance in the main current flowing path. High side MOSFET turn-on loss increase as the parasitic inductance (Ls) decreases. The turn-off loss decreases as Ls decrease.





(a) Waveforms for Ls=2.0nH





(b) Waveforms for Ls=0.1nH

Figure 9 Calculated waveforms of High side MOSFET during turn-on and turn-off period for (a) Ls=2.0nH and (b) Ls=0.1nH in the condition of total gate circuit resistance = 0.4 Ω. In the case of L=0.1 nH, a large power loss occurs during turn-on period. In the case of L=2.0 nH, high side MOSFET drain-source voltage rapidly decreases because voltage of L*di/dt is applied to parasitic inductance, and high side turn-on loss is reduced.

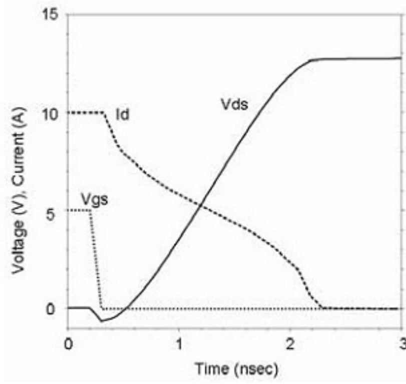


Figure 10 Turn off characteristics in the condition of Rg=0.4 Ω predicted by device simulation. The turn-off time is expected to be 2 nsec.

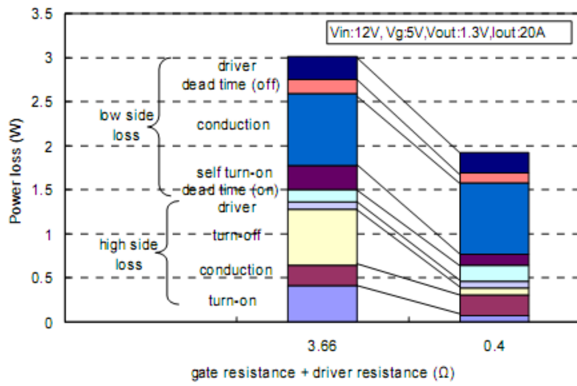
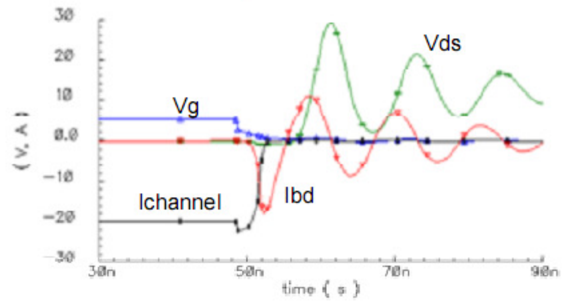
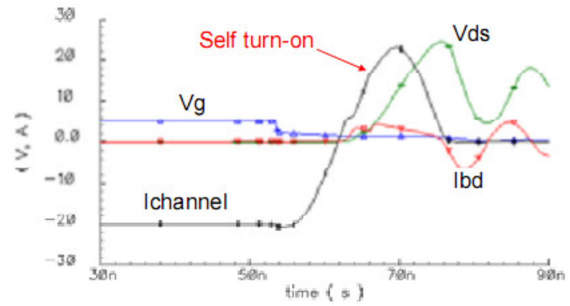


Figure 11 Power loss distributions for 3.66Ω and 0.4Ω of total gate circuit resistance. Reduction of gate resistance affects the losses of high side turn-on and turn-off, low side dead time and self turn-on loss.



(a) Total gate circuit resistance=0.4Ω.



(b) Total gate circuit resistance=3.66Ω.

Figure 12 Low side MOSFET waveforms when the high side MOSFET turns off. Fig.(a) shows the case of total gate circuit resistance=0.4Ω. (b) shows the case of total gate circuit resistance =3.66Ω. The large channel current peak (Ichannel) in (b) shows self turn-on of low side MOSFET. It is important to reduce gate resistance in order to decrease frequency dependent power loss.

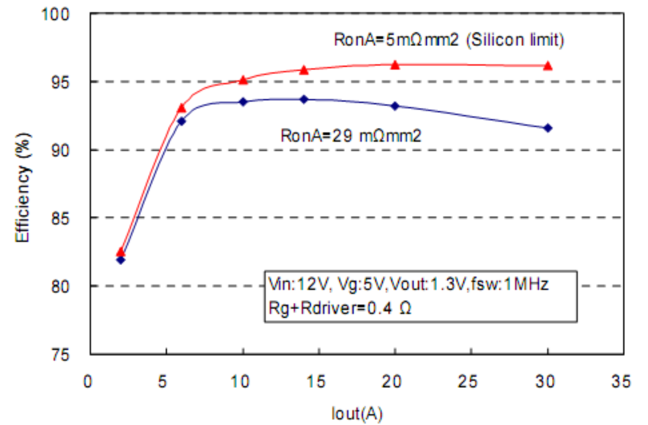


Figure 13 Dependence of efficiency on output current for current MOSFET (29mΩmm2) and silicon limit MOSFET (5mΩmm2). The calculated results predict that the maximum efficiency for ideal silicon MOSFET is 96% for 1MHz.

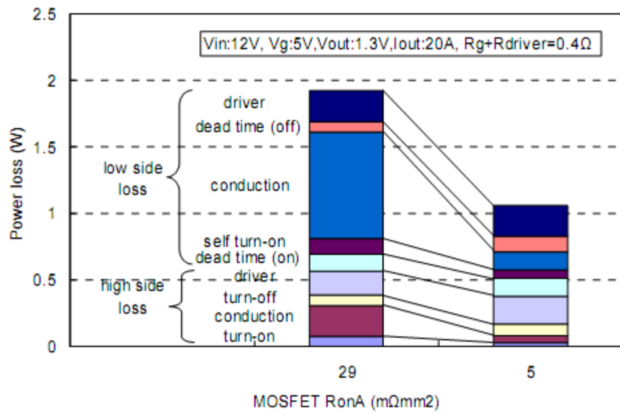


Figure 14 Power loss distributions for current MOSFET (29mΩmm2) and silicon limit MOSFET (5mΩmm2).

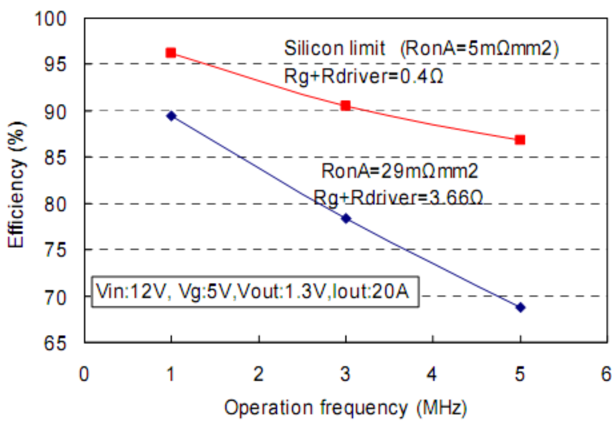


Figure 15 Dependence of efficiency on frequency. According to the result, the efficiency for 3.5 MHz for the ideal MOSFETs is equal to the efficiency obtained for the existing MOSFETs. It is concluded that the predicted operation frequency limit will be 5 MHz even if the ideal MOSFETs are adopted. The results predict that the switching frequency is limited to as high as 5MHz, if we assume more than 86% conversion efficiency, as far as the large current, 12V input voltage VRM are concerned.