NUMERICAL EXPERIMENT FOR 2500V DOUBLE GATE BIPOLAR-MODE MOSFETs(DGIGBT) AND ANALYSIS FOR LARGE SAFE OPERATING AREA(SOA)

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ABSTRACT

This paper proposes a double gate Bipolar-Mode MOSFET(DGIGBT) as a high-speed switching device exceeding 2500V. DGIGBT inherently has a reverse conducting diode in itself. It was numerically predicted that the 2500V DG-device will attain a better trade-off relation between turn-off time and forward voltage as compared with a 1800V single gate device.

It was experimentally comfirmed that Bipolar-Mode MOSFETs have a large SOA exceeding the theoretical power dissipation limit for an npn transistor. This paper also shows why the Bipolar-Mode MOSFET SOA can exceed this limit.

1. INTRODUCTION.

Bipolar-Mode MOSFETs[1,2] have a high switching speed of MOSFETs and a large current handling capability of bipolar transistors, simultaneously. Recent advances in the device design have enabled practical nonlatchup operation[3] in the Bipolar-Mode MOSFET, not only achieving a greater SOA than that for bipolar transistors[3] but also realizing sufficiently large current devices, comparable to Darlington bipolar transistors, such as 300A,1000V and 400A,500V devices[4].

Currently, the voltage capability is limited to below 1800V[5], because the device basically operates in a kind of transistor mode although its structure is the same as that for a thyristor.

In the present paper, first, a double gated structure is proposed, for the first time, to breakthrough the technological limitations and attain 2500V devices. Moreover, it is shown that the double gate Bipolar-Mode MOSFET inherently has a reverse conducting diode in itself.

Second, it is numerically analyzed why the Bipolar-Mode MOSFET SOA is large[6].

2. DEVICE SIMULATOR TONADDEII.

In this section, physical models included in the device simulator TONADDEII is described. TONADDEII[7] includes heavy doping effects based on effective Fermi statistics[8], Auger recombination, carrier to carrier scattering[9], impurity and electric field dependent mobility, and impurity dependent carrier lifetime.

Hole lifetime τ_p is given by the following expression:

$$1/\tau_p=1/\tau_i+1/\tau_1,$$

$$\tau_i=1\mu s\cdot[10^{18}/(N_D+N_A)]^{0.4},$$

Where τ_1 is the lifetime for a high resistivity region.

Electron lifetime τ_n is given by the following expression:

$$\tau_n=R\,\tau_p,\ (R=1.0 \text{ for the present calculations})$$

where R is chosen depending on what lifetime killer is introduced.

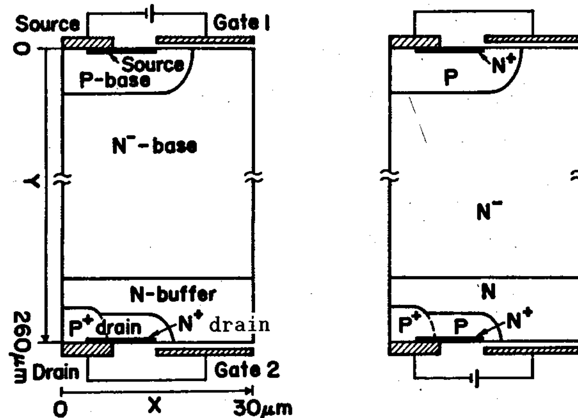

Fig.1 Basic structure and two fundamental operating modes.

3. DOUBLE GATE BIPOLAR-MODE MOSFET(DGIGBT).

Figure 1 shows a basic structure and two fundamental operating modes. Throughout the present paper, terms : N^+-drain, P-drain, N^--base, P-base, N^+-source are defined according to the figure. V_{th}=4V, ϕ_{FB}=-2.5V are assumed.

In Fig.1(a), gate-1 is positively biased and gate-2 is shorted to the drain electrode, providing ordinary forward bipolar-mode MOSFET operation. In Fig.1(b), gate-2 is positively biased, in contrast to Fig.1(a), and gate-1 is shorted to the source electrode. This configuration provides a forward blocking state and a bipolar-mode MOSFET operation in the reverse direction, serving as a reverse

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conducting diode. The voltage drop for the reverse conducting diode mode operation is expected to be lower than that for the forward bipolar-mode MOSFET operation because the N-buffer serves as an N-emitter.

In switching off the DG Bipolar-Mode MOSFET, positive gate-1 bias is reduced to zero and gate-2 is positively biased to induce an n-channel beneath the gate-2 electrode, effectively realizing an "anode short" structure and resultant short fall-time, regardless of there being a large carrier lifetime inside the device. Low forward voltage drop can be attained taking advantage of the large carrier lifetime and the punch-through structure with an N-buffer.

Figure 2 shows calculated forward current voltage characteristics by a device simulator TONADDEII. 2.75V forward voltage is attained for 10μs. electron and hole lifetime, 12.5V gate voltage and 50A/cm² current density in a 2500V DG device.

Figures 3 and 4 show calculated inductive turn-off waveforms. 0.65μs and 0.8μs fall-times could be obtained by adjusting the timing for creating n-channel anode short (n-channel shunt) in spite of 10μs. carrier lifetime.

In Fig.3, gate-2 was positively biased approximately 2μs before turning off the device or reducing the gate-1 bias. By creating the n-channel shunt, a few microseconds before turning off the device, the excess carriers inside the device were effectively removed, realizing a short fall-time.

Figure 5 to 10 show three dimensional plots for electron and hole densities for various time steps corresponding to the turn-off waveforms shown in the Fig.3. Each figure includes three types of carrier distributions: (a)a three dimensional electron density distribution; (b)another electron density distribution from a view angle opposite to that of (a); (c)hole density distribution from the same view angle as that of (a).

Figure 5 shows those three plots for the initial time step. First,the gate-2 voltage is raised from -2.5V to 12.5V in 0.4μs. Figure 6 shows those for the time step t=1.98μs. It is seen that carriers in the N-buffer are being removed through the created n-channel shunt. This situation is more clearly seen in Figure 11, which shows electron density distributions along the symmetry axis passing through the centers of the two gates.

From t=2μs, the gate-1 voltage begins to be reduced to turn off the device. Figure 7 to 9 show the transient carrier density distributions during the storage-time. Electron current still exists in the depletion layer only under the gate-1 electrode until the gate-1 voltage becomes below the threshould voltage, as seen in Fig.8. After the n-channel disappears under the gate-1 electrode, all of the current is carried by holes in the depletion layer, where all of the charge consists of positive donors and holes as seen in Fig.9.

It should be noted that the hole accumulation layer appears under the gate-1 electrode even though the gate-1 voltage is not negative as seen in Fig.7 to 10.

Figure 10 shows carrier distributions for t=2.54μs. in the fall-time period. It is clearly seen from Fig.11 that the rapid decay in the current comes from the fact that the excess carriers is reduced to less than the tenth of the

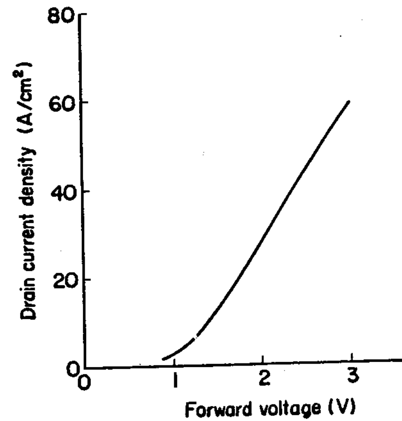


Fig.2 Calculated current-voltage relation by a device simulator TONADDEII

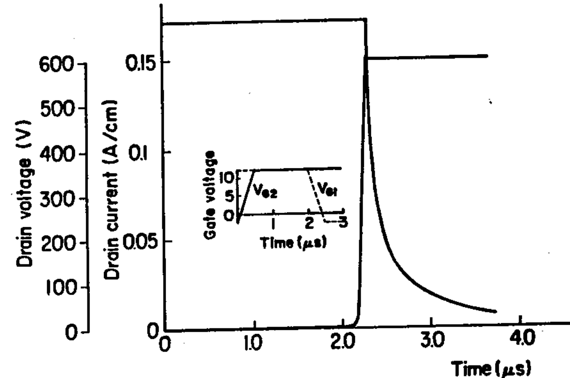


Fig.3 Caluculated inductive turn-off waveforms when positive gate-2 bias is applied 2μsec before the gate-1 is turned-off.
Solid line shows gate-2 waveform and broken line shows gate-1 voltage waveform, respectively in the inserted figure.

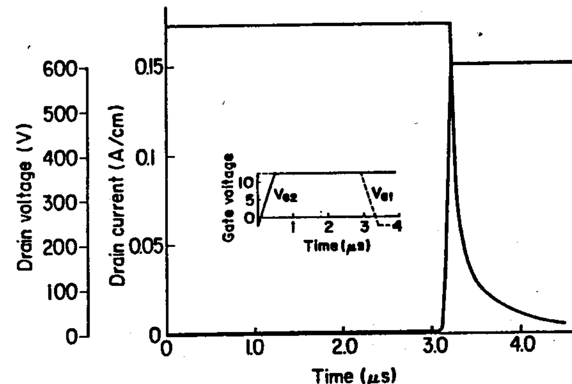
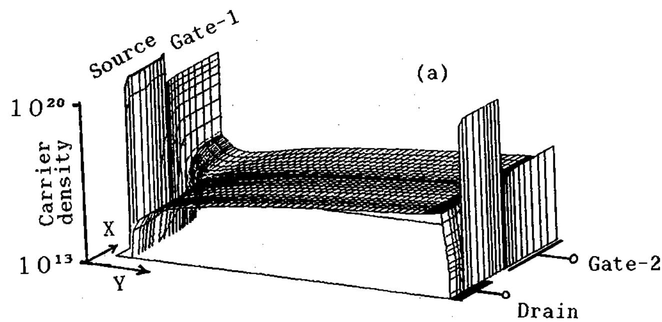
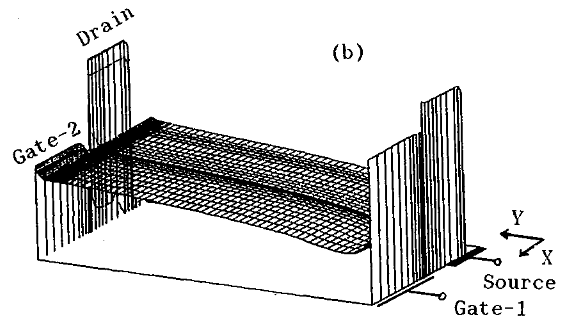


Fig.4 Caluculated inductive turn-off waveforms when positive gate-2 bias is applied 3μsec before the gate-1 is turned-off.
Solid line shows gate-2 waveform and broken line shows gate-1 voltage waveform, respectively in the inserted figure.





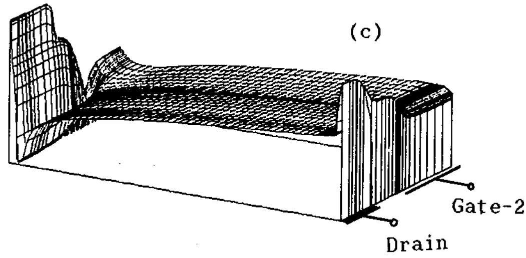
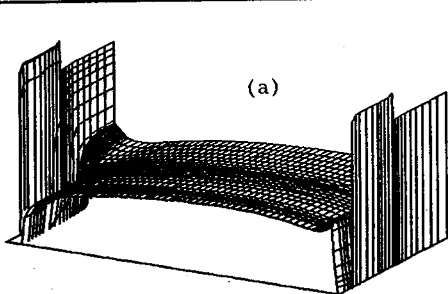
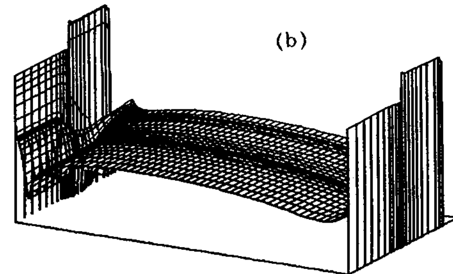


Fig.5 Carrier density distributions for $t=0\mu sec.$:
(a)3-D electron density distribution,
(b)electron density distribution from a view angle opposite to that of (a),
(c)density distribution from the same view angle as that of (a).





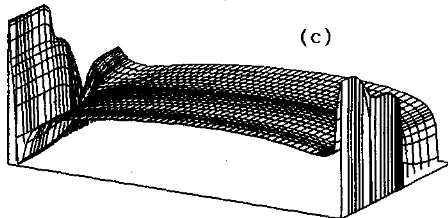
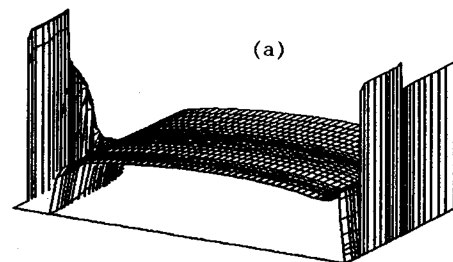
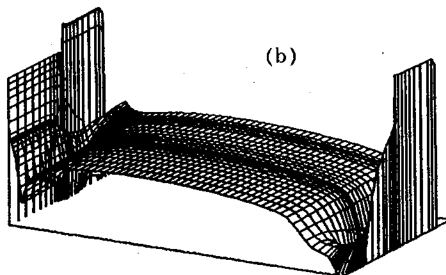


Fig.6 Carrier density distributions for $t=1.98\mu sec.$





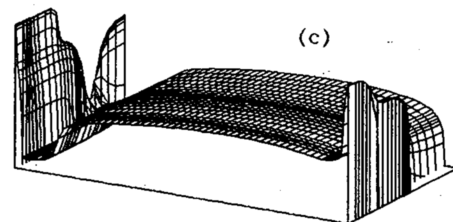
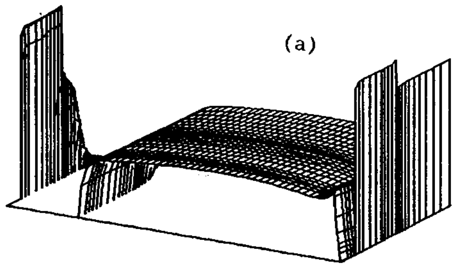
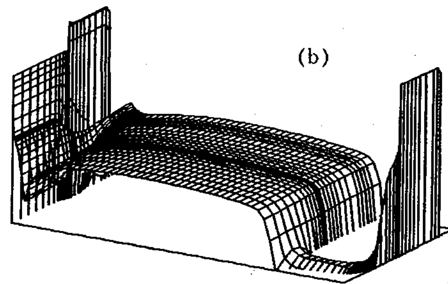


Fig.7 Carrier density distributions for $t=2.2\mu sec.$





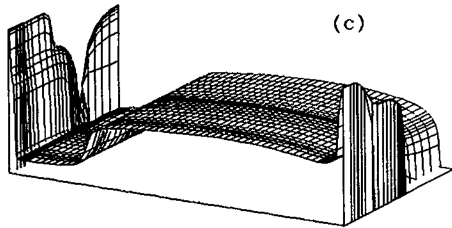
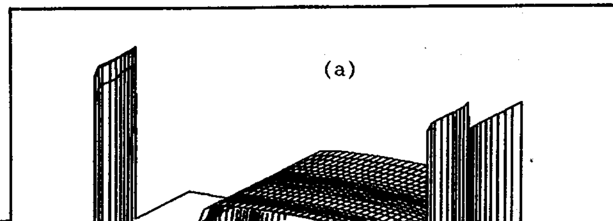
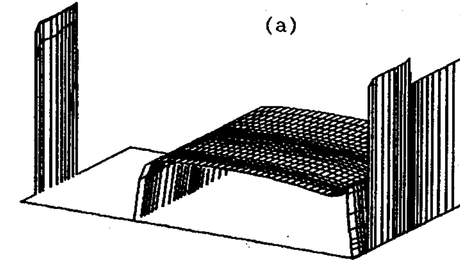
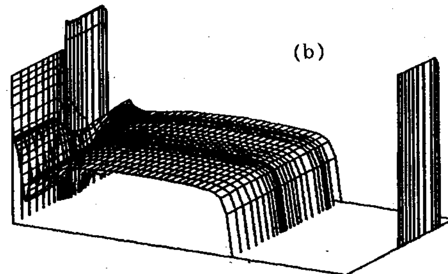


Fig.8 Carrier density distributions for t=2.23μsec.







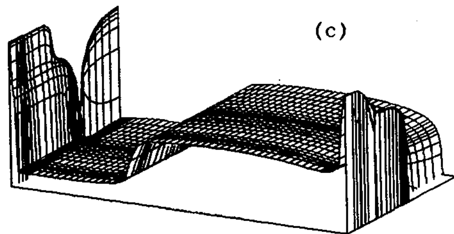
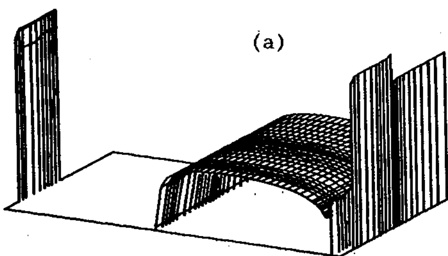
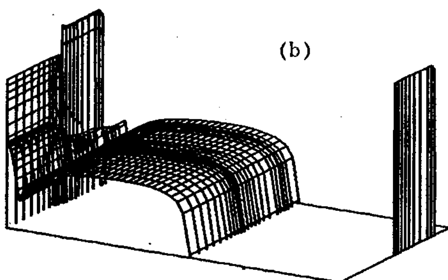


Fig.9 Carrier density distributions for t=2.3μsec.





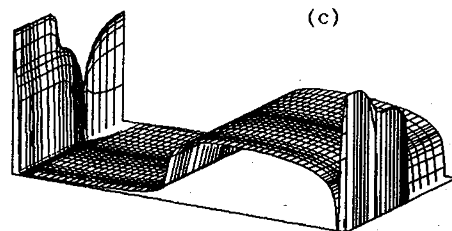


Fig.10 Carrier density distributions for t=2.54μsec.

initial value.

Figure 12 shows the comparison in the trade-off relation between 1800V single gate device and 2500V DG device. It is expected that a 2500V DG device have a better characteristics than a 1800V single gate device.

However, an expected major problem for the DG device is what kind of package should be used.

4. NUMERICAL ANALYSIS ON WHY THE SOA FOR BIPOLAR-MODE MOSFET IS LARGE.

In this section, two dimensional numerical analysis is carried out to analyze a large SOA for the Bipolar-Mode MOSFET.

Figure 13 shows the analyzed 600V device structure and the outer circuit. A sufficiently large inductance with an ideal free wheel diode is adopted for a load impedance. Calculations were carried out under the assumptions that the drain current is kept constant until drain voltage recovers to the electric source voltage. Figure 14 shows one of typical calculated turn-off waveforms. Electron and hole carrier lifetimes for the high resistivity region were assumed to be 0.13μsec. Carrier lifetimes for more highly doped region is given by the same expression described in Section 2. Gate voltage was decreased from 12.5V to 0V in 0.1μsec.

As the gate voltage decreases, the device resistance simply increases and depletion layer develops beneath the P-base as well as under the gate electrode. Channel electron current flows only under the gate electrode, as seen in Fig.15, after the anode voltage begins to recover. Thus, conductivity is relatively high even in the depletion layer only under the gate electrode region, where both electron and hole current flow. On the other hand, in the depletion layer beneath the P-base region, all of the current is carried by holes. This situation is seen in Fig.16. While channel electron current exists, the hole current density flowing up directly under the P-base is lower than the average current density,because most of the current flows in the high conductivity area under the gate electrode, where both electrons and holes exist.

The stored excess carriers beneath the depletion layer are swept away by the depletion layer expansion. The swept away electrons serve as base current to the PNP transistor portion. The sum of the electron base currents, consisting of electrons from the channel and swept away electrons due to depletion layer expansion, is kept constant during the storage time. The swept away holes from the depletion layer and the holes injected from the P-emitter(P-drain) constitutes the total hole current flowing into the P-base. Hole current becomes considerably uniform in the turn-off transient as compared with the initial state(t=0), because the hole current components due to the depletion layer expansion flow uniformly.

After channel electron current completely ceases (the gate voltage becomes below the threshould voltage), all of the current is carried by holes. Hole current density beneath the P-base becomes greater than the average current density (see 300V case in Fig.16). Thus, it is predicted that SOA determined by avalanche breakdown will become

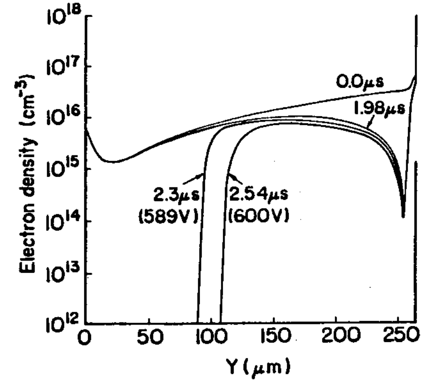


Fig.11 Electron density distribution vs. distance from the center of the gate-1 electrode shown as a function of time. The numbers in the parentheses show corresponding applied drain voltages.

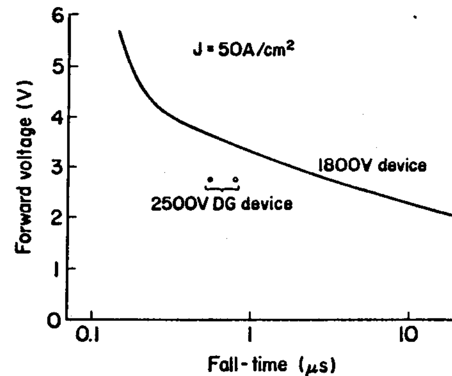


Fig.12 Comparison in trade-off relation between 2500V DG device and 1800V single gate device.

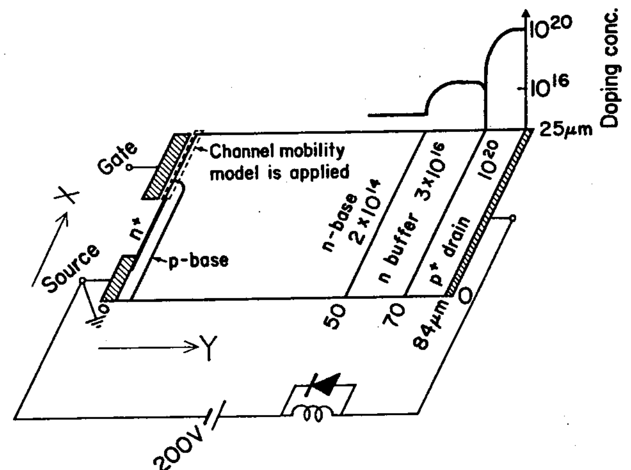


Fig.13 Analyzed 600V device structure and outer circuit configuration.

greater as the total P-base area becomes larger for a unit device area.

Another important conclusion is that if the device resistance is sufficiently large, channel electron current still exists even after anode voltage has recovered to the electric source voltage level. This situation is realized for the cases of low carrier lifetime or low hole injection efficiency, ie. for the cases where most of the current is carried by electrons in the steady state. In addition, a slow dV_G/dt driving condition is effective.

Figure 17 shows this example. dV_G/dt rate is reduced to one forth of that for Fig.14 and carrier lifetime is reduced to 0.1μsec. Figure 18 shows current density distribution for a time step when anode voltage has just reached 200V. Hole current density beneath the P-base is only a half of the average current density (=122A/cm^2). Hole and electron density distributions corresponding to Fig.18 are shown by the curves A in Fig.19. Maximum electric field appears where the arrow indicates. If the device maximum current is limited by avalanche breakdown not by latch-up, and if avalanche breakdown is determined by the positive charge density beneath the P-base, it can be shown that apparent power dissipation can exceed the transistor theoretical limit, This is true as long as the channel electron current still exists when the anode voltage reaches its peak value in the turn-off transient as is proven in the following. Positive charge C^+ is given by:

$C^+=N_D+p=N_D+J/qv_s$

Thus, allowable maximum voltage V_{BD} is given by the following expression:

$$V_{BD}=60(E_G/1.1)^{1.5}([N_D+J_p/qv_s]/10^{16})^{-3/4}$$

$$=60(E_G/1.1)^{1.5}\{[N_D+\frac{I_D-(1+\alpha)I_{ch}}{qv_s S}]/10^{16}\}^{-3/4}$$

where S is the effective P-base area, Ich the channel electron current, v_s the saturated hole velocity N_D the donor concentration and α the factor which takes into account the enhanced hole current density under the gate electrode due to the existence of electron hole plasma. Thus, power dissipation can exceed the pnp transistor theoretical limit unless Ich is zero.

Figure 19 also shows the charge distribution for the case (curve B), where no channel electron current exists. The breakdown voltage under a large drain current condition becomes lower for this case.

It should be pointed out that if the dV_G/dt rate is too steep, channel electron current ceases rapidly, because a large amount of excess carriers afford to supply a large drain current due to depletion layer expansion.

If the device p-base resistance is high and the maximum current is limited by latch-up, then the maximum controllable current may decreases as the carrier lifetime decreases. This is because a larger hole current flows up especially under the gate electrode as seen in Fig.18, causing a large lateral voltage drop in the p-base beneath the source layer.

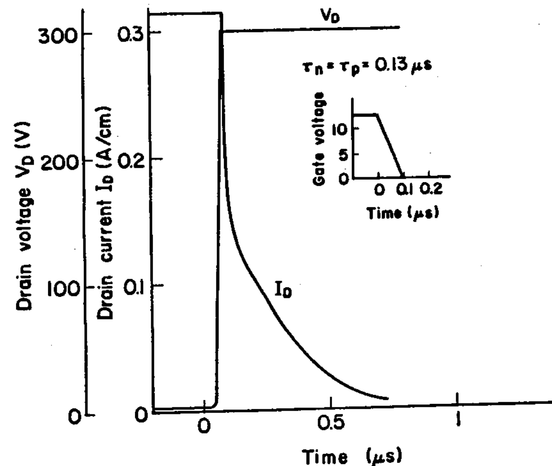


Fig.14 Calculated inductive turn-off waveforms (0.13μs carrier lifetime).

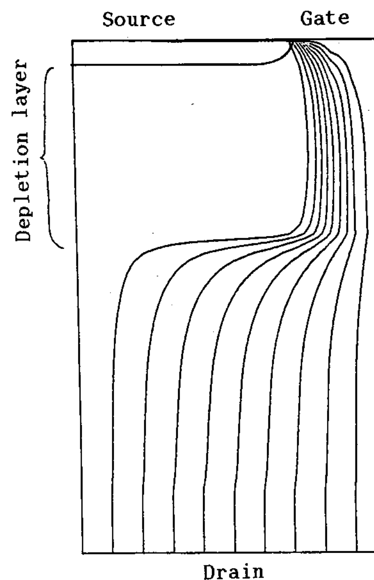


Fig.15 Channel electron current flow line for 183V drain voltage.

5. CONCLUSION.

A 2500V DG Bipolar-Mode MOSFET was proposed. It was shown that a DG device inherently has reverse conducting diode in itself and that it has a better trade-off relation than a 1800V single gate device.

Numerical analysis predicted that the channel electron current plays an important role for a large SOA if it exists even after the drain voltage recovers, because it neutralizes positive charges in the depletion layer .

REFERENCES

[1]A.Nakagawa et al, 1984 Ext.Abs.16th Conf. Solid-State Devices Mater., p.309
[2]B.J.Baliga et al, 1982 IEDM Tech.Digest., p.264.
[3]A.Nakagawa et al, 1985 IEDM Tech.Digest., p.150. A.Nakagawa et al, IEEE Trans. Electron Devices, ED-34, p.351(1987)
[4]Toshiba data sheet.
[5]A.Nakagawa et al, 1986 IEDM Tech.Digest., p.122.
[6]A.Nakagawa et al, 1987 Ext.Abs.19th Conf. Solid-State Devices Mater., p.43.
[7]A.Nakagawa et al, Proceedings of NASECODE-V.
[8]A.Nakagawa, Solid-St. Electron 22,p.943(1979)
[9]M.S.Adler, IEEE Trans. Electron Devices, ED-25, p.16(1978)

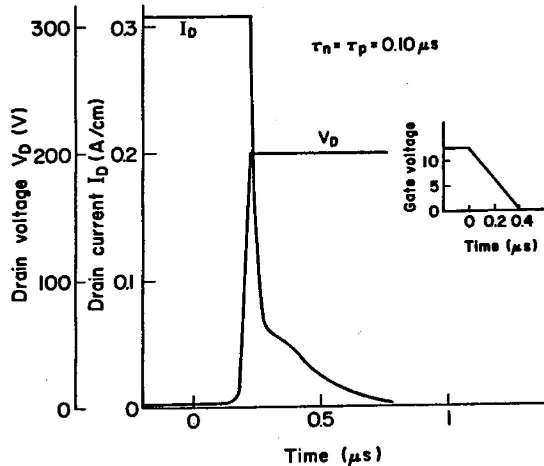


Fig.17 Calculated inductive turn-off waveforms(0.1μs carrier lifetime)

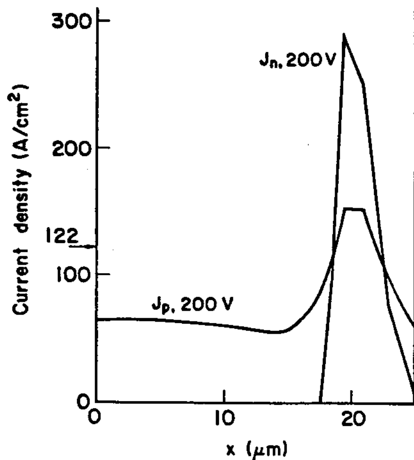


Fig.18 Hole and electron current density flowing across y=6.6μm line vs. x-axis when anode voltage just has become 200V.
Average current density=122A/cm^2.

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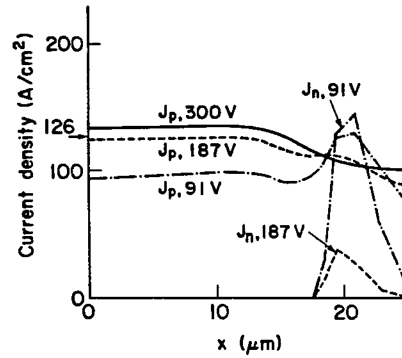

Fig.16 Distribution of hole and electron current density flowing across y=6.6μm line vs.x-axis, corresponding to Fig.14, with anode voltage as a parameter. Average current density=126A/cm^2.

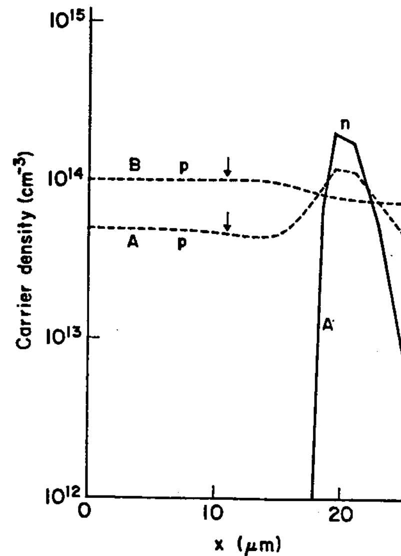

Fig.19 Carrier density distribution on y=6.6μm line. Curve A correspond to Fig.18. Solid and broken lines denote electron and hole density, respectively.